

4111/CX4111 COMPUTER DISPLAY TERMINAL

*Please Check for
CHANGE INFORMATION
at the Rear of This Manual*

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS
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PRODUCT: 4111 and CX4111 Computer Display Terminals

This manual supports the following versions of this product: Serial Numbers B010100 and up.

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OPERATORS SAFETY SUMMARY

This general safety information is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

IN THIS MANUAL

CAUTION statements identify conditions or practices that can result in damage to the equipment or other property.

WARNING statements identify conditions or practices that can result in personal injury or loss of life.

AS MARKED ON EQUIPMENT

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

IN THIS MANUAL



This symbol indicates where applicable cautionary or other information is to be found.

AS MARKED ON EQUIPMENT



DANGER high voltage.



Protective ground (earth) terminal.



ATTENTION — refer to manual.



Refer to manual.

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

OPERATORS SAFETY SUMMARY

GROUNDING THE PRODUCT

This product is grounded through the grounding conductor of the power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the power input or output terminals. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

DANGER ARISING FROM LOSS OF GROUND

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

USE THE PROPER POWER CORD

Use only the power cord and connector specified for your product.

Use only a power cord that is in good condition.

Refer cord and connector changes to qualified service personnel.

USE THE PROPER FUSE

To avoid fire hazard, use only the fuse specified in the parts list for your product, and which is identical in type, voltage rating, and current rating.

Refer fuse replacement to qualified service personnel.

DO NOT OPERATE IN EXPLOSIVE ATMOSPHERES

To avoid explosion, do not operate this product in an atmosphere of explosive gases unless it has been specifically certified for such operation.

DO NOT REMOVE COVERS OR PANELS

To avoid personal injury, do not remove the product covers or panels. Do not operate the product without the covers and panels properly installed.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

DO NOT SERVICE ALONE

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

USE CARE WHEN SERVICING WITH POWER ON

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing the power supply shield, soldering, or replacing components.

DO NOT WEAR JEWELRY

Remove jewelry prior to servicing. Rings, necklaces, and other metallic objects could come into contact with dangerous voltages and currents.

X-RADIATION

X-ray emission generated within this instrument has been sufficiently shielded. Do not modify or otherwise alter the high voltage circuitry or the CRT enclosure.

POWER SOURCE

This product is intended to operate from a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.

HANDLING

Due to the weight of the Monitor, and its component subassemblies, at least two persons are required to perform installation or service to prevent injury to personnel or damage to the Monitor.

IMPLOSION PROTECTION

Whenever the implosion shield is removed from the CRT, protection against implosion hazard is reduced. Service personnel should wear full face masks and protective clothing at any time the CRT is removed from the CRT module or the implosion shield is not in place.

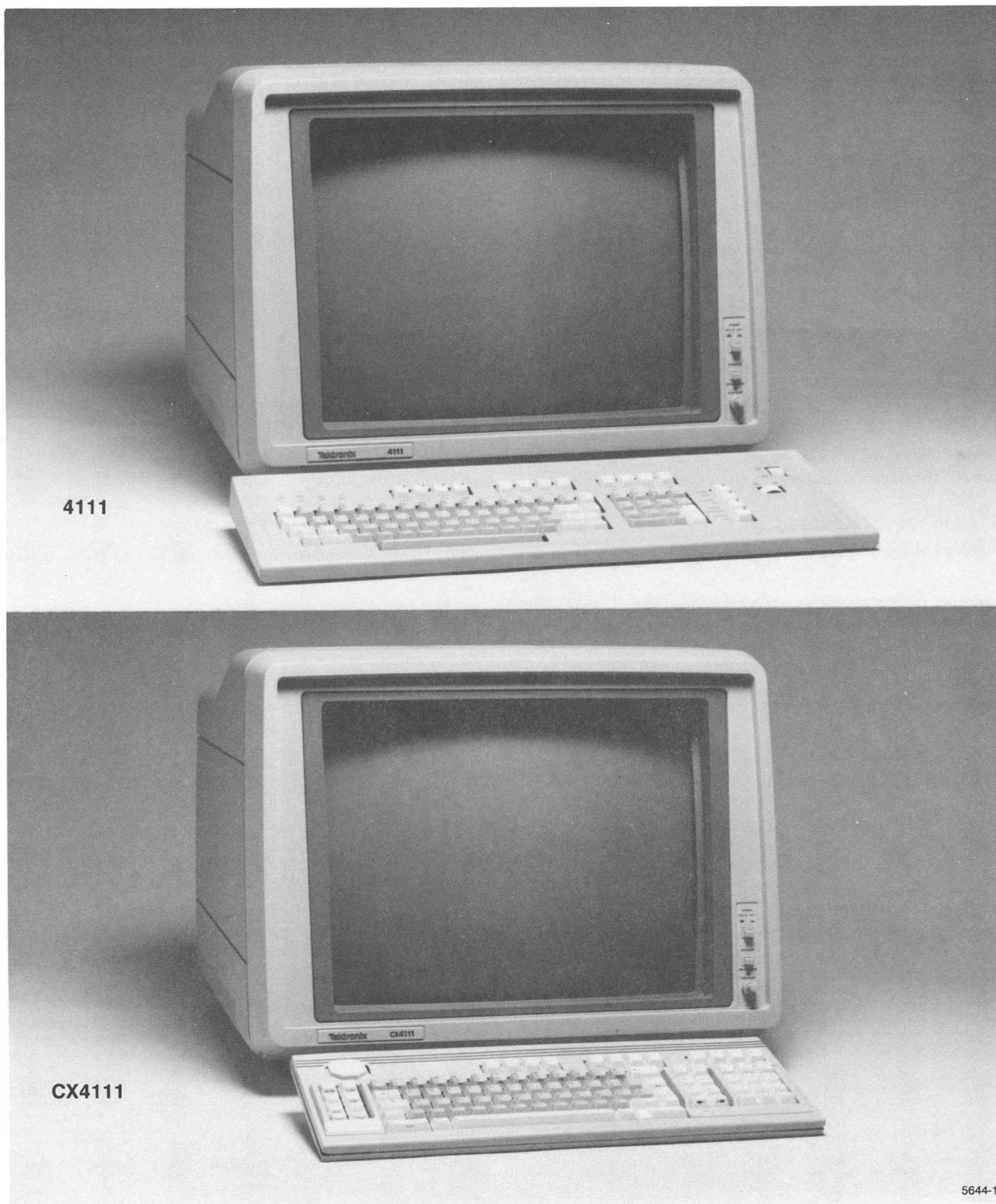


Figure 1-1. 4111 and CX4111 Computer Display Terminals.

Section 1

INTRODUCTION

USING THIS MANUAL

This manual contains service information for the standard 4111 Computer Display Terminal and for the CX4111 Computer Display Terminal. Throughout the remainder of this manual, the 4111 and CX4111 are generally referred to as the "terminal" unless specifically called out.

This manual provides detailed descriptions for all parts of the terminal except for the Display Module, and Keyboards. For detailed service information on these parts, refer to additional service manuals described further in this manual.

This manual is divided into ten sections and three appendices that cover the following topics:

- Section 1 — *Introduction*, describes manual contents, related documentation, the terminals, options, and accessories.
- Section 2 — *Specification*, presents product characteristics in a tabular format.
- Section 3 — *Operating Information*, describes terminal controls and indicators, and specific Self-test information necessary for the service technician.
- Section 4 — *Theory of Operation*, discusses the electronic design of the terminal; an overview of terminal operation is followed by detailed circuit descriptions for each module or circuit board.
- Section 5 — *Checks and Adjustments*, presents procedures for functionally checking the terminal, and describes how to adjust each part of the terminal.
- Section 6 — *Maintenance*, presents mechanical disassembly/assembly procedures and interpretation to Self-test error messages.
- Section 7 — *Installation*, provides procedures for installing a terminal.
- Section 8 — *Replaceable Electrical Parts*, lists electrical parts and subassemblies that can be ordered.
- Section 9 — *Diagrams*, provides circuit board interconnect diagrams, schematics, component location figures, and timing diagrams.
- Section 10 — *Replaceable Mechanical Parts*, lists mechanical parts and subassemblies that can be ordered.
- Appendix A — *Signal List*, describes major signals for the terminal.
- Appendix B — *PAL Information*, provides a detailed description of Programmed Array Logic (PAL) ICs used in the terminal.
- Appendix C — *CX Terminal Interfacing Information*, describes the coaxial CX terminal, the IBM Control Unit (Cluster Controller), and the IBM host interface.

The display module for your terminal may be different. (The GMA302N Display Module was used with earlier version 4111's. Later version 4111's and the CX4111 terminals use the 119-2387-00 Display Module.) All significant service information for the different display modules is contained in separate service manuals. Those manuals contain a theory of operation, repair procedures, parts lists, and full schematics.

In addition, Section 5 of this manual contains two adjustment procedures for the display in the 4111/CX4111 application (one for the GMA302 Display Module, and one for the 119-2387-00 Display Module). Section 6 also contains disassembly and reassembly procedures for the different display units as applied to your terminal.

The terminal is compatible with most applications designed for the Tektronix 4100 and 4110-series terminals (4107, 4109, 4113, 4113B, 4115, 4115B, etc.). Applications designed for use with the 4125 Workstation can also be used with the 4111.

The CX4111 is identical to the 4111 except that the CX terminal contains an IBM-style keyboard, an IBM interface board, and a coax connector for connection to an IBM Control Unit.

All peripherals to this terminal are covered in their separate service manuals. These include hard copy units, printers, and programmability unit.

Refer to the appropriate service manual for further detailed information about the display modules, or keyboards.

RELATED DOCUMENTS

Additional information regarding the 4111 or CX4111 Computer Display Terminal is contained in the following documents:

- The *GMA302 19-inch Color Raster Monitor Service Manual*, which contains a detailed description of the display specifications, theory of operation, checks and adjustments, maintenance and troubleshooting information, electrical and mechanical parts lists, and block/interconnect/schematic diagrams.
- The *119-2387-00 Display Module Service Manual*, which also contains specifications, a detailed theory description, checks and adjustments, maintenance and troubleshooting information, electrical and mechanical parts lists, and block/interconnect/schematic diagrams.
- *4111 Computer Display Terminal Operators Manual*.
- *CX4111 Computer Display Terminal Users Information Supplement*, which describes the differences and added features of the CX4111.
- *4110/4120 Series Host Programmers Manual*.
- *4110/4120 Series Command Reference Manual*.
- *4110/4120 Series Reference Guide*.
- *4120 Series Serial Keyboard Service Manual*, which describes the standard 4111 keyboard with thumbwheels.
- *119-1989-00/119-2315-00 Keyboards with Mouse Technical Data Manual*, which describes the optional 4111 keyboard with the Joydisk. This manual contains information on theory, disassembly, schematics, and part ordering.
- *119-1990-00/119-2307-00 CX Keyboards with Mouse Technical Data Manual*, which describes the optional CX4111 keyboard with the Joydisk. This manual also contains information on theory, disassembly, schematics, and part ordering.

INSTALLATION INFORMATION

Section 7 provides complete instructions for installing the terminal. Immediately after receiving the terminal, unpack and inspect it for possible shipping damage. Do not throw away the shipping container until the terminal passes the damage inspection and is fully operational. Run the Self-test program to be sure the terminal works (see Section 5, Checks and Adjustments). Also verify that all accessories checked on the Accessories Packing Slip are included and work properly.

4111 OVERVIEW

GENERAL DESCRIPTION

The 4111 and CX4111 are low-cost color graphics terminals. They are microprocessor-controlled color graphics computer terminals capable of creating or modifying complex graphics locally and then storing these graphics locally.

The terminals use microprocessor technology to process graphics-related and text-editing commands. Using these commands, the terminals can create (or receive from a host computer) color graphic images, display and modify those images, and transmit them to the host computer. Using the local graphics capability, the host graphics processing time burden is reduced, thus reducing host overhead.

The primary applications for the 4111 are:

- Multiple-user CAD/CAM systems.
- Text/graphics entry/editing.
- Technical data analysis (complex charts, graphs, and maps).

The CX4111 is a graphics terminal that connects directly to any IBM system (via its coaxial host interface). Its primary applications are the same as the standard 4111, but the user can switch between an RS-232 host and an IBM host without ending either session.

These terminals present graphics and text data on a high-resolution 19-inch diagonal measurement, color raster-type crt. The display resolution of the crt is 1024 × 768 pixels, non-interlaced. The display refreshes at the rate of 60 Hz. Both graphics and text data are displayable in color (selected from 4096 possible hues). A total of 16 colors are displayable at one time:

- 16 colors are displayable in the graphics part of the display.
- 8 color pairs (for character foreground and background) may be used to display text and dialog information. The 8 color pairs are chosen from the 16 graphics area colors.
- 1 color shows the crosshair graphics cursor (when present).

The 4111 standard keyboard is detached and contains an ASCII keyset, a numeric keypad, 12 special-purpose function keys, and two cursor thumbwheels. An optional keyboard for the 4111 provides a graphics Joydisk in place of the thumbwheels and has fewer dedicated function keys. Both the Joydisk and cursor thumbwheels control the position of the graphics cross-hair cursor and scroll text on the screen. The CX4111 keyboard uses the IBM-style layout and contains special keys for that host environment.

The standard terminal has 256K bytes of RAM (read/write) memory with 1024K of additional optional RAM available. The maximum host computer-to-terminal communications speed ("baud rate") is 19,200 bits per second (bps). The maximum speed for RS-232 communications is 38.4 kbaud with flagging. By using direct memory access (DMA), one can communicate at rates up to 737 kbaud.

In addition to the commands that communicate with the host computer, the terminal has a feature called Setup mode. Setup mode uses English-language-type commands to initialize many terminal operating parameters locally. The major classifications of Setup commands are:

- General terminal control
- Dialog area control
- File transfer control
- Graphics input (GIN) control
- Standard and blockmode communications control
- Two port peripheral interface (2PPI) control
- Graphics tablet control
- Screen copy control

These parameters can be set to the desired quantity or mode by the operator when the terminal is placed in Setup mode.

Most commands for the terminal are encoded as three-character ASCII codes beginning with the E_c character. The host computer controls the terminal by sending it these three-character "escape" sequences in the order determined by each specific job to be done. (The Setup mode commands are encoded both as English-language type commands and as E_c sequences.) The terminal also accepts selected ANSI X3.64 text-editing commands.

In addition, the terminal has a self-diagnostics system called Self-test. Self-test uses messages displayed on the screen and the keyboard bell to inform the user that an error has occurred. The error messages provide a valuable servicing tool for locating most malfunctions.

INTRODUCTION

PHYSICAL DESCRIPTION

Figure 1-2 shows the major modules in the 4111 terminals, while Figure 1-3 shows the major parts of the CX4111. Figure 1-4 shows the major parts of the early version display (GMA302 Display Module), and Figure 1-5 shows the major parts of the later version display (119-2387-00 Display Module).

An RS-232 connector, on the rear panel connects to the host. The Two Port Peripheral Interface (2PPI) provides two RS-232 connectors on the rear panel for peripheral devices such as plotters and a graphics tablet unit. There is also a separate copier connector for the Tektronix 4690-series color copiers (this connector can also support Centronics-style printers and monochrome copiers). The COMM connector on the back of the CX4111 accepts a coax cable from an IBM 3274 Control Unit.

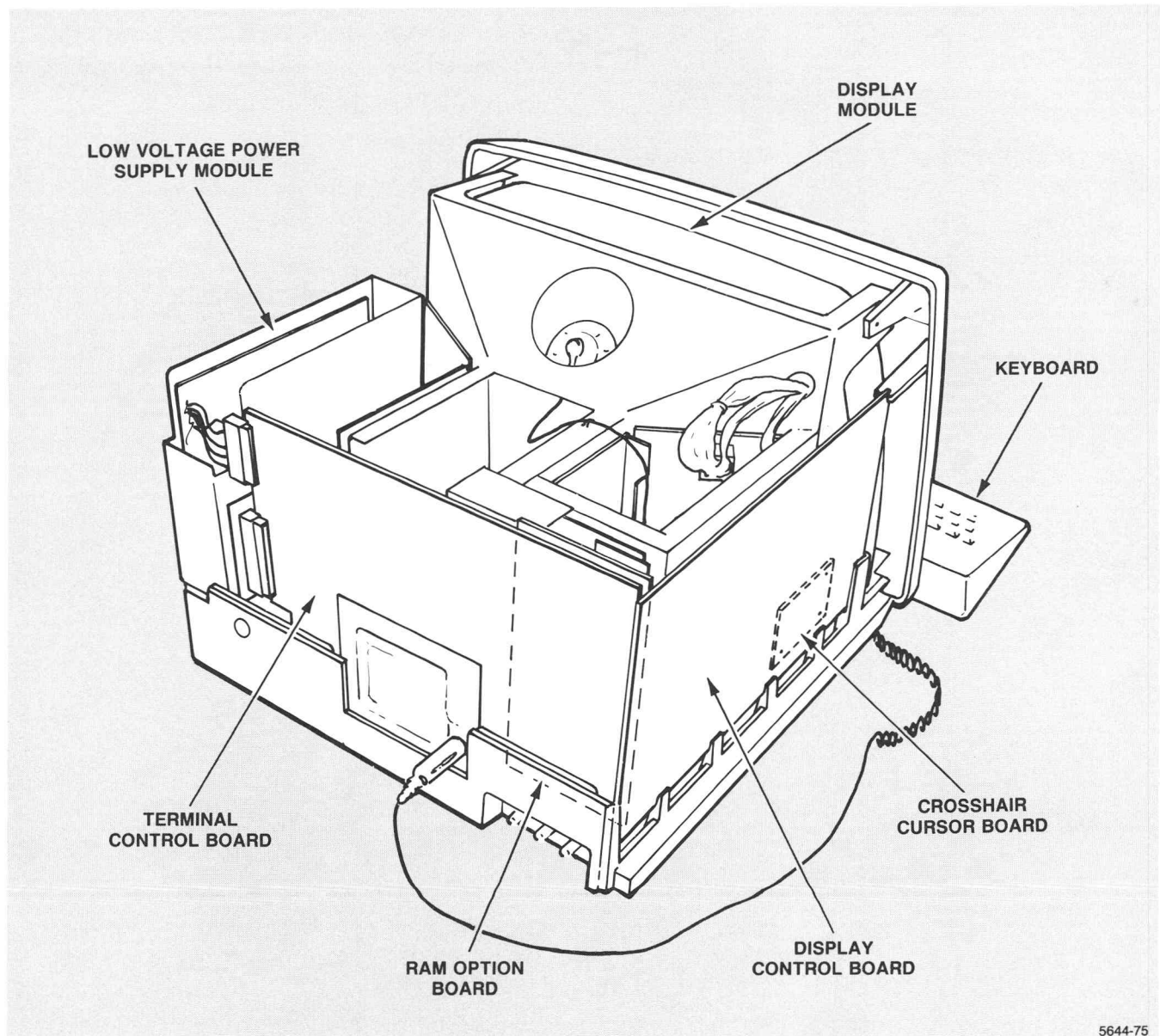


Figure 1-2. The 4111 Terminal's Functional Modules.

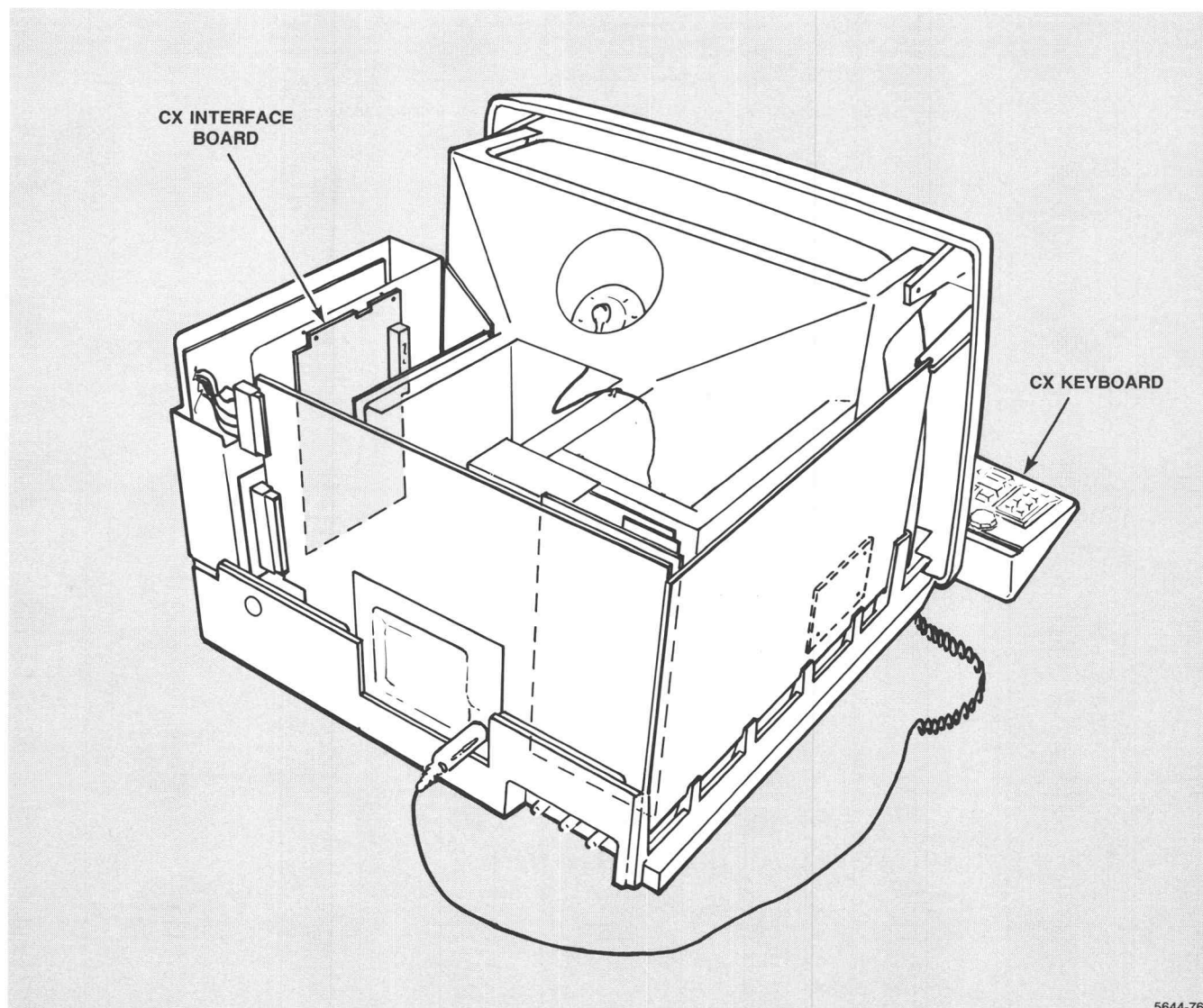


Figure 1-3. The CX4111 Terminal's Functional Modules.

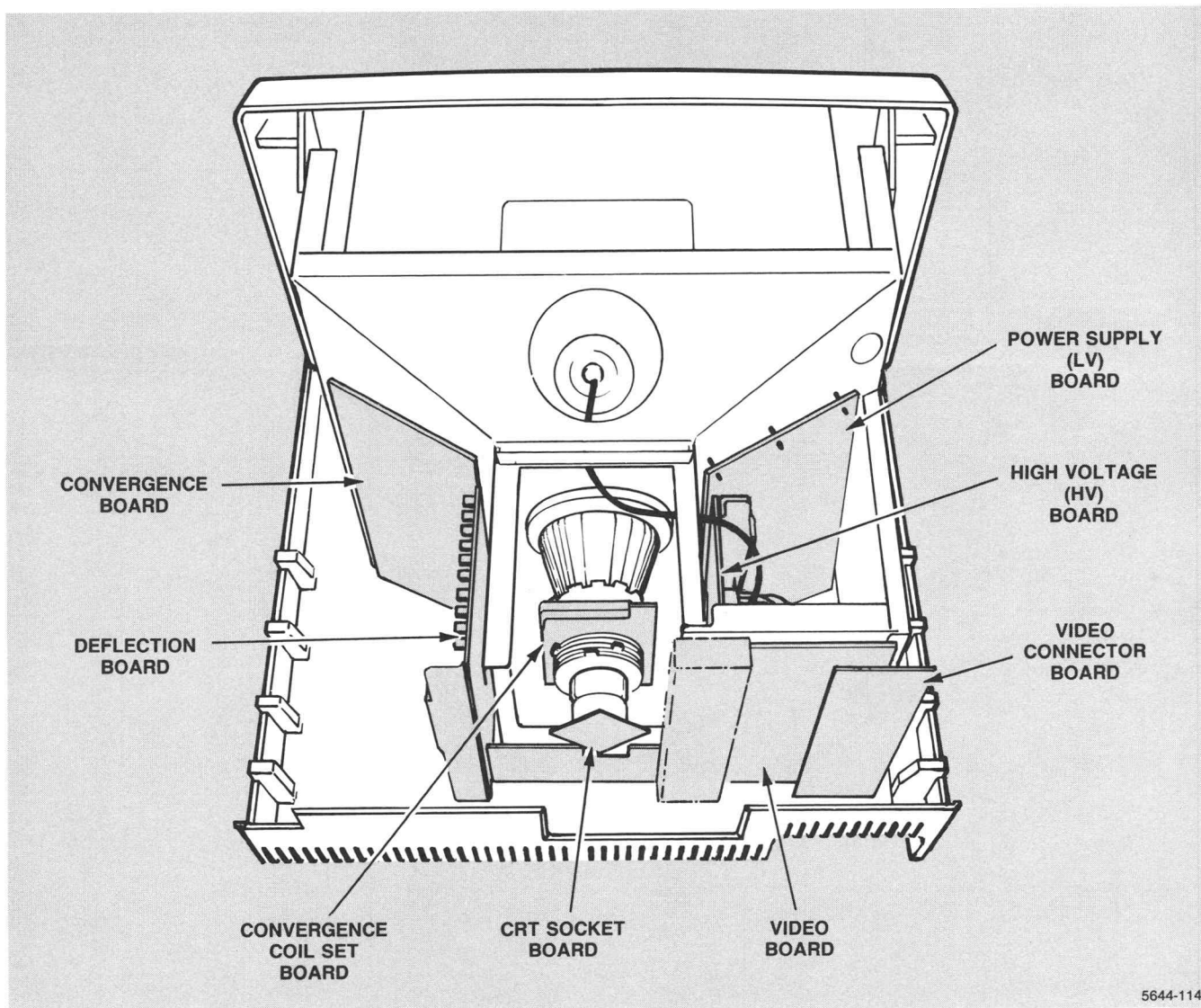


Figure 1-4. Circuit Boards in the GMA302 Display Module.

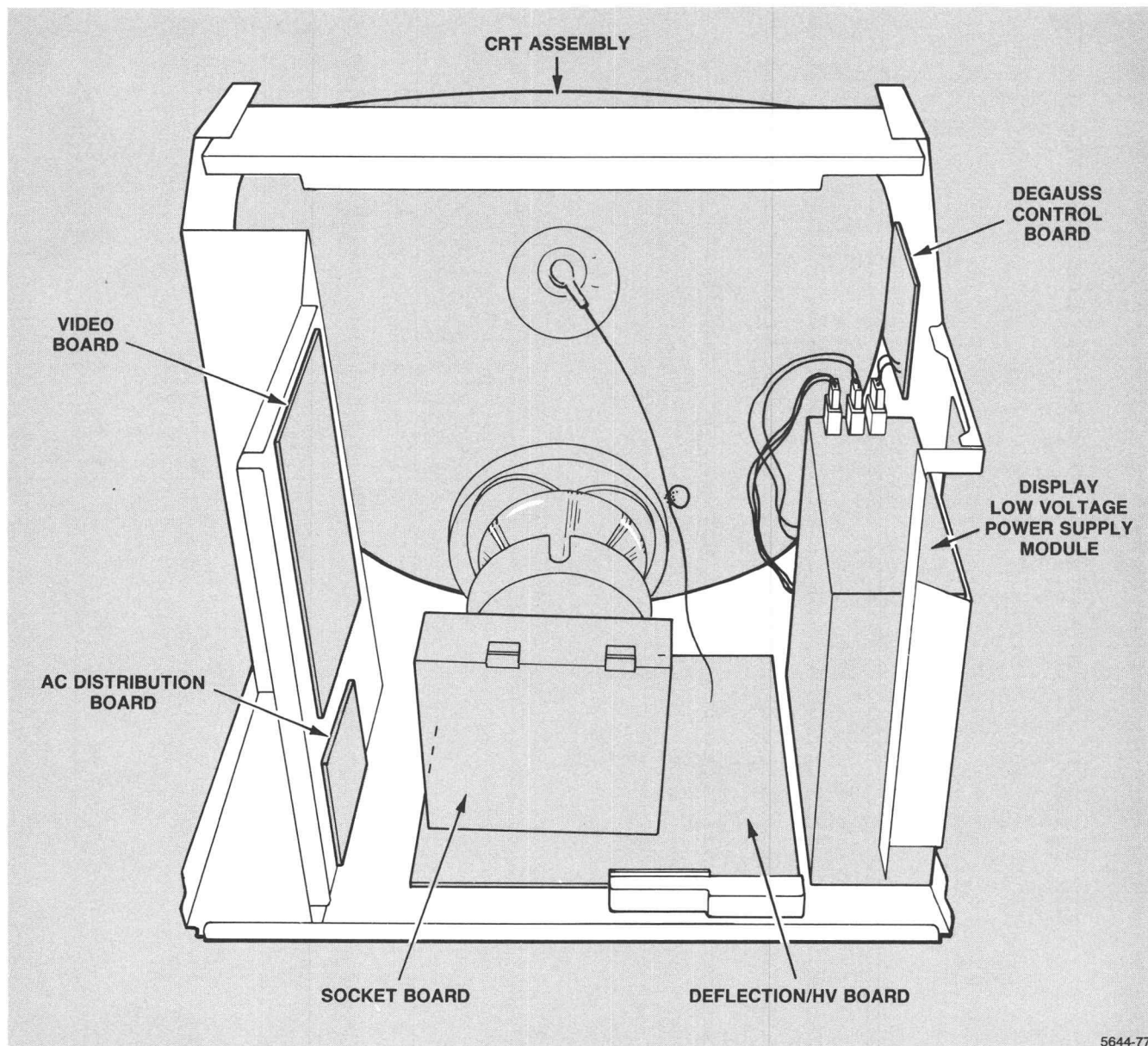


Figure 1-5. Circuit Boards and Assemblies in the 119-2387-00 Display Module.

INTRODUCTION

OPTIONS

Table 1-1 describes the options that are available for the 4111 Computer Display Terminal. Table 1-2 describes the options that are available for the CX4111 Computer Display Terminal.

Table 1-1
4111 OPTIONS

Option	Description
2C	Additional 1024 kBytes of RAM memory
4A	United Kingdom keyboard with thumbwheels
4B	French keyboard with thumbwheels
4C	Swedish keyboard with thumbwheels
4F	Danish/Norwegian keyboard with thumbwheels
4G	German Keyboard with thumbwheels
4M	Mouse
4N	North American keyboard with Joydisk
4P	United Kingdom keyboard with Joydisk
4R	French keyboard with Joydisk
4S	Swedish keyboard with Joydisk
4T	Danish/Norwegian keyboard with Joydisk
4U	German keyboard with Joydisk
A1	220 Vac/16 A, 50 Hz, with Universal European power cord
A2	240 Vac/13 A, 50 Hz, with United Kingdom power cord
A3	240 Vac/10 A, 50 Hz, with Australian power cord
A4	240 Vac/15 A, 60 Hz, with North American power cord
A5	220 Vac/6 A, 50 Hz, with Swiss power cord

Table 1-2
CX4111 OPTIONS

Option	Description
2C	Additional 1024 kBytes of RAM memory
4A	United Kingdom CX keyboard with Joydisk
4B	French CX keyboard with Joydisk
4C	Swedish CX keyboard with Joydisk
4F	Danish/Norwegian CX keyboard with Joydisk
4G	German CX keyboard with Joydisk
4M	Mouse
A1	220 Vac/16 A, 50 Hz, with Universal European power cord
A2	240 Vac/13 A, 50 Hz, with United Kingdom power cord
A3	240 Vac/10 A, 50 Hz, with Australian power cord
A4	240 Vac/15 A, 60 Hz, with North American power cord
A5	220 Vac/6 A, 50 Hz, with Swiss power cord

ACCESSORIES

These accessories are listed in the mechanical parts list (Section 10) where part numbers are given for each item. Standard accessories are supplied with each terminal, and optional accessories may be ordered separately, and in addition to, standard accessories.

Standard Accessories

The following accessories are standard:

- 120 Vac/6 A, 60 Hz operation, with North American power cord
- RS-232-C cable
- *4111 Computer Display Terminal Operators Manual*
- *4110/4120 Series Reference Guide*
- *An Introduction to Computer Color Graphics*
- Function key overlays (package of 6 in rear of *Operators Manual*)
- Standard ASCII Keyboard (with thumbwheels)

Optional Accessories

The following accessories are optional:

- 4111 (ASCII) Keyboard (with Joydisk)
- RS-422 cable
- Function key overlays (package of 6)
- RS-422 Loopback Connector
- RS-232-C Loopback Connector
- Centronics Loopback Connector
- Joystick connector EMI filter
- Test graticule
- Extender card
- *4110/4120 Series Host Programmers Manual*
- *4110/4120 Series Command Reference Manual*
- *4111/CX4111 Computer Display Terminal Service Manual*
- *GMA302 19-inch Color Raster Monitor Service Manual*
- *119-2387-00 Display Module Service Manual*
- *119-1989-00/119-2315-00 Keyboards with Mouse Technical Data Manual*
- *119-1990-00/119-2307-00 CX Keyboards with Mouse Technical Data Manual*
- *4120 Series Serial Keyboard Service Manual*

Section 2

SPECIFICATION

DEFINITION OF TERMS

The following terms are used in these tables:

- *Characteristic*. A property of the product.
- *Performance Requirement*. Statements that define characteristics that are essential to the intended application of the product and are verifiable by following a customer-available procedure (refer to the topic "Functional Check" in Section 5).
- *Supplemental Information*. Statements that describe typical performance for characteristics of secondary importance that are not usually verified by procedures in the manual, or statements that further explain related performance requirements.

PERFORMANCE CONDITIONS

In order for these specifications to be achieved and to ensure proper performance, the following conditions must be met:

1. The terminal must be adjusted at an ambient temperature of 68° to 86° F (20° to 30° C).
2. The terminal must be operating in an environment as specified in Table 2-1, and as specified in Section 7, *Installation*.

3. A warm-up time of at least 20 minutes must precede operation.
4. The terminal power source must meet specified power requirements. See Section 5, *Checks and Adjustments*. The terminal is designed to be operated from a power source with its neutral line at or near ground potential. It is not intended for operation from two phases of a multiphase system.

The following tables contain specifications and characteristics for the terminal:

Table	Description
2-1	Environmental Conditions
2-2	Electrical Requirements
2-3	Installation Requirements
2-4	Graphics Characteristics
2-5	Character Sets
2-6	Low Voltage Power Supply Specifications

SPECIFICATION

Table 2-1
ENVIRONMENTAL CONDITIONS

Characteristic	Performance Requirement
Temperature	
Non-operating	–40°F to 149°F (–40°C to 65°C)
Operating	32°F to 104°F (0°C to + 40°C)
Humidity	
Non-operating	95% relative humidity maximum (non-condensing)
Operating	75% relative humidity maximum (non-condensing)
Altitude	
Non-operating	To 50,000' (15,240 m)
Operating	To 15,000' ^a (4572 m)
Vibration	
Non-operating	0.010" constant displacement 15 min. @ 10-40-10 Hz. (in 1 min. sweeps) 10 min. Dwell @ 37 Hz. No resonances below 40 Hz. Three mutually perpendicular axes
Shock	
Non-operating	20 g, 11 ms, half sine, both directions, three mutually perpendicular axes, 3 drops per direction (18 drops)
Electrostatic Immunity	5 KV to 15 KV — No interruption of normal operation 15 KV to 20 KV — No permanent damage (15 KV if discharged to mouse or joystick)

^a Maximum operating temperature decreases 1° for each 1000' above 5000'.

Table 2-2
ELECTRICAL REQUIREMENTS

Characteristic	Performance Requirement
Nominal Input Voltages:	
115 Vac	87 — 128 Vac
230 Vac	174 — 250 Vac
Maximum Input Power	334 W
Frequency Range	48 — 66 Hz
Video Output	60 Hz non-interlaced RGB video at RS-170 levels, sync combined with green

Table 2-3
INSTALLATION REQUIREMENTS^a

Characteristic	Supplemental Information
Heat Dissipation	1700 BTU/hour
Surge Current	90 A @ 220 Vac, 50 Hz
Cooling Clearance	Terminal has design details that prohibit blockage of vents when placed against a flat surface wall. DO NOT BLOCK VENTS
Acoustic Noise	48 db max
Weight	80 lbs
Dimensions	Width — 21.8 " (553.7 mm) Height — 16.9 " (429.3 mm) Depth — 22.3 " (566.4 mm) ^b

^a These specifications do not include the Keyboard.

^b Does not include COMM connector on back of CX4111.

Table 2-4
GRAPHICS CHARACTERISTICS

Characteristic	Performance Requirement
Screen Addressability	1024 horizontal by 768 vertical pixels
Virtual Coordinate Space	-2^{31} to $(2^{31}-1)$ for each axis
Zooming	An image filling the coordinate space can be condensed for viewing in 1024 by 768 points by zooming out
Graphics Command Syntax	Compatible with 4115/4125 style escape sequences
Line Types	Solid, dashed, erase, XOR
Graphics Primitives	Vectors, polygons, rectangles, text, curves, circular arcs, and call-segment
Colors Available	In graphics area, 16 colors displayed at one time from a palette of 4096 colors; in dialog area, 8 color pairs displayed at one time
Graphics Input	The thumbwheels (or optional joystick, Joydisk, or mouse) control the crosshair cursor

Table 2-5
CHARACTER SETS

Characteristic	Performance Requirement
Standard Characters	Full ASCII character set of 94 displayable characters; 128 displayable characters in Snoopy mode
Other Characters	United Kingdom Danish/Norwegian German French Swedish Supplementary Rulings ASCII Multilingual
Character Format	80 characters per line 132 characters per line, 48 lines; uses 7 × 9 dot matrix in an 8 × 16 character cell (with descenders) 160 characters per line ^a

^a The smallest character size (160 characters per line) is available only for compatibility purposes and is not recommended for new development. It is normal for this character size not to display as clearly (for example, you may not see the hole in the center of a lower case "e" character).

Table 2-6
LOW VOLTAGE POWER SUPPLY SPECIFICATIONS

Characteristic	Performance Requirement
+ 5.1 V secondary	
Accuracy	$\pm 1\%$ nom. V @ 11A load
Regulation	$\pm 3\%$ of nom. voltage
Rated full load current	13A
Minimum load current	2.0A
Short Circuit protection	Current limited to 40A Maximum
- 5.4 V secondary	
Accuracy	$\pm 1\%$ nom. V @ 4.3A load
Regulation	$\pm 5\%$ of nom. voltage
Rated full load current	4.7A
Minimum load current	0A
Short Circuit protection	Current foldback at 6.0A $\pm 0.5A$
+ 12 V secondary	
Accuracy	$\pm 10\%$ nom. V @ 1.0A load
Regulation	$\pm 20\%$ of nom. voltage
Rated full load current	1.5A
Minimum load current	0.10A
Short Circuit protection	Power supply will cycle if + 12V is shorted directly to ground
- 12 V secondary	
Accuracy	$\pm 10\%$ nom. V @ 0.50A load
Regulation	$\pm 20\%$ of nom. voltage
Rated full load current	1.0A
Minimum load current	0A
Short Circuit protection	Power supply will cycle if - 12V is shorted directly to ground

Section 3

OPERATING INFORMATION

INTRODUCTION

This section contains operating information of special interest to the service technician. For more detailed operating information, refer to the *4111 Computer Display Terminal Operators Manual* and the *CX4111 Computer Display Terminal Operators Supplement*.

CONTROLS, INDICATORS, AND CONNECTORS

Tables 3-1 through 3-3 list controls, indicators, and connectors for the terminals and their different keyboards. Refer to Figures 3-1 through 3-3 for specific locations. Table 3-4 lists predefined keys for the different keyboards (standard 4111 keyboard with thumbwheels, optional 4111 keyboard with Joydisk), and CX4111 keyboard with Joydisk).

Table 3-1

TERMINAL CONTROLS

Control	Use
POWER switch (front panel)	To turn on the power, push in and release.
RESET button (rear panel)	By itself, the RESET button resets the terminal to the same status as at power-up. When used with the SELF TEST button, it initiates a Self-test sequence.
SELF TEST button (rear panel)	The SELF TEST button does nothing by itself, but initiates the Self-test sequence when used with the RESET button. (Self-test is discussed later in this section.)
BRIGHTNESS control (front panel)	Controls the intensity of the display image. Turning the control clockwise increases the intensity of the white level (screen brightness); turning the control counter-clockwise decreases the intensity of the white level.
DEGAUSS button (front panel)	Activates a degaussing coil in the display, demagnetizing the CRT and chassis. (With use, the CRT and chassis build up a magnetic field, which causes the color and convergence to be non-uniform.)
CONTRAST control (front panel — 119-2387-00 Display Module only)	Controls the contrast of the display being viewed. Turning the control clockwise increases the grey-scale ratio between black and white; turning the control counter-clockwise decreases the ratio. The center-indent position is the recommended factory setting.
VOLTAGE CHANGE switches (rear panel)	Sets the terminal's operating line voltage (either 115 or 230 Vac).

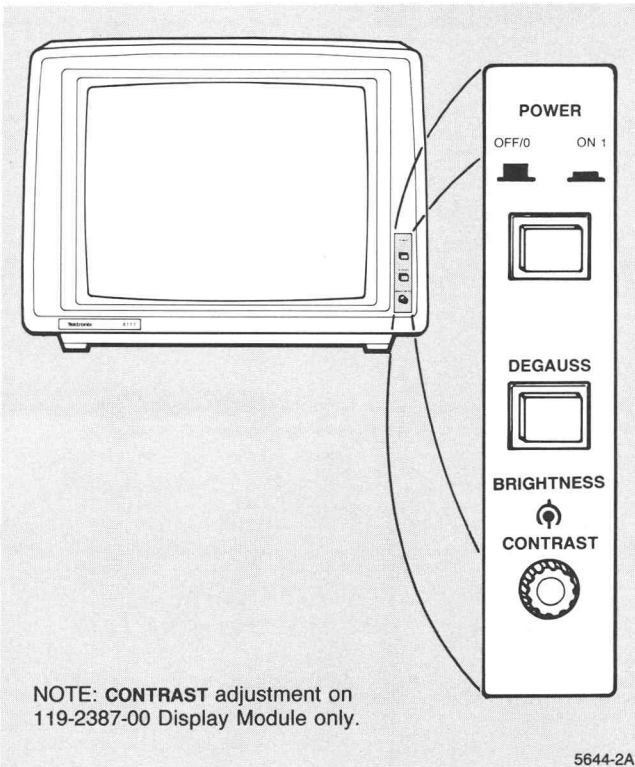


Figure 3-1. Controls and Indicators (Front).

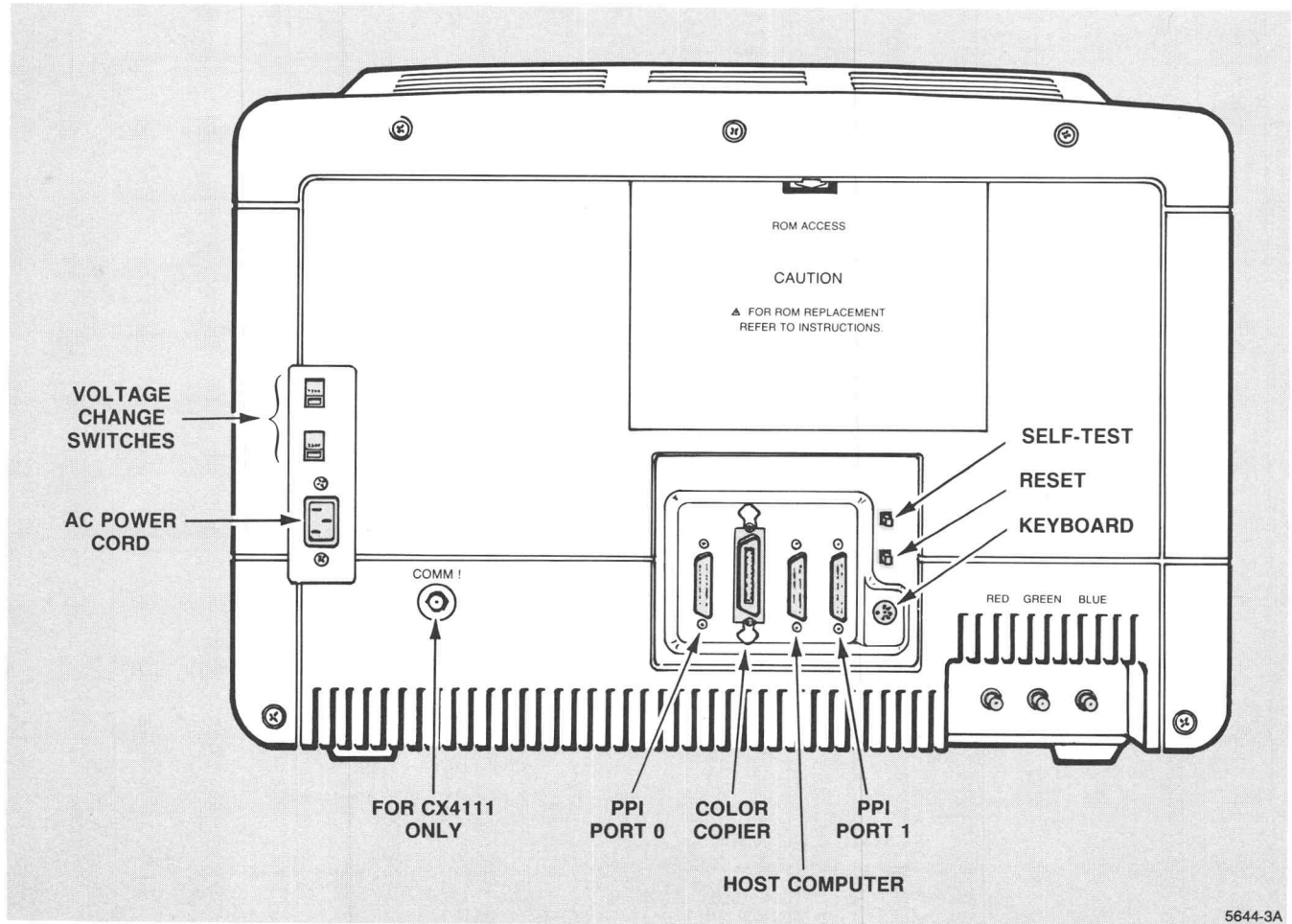
Table 3-2

TERMINAL AND KEYBOARD INDICATORS

Indicator	Meaning
POWER (front panel)	Shows status of POWER switch. A depressed switch indicates power is on. A switch fully extended indicates power is off.
KYBD LOCK ^a	Indicates the keyboard has been temporarily locked by the applications program. The locked state can be cleared by the program or by pressing one of the following: Cancel key, Break Key, or MASTER RESET switch.
PAGE FULL ^a	Awaiting operator action to make copy (Hard Copy key), clear screen (Page key), or allow overwriting (any other key except Shift).
XMT ^a	Shows data bits being transmitted to host computer.
RCV ^a	Shows data bits being received from host computer.
CAPS LOCK light ^b	Shows when the Caps Lock key has been pressed (to make alphabetic characters uppercase).

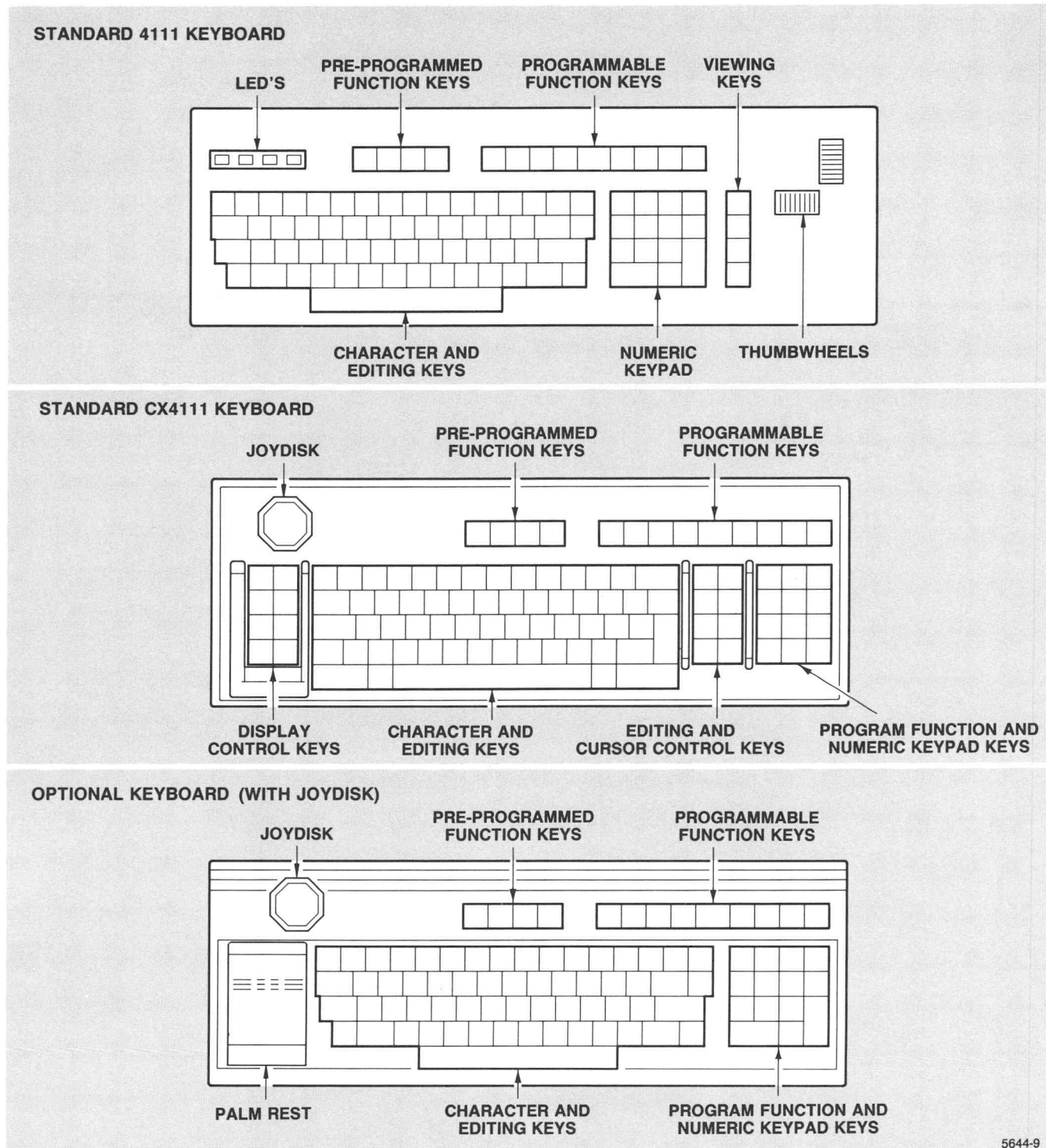
^a Standard 4111 keyboard with thumbwheels.

^b CX4111 and optional 4111 keyboards with Joydisk.



5644-3A

Figure 3-2. Controls, Indicators, and Connectors (Rear).



5644-9

Figure 3-3. The Three Keyboards.

Table 3-3

TERMINAL AND KEYBOARD CONNECTORS

Connector	Use
AC Power Cord	Accepts power cords from a standard power source. (The voltage rating of the source should match the setting of the VOLTAGE SELECTOR switches.)
COPIER	Provides a Centronics-style interface to TEKTRONIX 4691, 4692, or 4695 Color Graphics Copiers, and 4696 Color Ink-Jet Printers.
COMPUTER	Provides RS-232 connection to a host computer.
KEYBOARD	Connects the keyboard cable to the terminal.
PORT-0 and PORT-1	Provides standard RS-232-C communications to Tektronix peripheral devices such as the 4662/4663 Plotters and the 4957/4958 Graphics Tablets. Also provides RS-422 communication on Port-0
RED, GREEN, and BLUE video outputs	Provides red, green, and blue color signals to an external monitor or color hard copy device, such as a 35 mm slide camera.
COMM (for CX4111 only)	Provides coaxial cable connection to an IBM 3274 or 3276 Control Unit for connection to an IBM host computer.

Table 3-4

PREDEFINED KEYS

Key	Use
Dialog ^a	Toggles visibility of the Dialog buffer.
Clear ^a	Erases the Dialog buffer.
Setup	Toggles Setup mode on and off. In Setup mode, the terminal is ready to process English-like commands from the keyboard.
Local ^a	Toggles Local mode on and off. In Local mode, keyboard input is interpreted as if it came from the host, and host input is held in a queue. Setup mode has priority over Local mode.
Cancel	Cancels operations (except spooling), resets a number of modes, and flushes input/output queues.
Hard Copy ^a	Sends contents of the screen to a copier (if attached). (Since ordinarily, white on the screen prints as black on the copy, pressing SHIFT and HARD COPY simultaneously causes black on the screen to appear as black on the copy.)
Dialog/GEras ^b	Dialog turns the dialog area on or off. GEras (Shift Dialog) erases the graphics area.
SCopy/DCopy ^b	SCopy makes a copy of the screen. DCopy (Shift-SCopy) makes a copy of the dialog area.
Menu ^b	Accesses the Set Color and Zoom/Pan functions.
SEras/DEras ^b	SEras erases the entire screen. DEras (Shift-SEras) erases just the dialog area.

^a Only on 4111 keyboard with thumbwheels.^b Only on keyboards with Joydisk (CX4111 keyboard and optional 4111 keyboard).

NONVOLATILE MEMORY

INTRODUCTION

Non-volatile storage of certain operating parameters and values is accomplished by an Electrically Erasable Programmable Read-Only Memory (EEPROM) chip. Table 3-5 lists stored parameters in non-volatile memory.

PARAMETERS STORED IN NON-VOLATILE MEMORY

Table 3-5
STORED PARAMETERS

Function	Command Name	Factory Default	Purpose
General Terminal Operation	CRLF	NO	Sets or terminates "carriage return implies line feed."
	ECHO	NO	Sets local or remote echo.
	GAMODE	REPLACE	Determines if background of character is visible when text is displayed in graphics area.
	IGNOREDEL	NO	Specifies whether or not the ASCII delete character is ignored.
	KEYEXCHAR	DE	Specifies the key execute toggle character.
	LFCR	NO	Sets or terminates "line feed implies carriage return."
	PAGEFULL	NONE	Determines action to be taken when pagefull condition occurs.
Dialog Area Control	DABUFFER	48	Sets maximum size of dialog buffer in lines.
	DACHARS	132	Sets maximum number of characters per line in the dialog area.
	DAENABLE	NO	Specifies whether or not alpha text is sent to the dialog area.
	DAINDEX	1,0,0	Specifies the display colors in the dialog area.
	DA2INDEX	7	Sets color of special ANSI character representations (bold, underline, etc.).
	DALINES	5	Specifies the visible portion of the dialog buffer.
	DAMODE	REPLACE	Sets Overwrite or Replace mode in dialog area.
	DAPOSITION	0,0	Sets position of dialog area.
	DASURFACE	1	Sets dialog area surface.
	DAVIS	NO	Sets visibility of dialog area.
Graphic Input (GIN)	REOM	1	Determines use of end-of-message character for GIN mode.
Communication	BAUDRATE	2400,2400	Sets transmit and receive baud rates.
	BELLTYPE	CONTINUOUS	Sets bell to continuous or discrete (only for keyboards with Joydisk).
	BELLVOLUME	MEDIUM	Sets volume of the keyboard bell (only for keyboards with Joydisk).
	BREAKTIME	200	Defines length of break transmission in milliseconds.
	BYPASSCANCEL	LF	Sets bypass cancel character.
	EOFSTRING	' '	Defines end-of-file string.
	EOLSTRING	'CR'	Defines end-of-line string.
	EOMCHARS	CR LF	Defines end-of-message characters.
	FLAGGING	NONE	Specifies type of flagging performed.
	PARITY	NONE	Specifies kind of parity sent.
	PROMPTSTRING	' '	Specifies the prompt used when in Prompt mode.
	QUEUE SIZE	300	Sets the size of the input queue.
	STOPBITS	1	Specifies the number of stop bits used.
	XMTDELAY	100	Specifies the length of time to wait after receiving end-of-message character.
	XMTLIMIT	19200	Specifies maximum transmit rate.

continued

Table 3-5 (cont)
STORED PARAMETERS

Function	Command Name	Factory Default	Purpose
Communication (cont)	BCONTINUECHARS	& &	Specifies block-continue characters.
	BENDCHARS	\$ \$	Specifies end-of-block characters.
	BHEADERS	'HEADTX' 'HEADRX'	Specifies block-header sequences.
	BLENGTH	256 256	Specifies block length.
	BLINELENGTH	70	Specifies line length for Block mode transmission.
	BLOCKMODE	NO	Specifies whether or not the terminal is armed for Block mode.
	BMASTERCHARS	# #	Specifies master characters for Block mode.
	BNONXMTCHARS	'#\$&'#\$&'	Specifies nontransmittable characters for Block mode.
	BPACKING	7 6 7 6	Specifies manner in which blocks are packed.
	BTIMEOUT	0	Specifies the length of wait before retransmitting previous block of data.
Two Port Peripheral Interface (Both ports are the same on EEPROM reset.)	PASSIGN	PPORT	Assigns a device to a port.
	PBAUD	2400	Sets baud rate for a port.
	PBITS	1 8	Sets the stop and data bits for a port.
	PEOF	' '	Defines the end-of-file string for a port.
	PEOL	' '	Defines the end-of-line string for a port.
	PFLAG	NONE	Establishes the type of flagging for a port.
	PPARITY	NONE	Establishes the parity checking used on a port.
Color Copier Interfacing	HCDATARES	1	Sets either one or two-byte resolution for color hard copies.
	HCORIENT	HORIZONTAL	Sets image orientation on color hardcopy media.
CX4111 Commands	BASECOLOR	BASE	For CX4111, determines whether the terminal displays information in two or three colors; acts like the Base Color switch of the IBM 3279 terminal.
	CAPITALS	NO	For CX4111, selects display of uppercase-only text or both uppercase and lowercase; acts like Dual Case/Mono switch of IBM 3279 terminal.
	CLICK	NO	For CX4111, turns the key click on or off.
	HOSTPORT	COAX	For CX4111, selects the port (coax or RS232) to be used for host-to-terminal communications.
	TEKHEADER	112	For CX4111, specifies (by EBCDIC value) the header character that identifies Tek commands in the 3270 data stream.
	TMETHOD	1	For CX4111, specifies the method used to translate EBCDIC data to ASCII.

RESETTING NON-VOLATILE PARAMETERS

You can restore the terminal parameters to the factory defaults by using the following Self-test procedure:

1. Press and hold the SELF TEST button while pressing and releasing the RESET button.
2. When the bell sounds, type **Ctrl-C** within 20 seconds to call up the Adjustment Self-test menu.
3. Press F1. The Processor Board menu will appear on the screen.
4. Press Function Key 1 (F1). A confirmation message should appear on the screen.
5. Type **Ctrl-E**. This causes the terminal to exit from Self-test.

Because resetting the non-volatile memory disables the dialog area, you may want to enter Setup mode (press the Setup key) and type **DAENABLE YES**.

INQUIRY COMMANDS

The REPORT-TERMINAL-SETTINGS command can be used in Local mode to obtain firmware version information. Enter Local mode (Setup mode must be off), then type:

`^cIQ inquiry code`

where *inquiry code* consists of two characters. `^cIQ00` returns the version number of the firmware and `^cIQ99` returns the firmware level.

One can also inquire about memory size while the terminal is in Set-up. Press the Set-Up key and enter either *sta mem* or *sta pmem*.

- *Status Memory* — reports the amount of standard memory available (256K bytes or 16K blocks). The first number reported back is total memory available to the user (in Kbytes). The second number reported is the largest contiguous block of memory (in Kbytes).
- *Status Pmemory* — reports the amount of optional segment memory available. Option 2C provides 1.024M bytes (65K blocks) of memory in four 256K byte pages of 16K blocks each. The first number reported back is total memory available to the user (in blocks of 16 bytes each). The second number reported is the largest contiguous block of memory (in blocks).

THE SELF-TEST DIAGNOSTIC PROGRAM

INTRODUCTION

The Self-test diagnostic program is the primary troubleshooting aid. This program resides in firmware and checks most of the circuitry in the system unit and display. There are four diagnostic and one adjustment Self-test programs:

- The Power Up Self-test sequence is a subset of the Extended Self-test program and is executed automatically when power is turned on or the system is reset. The power up sequence performs only as much of the full Self-test program as is necessary to determine that the processor circuitry is functional.
- The Extended Self-test program, referred to in this text as simply Self-test, must be initiated manually. Because these tests check the circuits more extensively, they take several minutes to run. In certain cases, a bad component or memory address can be pinpointed.
- The Adjustment Self-test program is a portion of Self-test that is oriented toward adjustments and specific, repeatable tests of certain components or circuits. The Adjustment Self-test can also be used to restore EEPROM factory default parameters. Detailed information is given under “Adjustment Self-test” later in this section.
- The Cycle Self-test program runs the entire Self-test program in a continuous loop for factory instrument cycle room testing.
- The DIACON Diagnostic tests are a superset of Self-test that require additional ROMs for use; refer to the *4111 DIACON Test Fixture Users Manual* for details.

In general, Self-test does not rely on any portion of the hardware until it has been tested. Once a test has been completed, however, that hardware can be used to test other hardware.

Keyboard

The keyboard contains its own Self-test program that runs automatically upon each power-up or reset.

Options

The RAM Option board is the only option automatically checked in the terminal hardware during the Power Up Self-test program.

TEST AND ERROR MESSAGES

Errors are reported in the following ways:

- Terminal screen messages
- Board-in-error LEDs on the Terminal Control and RAM Option boards
- The CAPS LOCK LED on the keyboard
- The keyboard bell

The terminal screen and host port error reports are English-language messages giving the test description and hexadecimal codes for specific tests and subtests. The hexadecimal codes are given in the error message descriptions in Section 6 of this manual.

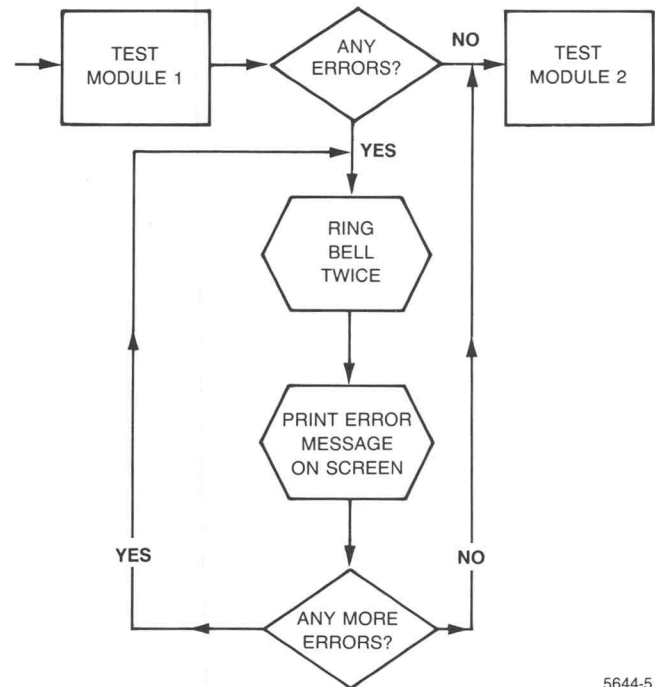
The board-in-error LEDs indicate the pass/fail status of each board. The LED is lit while the corresponding board is under test and remains lit if a failure occurs.

NOTE

The CX Interface board has an LED that is green. It blinks when the CX Interface board is in CUT (Control Unit Terminal) mode. During Self-test, the green LED goes through a sequence of blinking dimly and brightly.

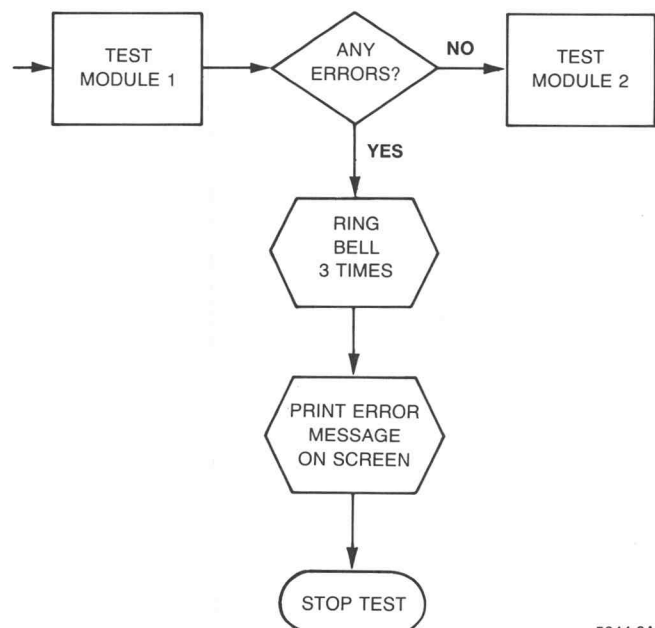
The CAPS LOCK LED remains lit if an error occurs. The keyboard bell rings twice if a non-fatal error occurs, and three times if a fatal error occurs.

Two types of errors can occur: fatal and non-fatal. A problem causing fatal error will halt Self-test and must be corrected for testing to continue. A non-fatal error will be recorded, but will not halt the testing of other areas of the terminal. (When the bell rings, the operator must press the Space Bar to continue Self-test if a non-fatal error occurs.) Figure 3-4 and 3-5 show the program sequence for reporting both types of errors.



5644-5

Figure 3-4. Non-fatal Error Flow Chart.



5644-6A

Figure 3-5. Fatal Error Flow Chart.

Error Codes

The error codes are given in Section 6 of this manual.

ENTERING SELF-TEST

Begin Self-test as follows:

1. Press and hold the SELF TEST button while pressing and releasing the RESET button.
2. When the LEDs begin to light, release the SELF TEST button.

The first test (keyboard LED check) begins by lighting the keyboard LEDs, then finishes by turning them off. (For keyboards with a Joydisk, only the Caps Lock LED is lit). If an error occurs at this point, the Self-test program does not stop but continues with the keyboard test. A non-working LED is usually a keyboard problem.

3. When the keyboard bell sounds once, the test should halt and wait 20 seconds for a keystroke. Perform one of the following to continue Self-test execution:
 - Press **Ctrl-D** to skip the Delay Memory Check, which can require six or more minutes to execute, depending on the amount of RAM memory installed in the terminal.
 - Press **Ctrl-C** to enter the Adjustment Self-test program, which is described separately.
 - Press any other key to continue immediately. (The entire Self-test, including the Delay Memory Check, will execute.)
 - Wait for Self-test to "time out" (20 seconds). If the test proceeds without halting, spurious keystrokes are being generated. This problem could be caused by dirt or corrosion in the keyboard or a poor connection in the keyboard cable.

If an error occurs, refer to the error code listings in Section 6.

ADJUSTMENT SELF-TEST

INTRODUCTION

The Self-test adjustment program allows you to adjust the terminal and use aids such as loopback connectors during troubleshooting. Some of the things that the Adjustment Self-test program can do are:

- Generate patterns to be used for convergence adjustments.
- Reset the EEPROM parameters.
- Display the character or name of each keyboard keystroke.
- Perform a Host Port check (this requires attaching a loopback connector).
- Do a Full-Loopback test of the CX Interface board.

STARTING ADJUSTMENT SELF-TEST

To enter the Adjustment Self-test program:

1. Press and hold SELF TEST while momentarily pressing RESET.
2. After the bell sounds, release SELF TEST.
3. When the keyboard bell sounds, press **Ctrl-C**. The Adjustment Self-test menu will be displayed after a short pause.
4. When the menu appears, select a procedure and press the corresponding function key ("fn" designates a function key, while "Sh" means to press Shift and the function key at the same time). A menu for that procedure will appear.

The Adjustment Self-test Menu

```

4111 Menu
--
f1 4111 Processor Board
f2 4111 Display
f3 4111 Coax Board
--
Selection
Function Key-Test Selection
^C 4111 Menu
^D Current Menu
^E End
*
```

In addition to function-key selections, the following commands are available at any time:

- Ctrl-C — returns to the general menu.
- Ctrl-D — returns to the current subordinate menu.
- Ctrl-E — exits Self-test and returns to normal operation.

Pressing an illegal key (one not defined by the menu) can have one of two possible effects:

- If the menu is displayed, pressing an illegal key prints the “?Illegal Selection” message.
- If a particular test within a menu is being run, pressing an illegal key causes either the current menu to be displayed or no response from the terminal.

The Display Menu

The Display menu contains routines to assist in checks and adjustments:

```

4111 Display Menu
--
f1 Grid
f2 White Screen
f3 Gray Scale
f4 Color Scale
f5 Dots
f6 Character Fonts
f7 Screen of H
f8 Visibility Mask
Sh f1 Crosshairs
--
Selection
Function Key-Test Selection
^C-4111 Menu
^D-Current Menu
^E-End
*
```

Pressing F1 through F6 results in displaying patterns to check or adjust the display:

- Grid (graticule pattern) — for adjusting horizontal/vertical aspects of the display and convergence.
- Dots and Screen of H — for adjusting focus.
- Gray Scale and Color Scale — for verifying operation.
- White Screen — for purity check.

For details, refer to either the *GMA 302 Display Module Service Manual* or to the *119-2387-00 Display Module Service Manual*.

When you select the Grid, Gray Scale, Color Scale, or Dots menus, the following keys are redefined:

- Dialog — Toggles the red gun.
- Setup — Toggles the green gun.
- Local — Toggles the blue gun.

LEDs in the keys indicate that the corresponding gun is turned on. By using these keys in combination, each pattern can be examined in eight different colors.

The Processor Board Menu

The Processor Board menu:

```

Processor Board Menu
--
f1 Non-volatile Parameters Reset
f2 Keyboard
f3 Host Port
f4 PPI Port 0
f5 PPI Port 1
f6 DMA Loopback
f7 Hard Copy Loopback
f8 Hard Copy Print
Sh f1 495X Tablet
Sh f2 Factory Cycle Mode
--
Selection
Function Key-Selection
^C-4111 Menu
^D-Current Menu
^E-End
*
```

NOTE

Resetting of the non-volatile memory is described earlier in this section.

Keyboard Test. Pressing the F2 key to run the keyboard test is useful in isolating keyboard and Terminal Control board interface problems. The test displays on the terminal screen the equivalent key-press and key-release codes for each key on the keyboard.

Therefore, every key on the keyboard displays two double-digit numbers. These numbers represent the 8-bit codes that the keyboard generates for each downstroke (key-press) and the upstroke (key-release) of a specific key. Figures 3-6, 3-7, and 3-8 illustrate the key-press codes for the three different keyboards; the standard 4111 keyboard with thumbwheels, the optional 4111 keyboard with a Joydisk, and the CX4111 keyboard with a Joydisk. In addition, thumbwheel, optional joystick, and optional mouse responses are shown for the 4111 standard keyboard. Joydisk responses are shown for the keyboards with a Joydisk.

EXAMPLES:

THUMBWHEELS
ROTATED UP: TW - 

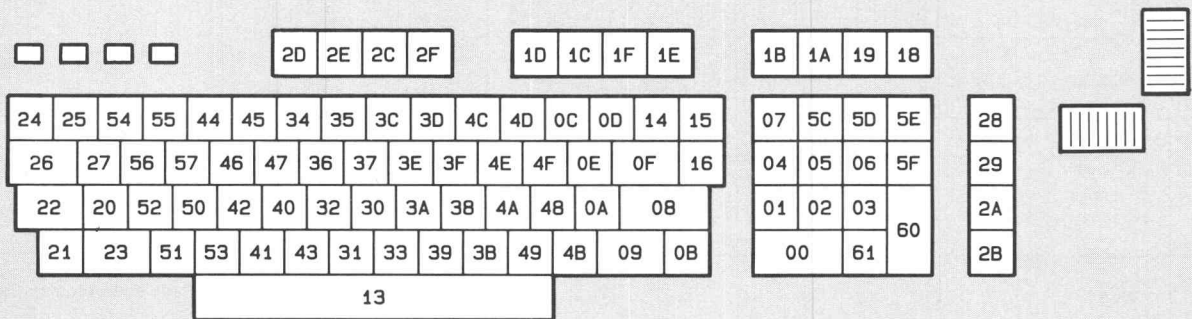
THUMBWHEELS
ROTATED DOWN: TW - 

THUMBWHEELS
ROTATED RIGHT: TW - 

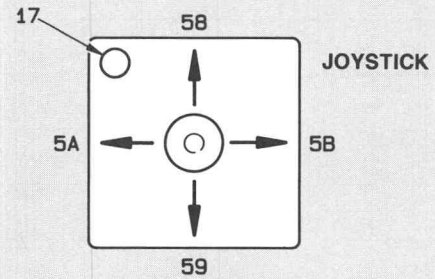
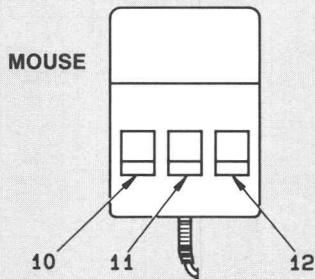
THUMBWHEELS
ROTATED LEFT: TW - 

FUNCTION KEYS

		F1	F2	F3	F4	F5	F6	F7	F8	DIALOG	SET-UP	LOCAL	HARD COPY
		1D 9D	1C 9C	1F 9F	1E 9E	1B 9B	1A 9A	19 99	18 98	2D AD	2E AE	2C AC	2F AF
		↑	↑										
		DOWN-STROKE	RELEASE-STROKE										



KEYBOARD



NOTE: Release code = press code + 80 (Hex)

5644-78

Figure 3-6. Standard Keyboard (with Thumbwheels) Key-Press and Key-Release Codes.

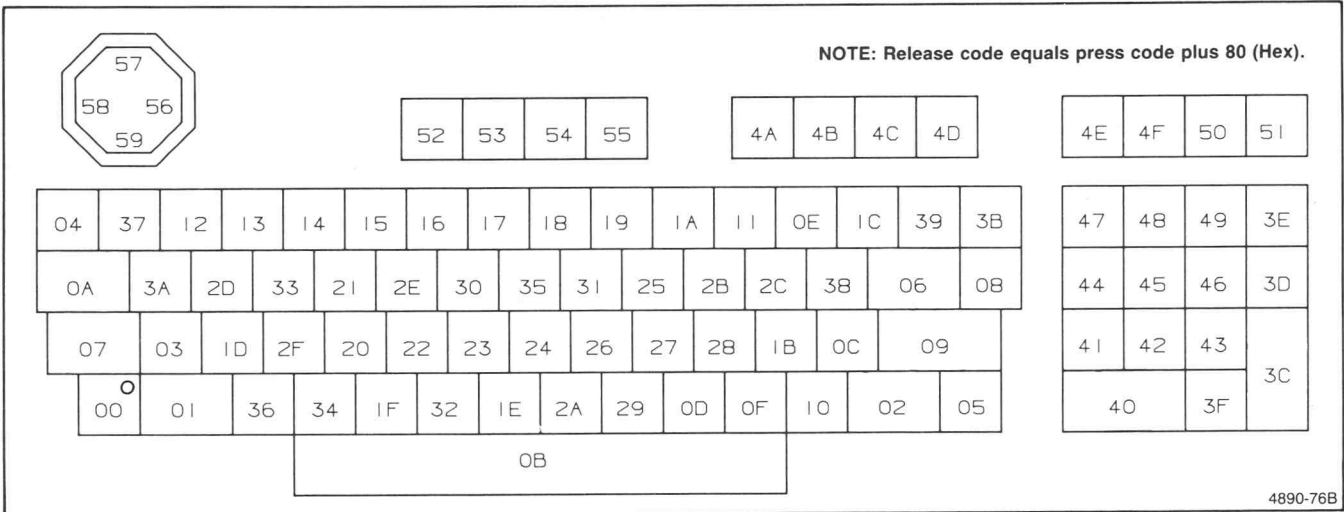


Figure 3-7. Optional Keyboard (with Joydisk) Key-Press and Key-Release Codes.

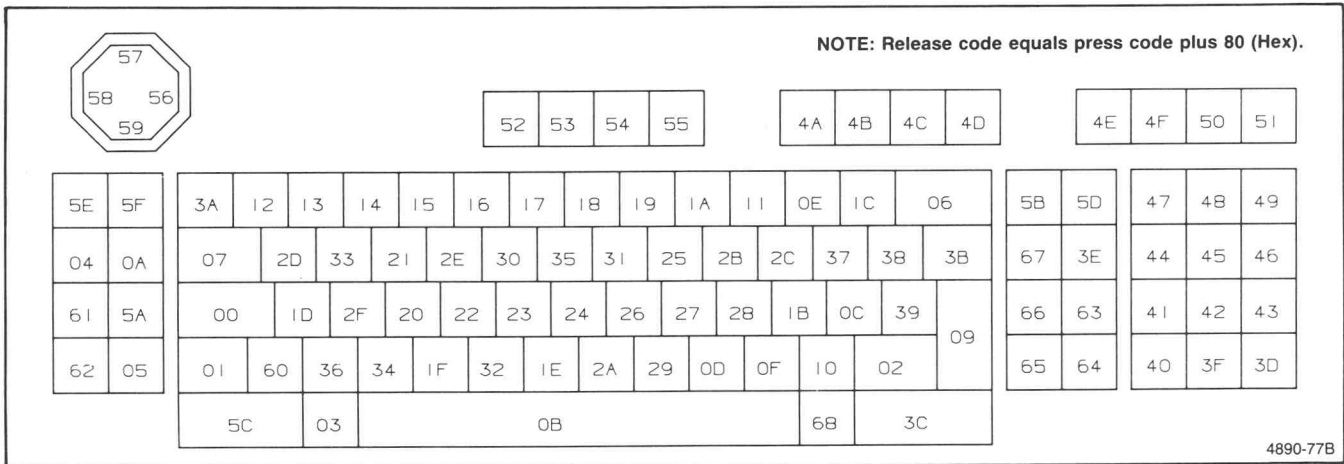


Figure 3-8. CX Keyboard (with Joydisk) Key-Press and Key-Release Codes.

The CX Interface (Coax) Board Test

NOTE

The CX Interface board has two modes of Self-test:

Mini-Loopback, where the coax receiver and transceiver have a TTL loopback connection (for example, nothing is sent out on the coax). This test occurs during the Power Up portion of Self-test.

Full-Loopback, where the coax receiver and transmitter are mutually coupled via the coax circuitry. In this mode, a diagnostics bit pattern is sent out the coax connector. The user should check that the terminal is disconnected from the IBM 3274 Controller. Otherwise, the test could confuse the Controller if still connected to the terminal. This test occurs during the Adjustment portion of Self-test.

If a user selects "f3 4111 Coax Board" from the Adjustment Self-test menu, the following message will appear:

```
4111 Coax Board Menu
--
f1 Coax Board Test
--
Selection
Function Key-Test Selection
^C 4111 Menu
^D Current Menu
^E End
*
```

Press f1 to continue the test on the CX Interface board.

If the terminal does not have a CX Interface board installed, the following prompt will appear:

Coax Option Not Present

Coax Self Test Complete
Press Space Bar To Continue

If the terminal has a CX Interface, the Coax Board test recognizes it and displays the following prompt:

Coax Board Test
Disconnect Coax Cable...
Press Space Bar To Continue

Upon a successful completion of the 4111 Coax Board test, the following message appears:

Coax Board Test Complete
Press Space Bar To Continue

Pressing the Space Bar will display the original Adjustment Self-test menu.

If an error occurs during the 4111 Coax Board test, the error code will be displayed in the normal 4111 error code format. See Self-Test Error Messages in Section 6, *Maintenance* for specific error codes.

Section 4

THEORY OF OPERATION

INTRODUCTION

This section first introduces the terminals as a whole, and then lists the major circuit boards and modules. It then presents an overview and theory of operation for each circuit board and module in the terminal.

This theory write-up requires that the reader be generally knowledgeable about basic digital design. Certain abbreviations and acronyms have found their way into common use in the industry. Such terminology is used (sparingly) because most digital-service technicians are aware of these terms.

Since many people assimilate and retain pictorial information more readily than text information, this section includes many illustrations and diagrams. The block diagrams present conceptual information, while the timing diagrams emphasize operating characteristics.

PRODUCT OVERVIEW

The 4111 and CX4111 computer display terminals present alphanumeric and graphics data in color. They can be used for text editing, graphics display, and other general purpose input/output. The terminal's firmware decodes commands entered by the operator or sent by a host computer. The Programmer's Reference manual describes the range of firmware-related features. This theory discussion focuses on the hardware aspects of the terminal and only describes the firmware features needed for troubleshooting. The terminal contains a Self-test routine in ROM that is the principal diagnostic tool for fault isolation.

The standard 4111 terminal communicates with its host¹ via an RS-232-C data path. The host interface hardware is part of the Terminal Control board.

The CX4111 terminal replaces an IBM-3279 terminal and contains both an RS-232 host port and an IBM host port. (To switch host ports, the user types the command HOSTPORT COAX or HOSTPORT RS-232.) When talking to an IBM host, the terminal's CX Interface board interacts between the Terminal Control board and an IBM 3270-type Control Unit. The Control Unit then connects to the host mainframe. The terminal uses a coax cable to connect to the Control Unit.

The CX4111 also has a unique keyboard that emulates the 3279 while providing extra programmable function keys and the Joydisk. While in HOSTPORT COAX and connected to the host, the Operator Information Area (system status line) appears across the bottom of the display screen.

¹ Non-IBM host.

CIRCUIT BOARDS AND MODULES

The following circuit boards and modules are described in this section:

- Display Module — There are two different versions of the Display Module; these are referred to in this manual as the “early version” for the GMA302 Display Monitor, and as the “later version” for the 119-2387-00 Display Module.
- Display Control Board — There are two different versions of the Display Control board; these are referred to in this manual as the “early version” for the 670-8524-nn board, and as the “later version” for the 670-9725-nn board.
- Cursor Board — This board works only with the early version Display Control board. The Cursor board’s circuitry was then included on the later version Display Control board.
- Video Converter Board (used only with GMA302)
- Terminal Control Board
- RAM Option Board
- CX Interface Board — Used only with the CX4111.
- Keyboard — There are three different keyboards available; the standard keyboard with thumbwheels, the optional keyboard with Joydisk (119-2315-00), and the CX Keyboard with Joydisk (119-2307-00).
- Terminal Low Voltage Power Supply (TLVPS)

Each of the two display modules, the three keyboards, and the CX Interface board has its own separate service manual that includes circuit theory and schematics.

CIRCUIT OVERVIEW

This section divides the 4111 circuitry into the following three classifications:

- The Display circuitry (converts analog signals to a visible display on the crt screen) which may be one of the following:
 - GMA302 Display Module
 - 119-2387-00 Display Module
- The Display Control circuitry (converts digital data to analog signals) which includes the following:
 - Display Control Board
 - Cursor Board (used only with 670-8524-nn Display Control board)
 - Video Converter Board (used only with GMA302 Display Module)
- The Terminal Control circuitry (processes digital data and communicates I/O data) which includes the following:
 - Terminal Control Board
 - RAM Option Board
 - CX Interface Board (for CX4111 only)
 - Keyboard
 - Low Voltage Power Supply

The three systems perform their relative functions at different rates:

- The Display circuitry is *time-driven* — it refreshes the screen constantly at a frame rate of 60 Hz.
- The Display Control circuitry is both *command* and *time-driven* — it responds to the Terminal Control circuitry as necessary, but also controls the screen refresh operation performed by the Display circuitry.
- The Terminal Control circuitry is *command-driven* — it responds when the operator, the host computer, or a peripheral device demands attention.

Figures 4-1 and 4-2 show the relationship of the three systems and their component modules to each other and to external devices.

The following discussions begin with the visible image on the screen (produced by the Display circuitry) and trace the operation back through the Display Control circuitry and the Terminal Control circuitry to show how the image is formed.

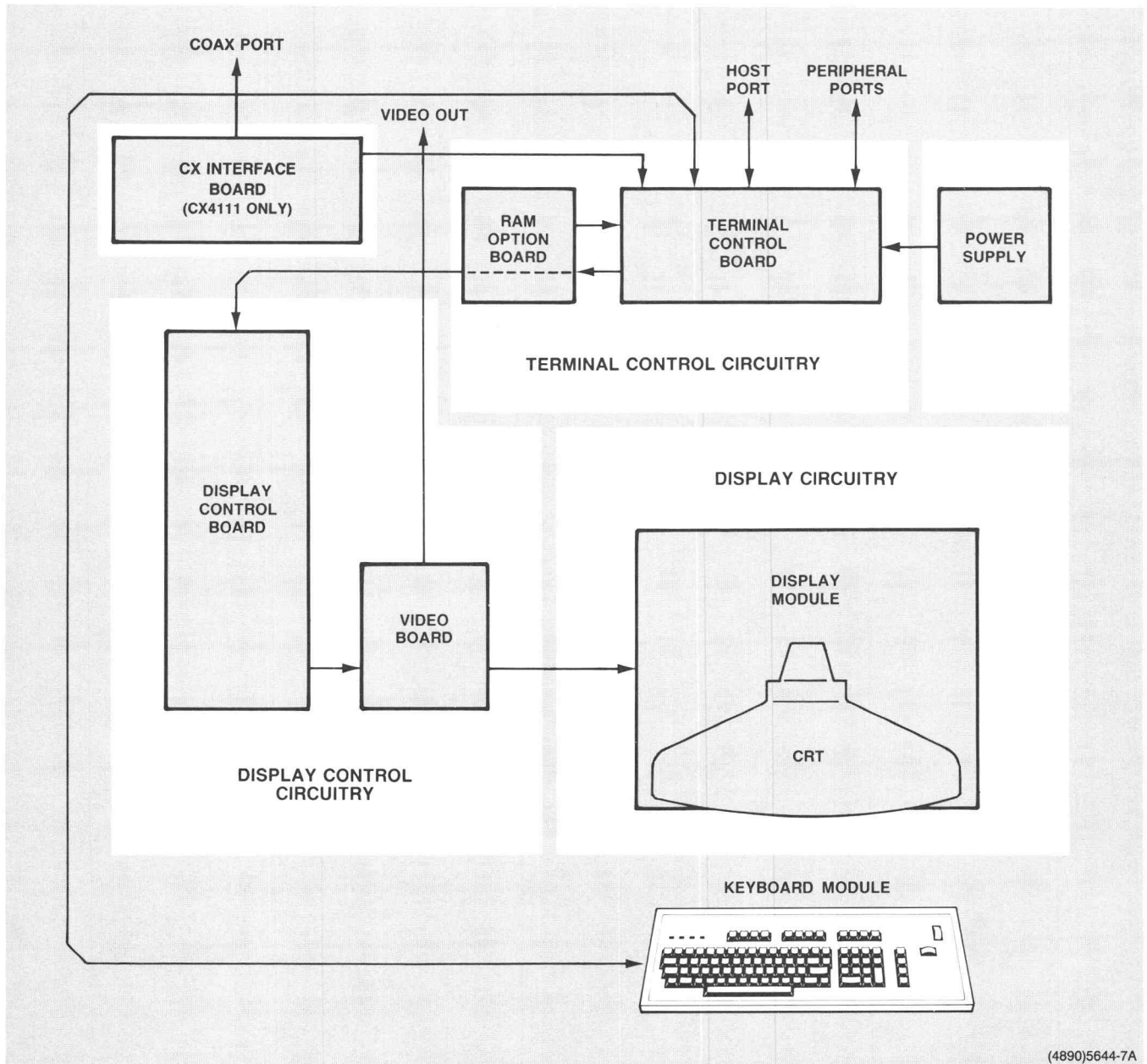


Figure 4-1. 4111/CX4111 Block Diagram.

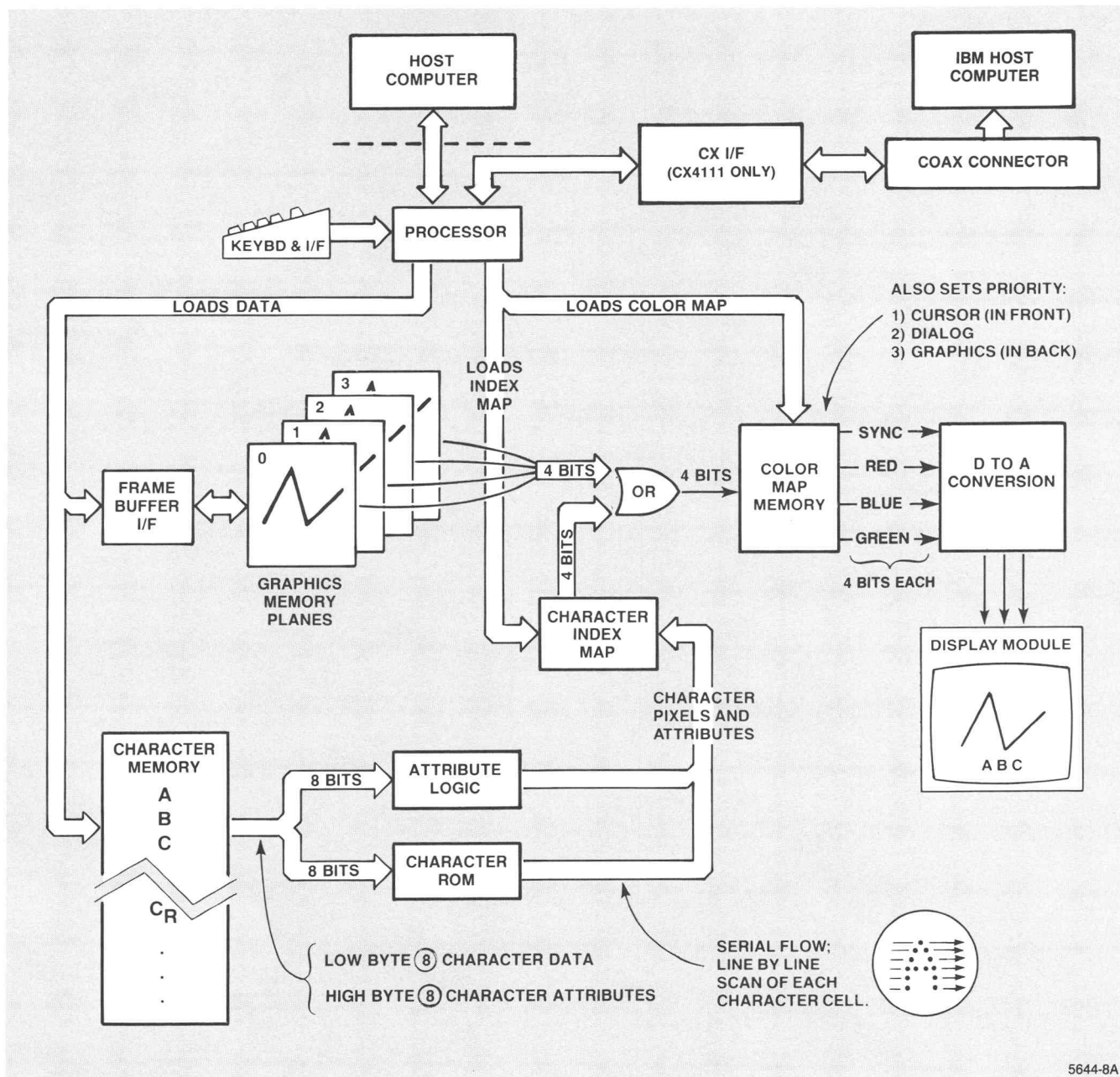


Figure 4-2. 4111/CX4111 Functional Diagram.

DISPLAY CIRCUITRY

INTRODUCTION

The Display circuitry creates the visible image on the crt from analog input signals (these include red, green, and blue with sync on green).

DISPLAY CIRCUITRY OVERVIEW

When you look at a raster display, your eyes blend the *pixels* and give the illusion of a continuous form. The word "*pixel*" (derived from the term "picture element") describes the smallest element of the screen that can be addressed. As an example, pixels arranged as in Figure 4-3 give the illusion of a straight diagonal line. The circuitry illuminates each pixel as a uniform color.

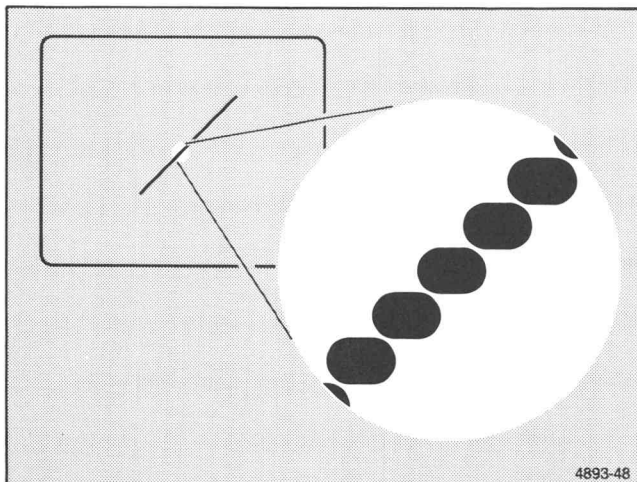


Figure 4-3. Magnified View of Pixels in a Line.

The crt gun emits electron beams that illuminate the red, green, and blue color dots. Your eye blends the color and intensity of the three dots into a single colored pixel, then blends the pixels into the final overall picture.

As the electron beam scans the screen, the Display circuitry adjusts the intensities of the three beams for each pixel to the proper color and brightness determined by the Display Control circuitry. The displays have 768 horizontal rows of 1024 pixels each. Their refresh rate is 60 Hz, and with the persistence of the crt, give the illusion of a continuously illuminated screen.

DISPLAY CIRCUITRY DESCRIPTION

For detailed display theory and service information, refer to either the *GMA 302 Display Monitor Service Manual* or the *119-2387-00 Display Module Technical Data Manual*.

DISPLAY CONTROL CIRCUITRY

The Display Control circuitry will be described in three levels; as an introduction, as a circuit overview, and as specific theory for each of the two versions of the Display Control board. The circuit description for the early version board (670-8524-nn) will refer to the 13 schematics for that board. The description of the later version Display Control board (670-9725-nn) will refer to the 26 schematics for that board.

The 670-9725-nn circuitry resembles the early version board (670-8524-nn) with the following exceptions:

- The re-layout of the 670-9725-nn version Display Control board changed almost all of the integrated circuit (IC) component numbers. But most of the ICs stayed the same in circuit function as the earlier 670-8524-nn board.
- Circuit blocks are drawn on the 26 schematics for the 670-9725-nn board.
- The 670-9725-nn schematics include the circuitry from the older Cursor board (used with the 670-8524-nn boards).

CIRCUIT INTRODUCTION

The Display Control circuitry serves as a buffer between the Terminal Control circuitry and the Display Module. This circuitry stores images in buffers in digital form, continually converts the stored display image to analog signals that drive the display, interacts with the Terminal Control circuitry on demand, and generates the horizontal and vertical sync signals that control the display.

To reduce the load on the system processor, separate Vector Generator circuitry handles the generation of the visible graphics display. The system processor generates a *display list*, which is an internal code for the display desired; the Vector Generator circuitry processes and executes this list. A *microcode* instruction set, resident in the Vector Generator circuitry, accomplishes the necessary tasks. Refer to Figure 4-4 for a simplified block diagram of a color raster display system.

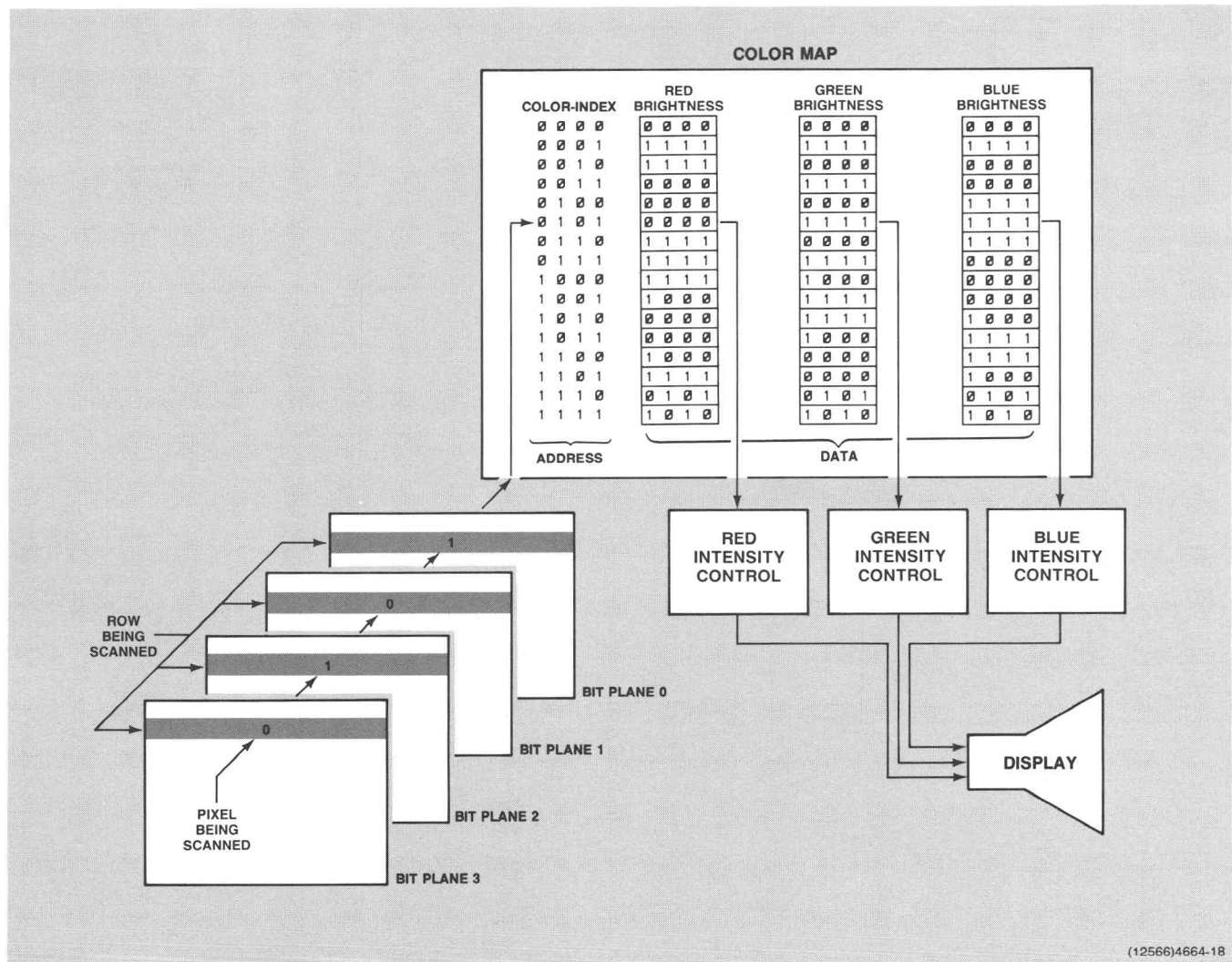


Figure 4-4. Block Diagram of a Color Raster System.

DISPLAY CONTROL CIRCUITRY OVERVIEW

Frame Buffer

The *frame buffer* consists of a memory area containing binary data that corresponds to the pixels on the screen. This data determines whether the pixel is to be turned on or off. The frame buffer stores the data for the graphics and *stroke characters*. (*Stroke characters* are alphanumeric characters created by combining short vectors, as opposed to *dot-matrix characters* that are composed of patterns of dots.)

You can visualize the frame buffer as a three-dimensional array of memory cells. The height and width of this array correspond to the pixel dimensions of the display screen. The depth of the display screen is expressed in the number of *bit planes*. The discussion of the use of the color map, which follows this discussion, shows how you can use groups of bit planes. Figure 4-5 shows how pixels correspond to the frame buffer.

The Terminal Control circuitry communicates with the frame buffer via a frame buffer interface. Any changes to the contents of the frame buffer are written by the frame buffer interface, under the direct control of the Terminal Control circuitry.

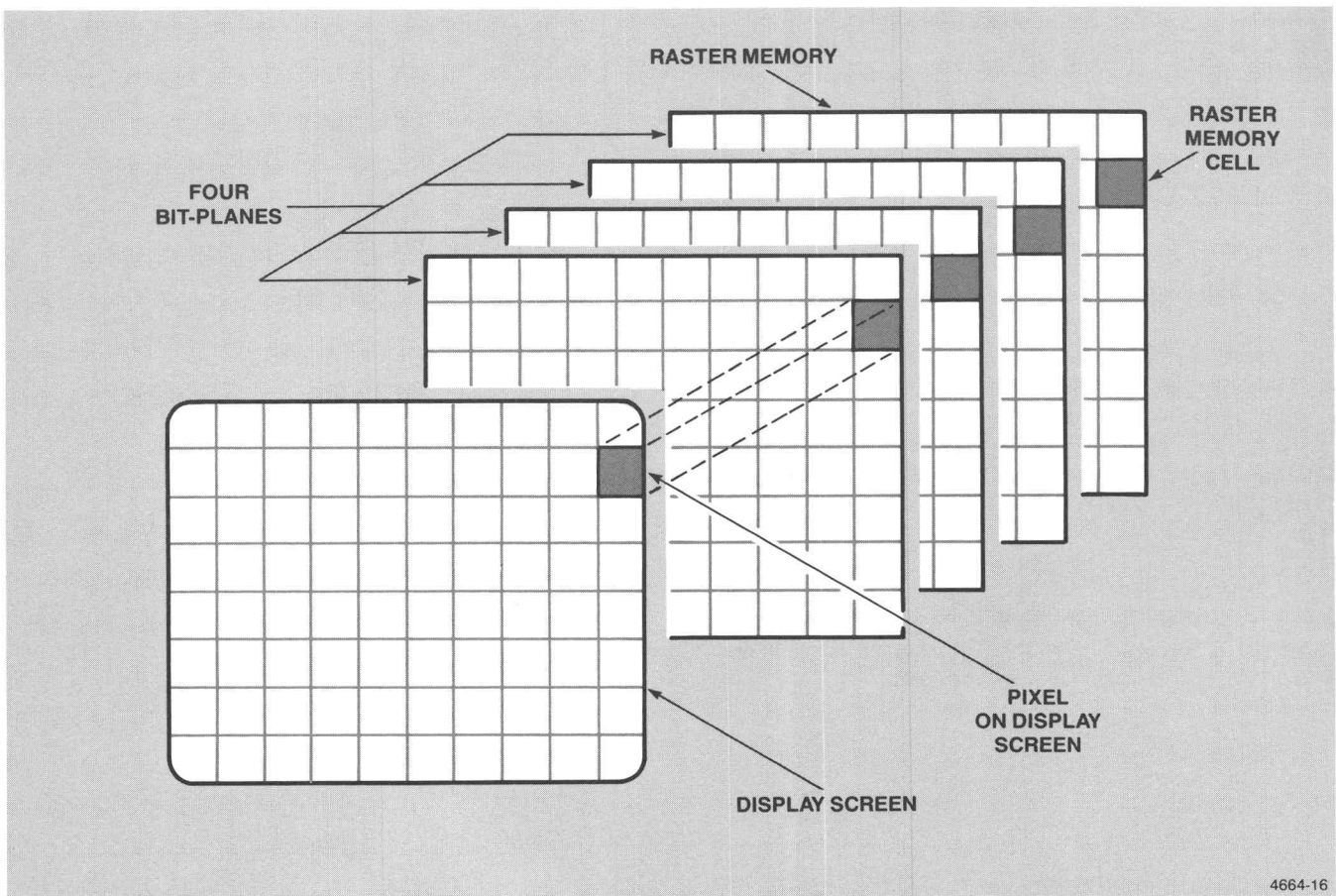


Figure 4-5. Pixels and the Frame Buffer Memory.

THEORY OF OPERATION

The Color Map. As the Display Control circuitry scans the frame buffer, it reads the data stored in each memory location and uses the value as an index into a table called the *color map*. The values stored in the color map are converted to signals that drive the intensities of the electron gun beams in the Display Module. As previously explained, the intensity of the electron gun beams determine the brightness and color of the corresponding pixel on the display screen. Thus, the pixel is a visual copy of the contents of that portion of the frame buffer.

The color map uses a relatively small number of indices (up to 16) to indicate a large number of colors (up to 4096). The color map default values can be changed by the user.

The binary number stored for each pixel in the frame buffer is called a *color index* — an index to the color map. The color map has entries corresponding to the color indices and causes the Display circuitry to produce the proper color mix for each pixel.

The user can change the image on the screen by changing the contents of the frame buffer memory, the color map, or both.

Dialog Area and Cursors

The *dialog area* is a portion of the screen temporarily overlaying the graphics area for the purpose of viewing instructions or text (Figure 4-6). Background color, character color, and size of the dialog area can be controlled by the operator or the host computer. Overlay circuitry handles the dialog functions through the *index map*.

The *index map* is similar to the color map, but is smaller and is used exclusively for non-graphics information. Dot-matrix character, dialog area, and cursor information is combined with graphics information by the *index map*.

The dot-matrix characters are resident in the system firmware, and can be used in both the dialog area and in graphics. Stroke characters, being created from graphics vectors, can only be used as graphics.

Overlay circuitry handles the dialog characters and cursor information in separate RAM memory. The cursor information is separate from the graphics information until output from the index map.

The dialog (or alpha) cursor is separate from the GIN (or graphics) cursors. The standard graphics cursor is crosshairs, but can be redefined as required.

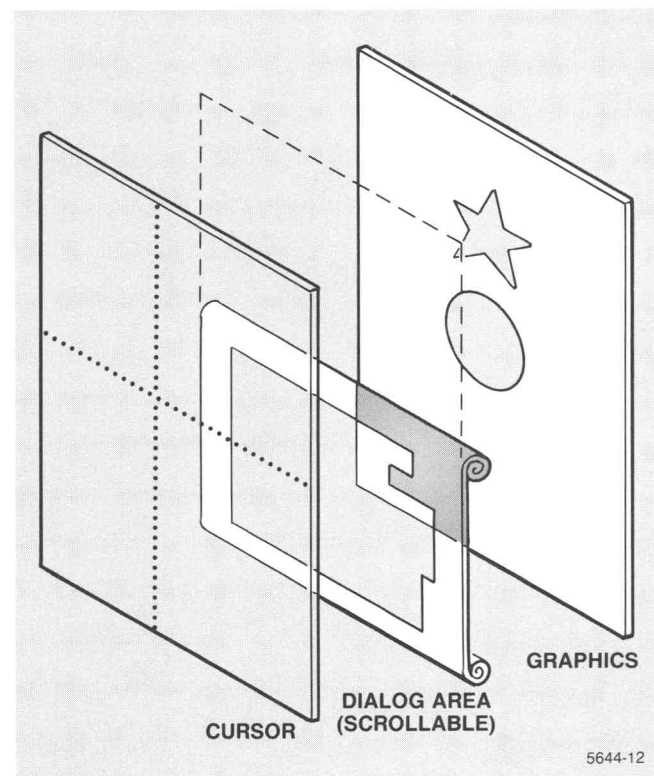


Figure 4-6. Graphics and Dialog Areas.

DISPLAY CONTROL BOARD CIRCUIT DESCRIPTION (670-8524-NN)

Figure 4-7 shows the general configuration and operation of the Display Control board.

Introduction

The earlier version Display Control board circuitry can be divided into 50 functional blocks. The following text explains the circuitry and operation of each block. Refer to the schematic diagrams (referenced in the descriptions) and the Display Control board timing diagrams in Section 10 of this manual while reading the descriptions.

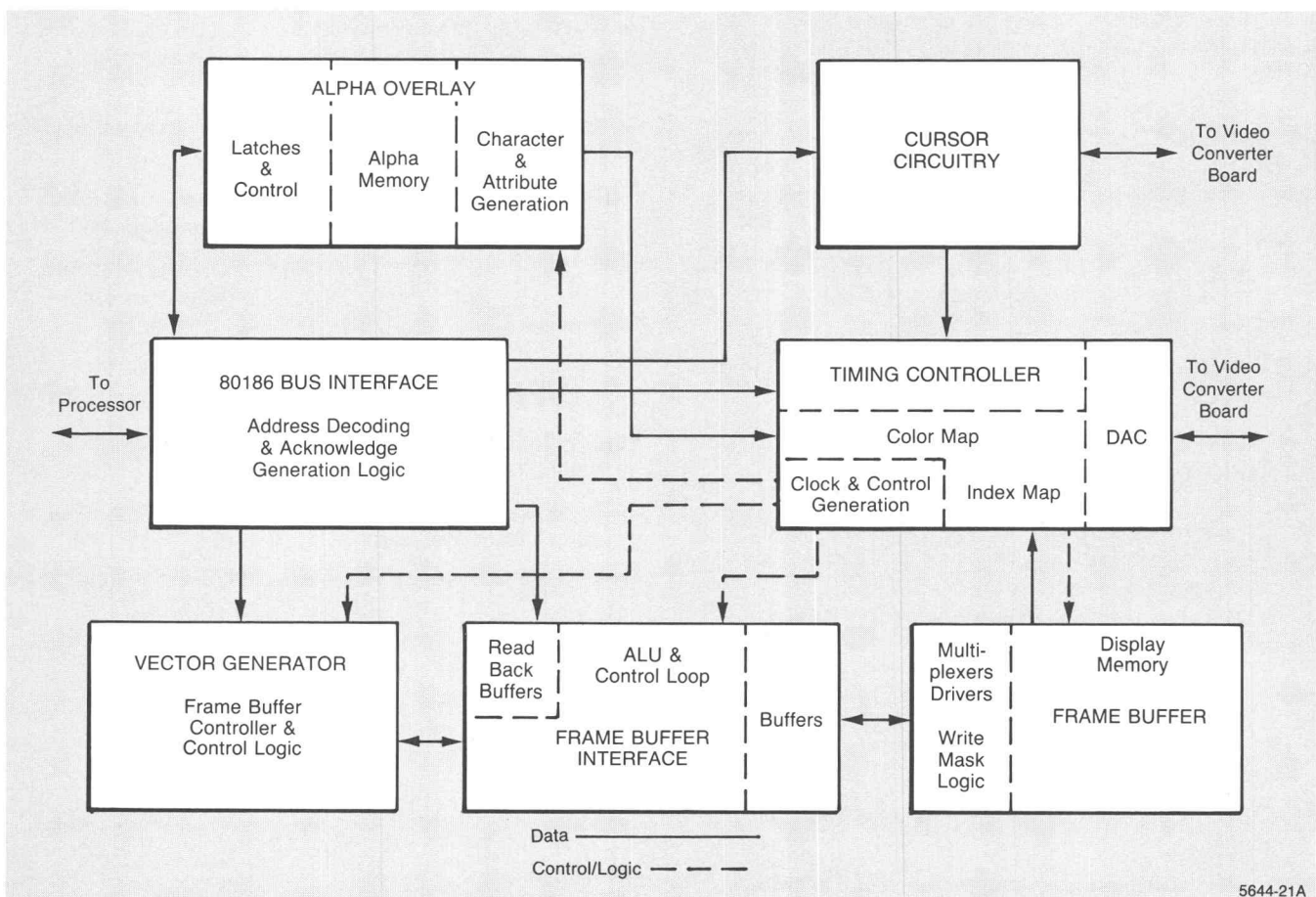


Figure 4-7. Display Control Board Block Diagram.

Address & Data Buffers (DSPLCTL-1)

Data Buffers. U488 and U492 buffer the data to/from the Terminal Control board. The buffers use the following signals:

- AD0-1 – AD15-1 (Address/Data Bus 0 – 15) become PD0-1 – PD15-1 (Processor Data Bus 0 – 15). Carry data between the Terminal Control board and the Display Control circuitry.
- DT/R-1 (Data Transmit/Receive) — Controls the direction of data flow through the buffers. When true, data flows from the Terminal Control board to the Display Control circuitry; when false, in the opposite direction.
- PCS0-0 (Peripheral Chip Select 0) and ARS-0 (Alpha RAM Select) — Enables the buffers when either is true.

Address Buffer. U494 buffers the address information for the lower half of the address information from the Terminal Control board. The buffer uses the following signals:

- LA0-1 – LA7-1 (Latched Address Bus 0 through 7) become PA0-1 – PA7-1 (Processor Address 0 through 7). Carry the lower half of the address information from the Processor.
- PCS0-0 (Peripheral Chip Select 0) — Enables the buffer when true.

I/O Address Decoder (DSPLCTL-1)

All I/O registers for the Display Control board reside in the address space 0000 to 007F. The Terminal Control board selects this section of memory by driving PCS0-0 true. U179, U180, and U182 decode the specific addresses in this range.

The I/O Address Decoder inputs are:

- PA1-1 – PA6-1 (Processor Address 0 through 6) — Contain the register address.
- IORC-0 (I/O Read Command) — True for an I/O read operation.
- IOWC-0 (I/O Write Command) — True for an I/O write operation.
- PCS0-0 (Peripheral Chip Select 0) — Terminal Control board drives PCS0-0 true when addressing the Display Control board I/O Registers. When either IORC-0 or IOWC-0 is true AND PCS0-0 is true, U179 is enabled. Depending on the address on PA1-1 through PA6-1, outputs of U179 combine with IORC-0 or IOWC-0 to enable U180 and/or U182.

The outputs of the I/O Address Decoder are:

- DDARD-0 & DDAWR-0 (DDA Read and DDA Write) — Enable internal registers of DDA Gate Array IC (U226)
- IMAPRD-0 & IMAPWR-0 (Index Map Read and Index Map Write) — Enable Index Map registers
- CMAPRD-0 & CMAPWR-0 (Color Map Read and Color Map Write) — Enable Color Map registers
- YADDRD-0 (Y Address Read) — Enables pixel address read register for Self-test
- MAJEXT-0 (Major Extent) — Enables major extent/rectangle X extent register
- XADDRD-0 (X Address Read) — Enables frame buffer control (FBC) busy/pixel address read register for Self-test
- RECYEXT-0 (Rectangle Y Extent) — Enables rectangle Y extent register
- FBCCMD-0 (Frame Buffer Control Command) — Enables mode control and FBC command register
- AOCTLRD-0 & AOCTLWR-0 (Alpha Overlay Read and Alpha Overlay Write) — Enable alpha overlay control register
- ALURD-0 & ALUWR-0 (ALU Read and ALU Write) — Enables frame buffer operation control register
- XCURSWR-0 (X Cursor Write) — Enables crosshair cursor X address register
- YCURSWR-0 (Y Cursor Write) — Enables crosshair cursor Y address register
- PIXELRD-0 (Pixel Read) — Enables pixel data register

Acknowledge Generator (DSPLCTL-1)

Since almost all of the I/O registers can be accessed by the Terminal Control board processor with no wait states, ACK-0 (Acknowledge) is true whenever PCS0-0 (Peripheral Chip Select 0) is true. However, there are two registers, the ALU Read/Write and the Pixel Read Registers, that the processor cannot always interrupt. These registers generate their own acknowledge signal, EN86ACC-0 (Enable 80186 Access).

The Acknowledge Generator logic prevents ACK-0 from following PCS0-0 true when the ALU or Pixel registers are accessed. This is accomplished by using PA1-1, PA3-1, and PA6-1 (Processor Address 1, 3, and 6) to disable the ACK-0 signal during an ALU or Pixel register access. When EN86ACC-0 becomes true, it drives ACK-0 true.

Overlay and Cursor Control Registers (DSPLCTL-1)

The Overlay and Cursor Control Registers are located at I/O address 0048.

The registers use data on PD0-1 – PD7-1 (Processor Data 0 through 7) for Alpha Overlay and crosshair cursor control. YSYNC-0 (Y Synchronization) enables the output of the registers. (This insures that the control functions only change at the beginning of a frame, not in the middle of a frame.)

The outputs are:

- ENBLNK-0 (Enable Blink) — Enables the character blink function
- CURBLNK-0 (Cursor Blink) — Enables cursor blinking
- ALPHAON-1 (Alpha On) — Enables character visibility
- XCURSEN-0 (X Cursor Enable) — Enable for the Cursor board

Clock Signal Generation (DSPLCTL-2)

Oscillator. The Oscillator circuit generates the 67.659 MHz clock that is the base for all Display Control board clock signals.

Clock Generator. The Clock Generator divides the output of the Oscillator into 33.8295 (divide-by-2), 16.9148 (divide-by-4), 8.4574 (divide-by-8), and 4.2287 (divide-by-16) MHz outputs.

Clock Drivers. The Clock Drivers buffer the outputs of the Oscillator and the Clock Generator and convert them to TTL or ECL levels (ECL levels will be noted). The outputs of the Clock Drivers are as follows:

- DDACLK-1 (DDA Clock) — 4.2287 MHz, used by the Vector Generator circuitry
- CNTRCLK-1 (Counter Clock) — 8.4574 MHz, used by the horizontal and vertical counters
- CHARCLK-0 & CHARCLK-1 (Character Clock) — 8.4574 MHz, used by the Alpha Overlay circuitry
- 2XDCLK-1 (2 Times D Clock) — 33.8295 MHz, used by the blanking and sync delay registers (one half the frequency or twice the time of DCLK-1)
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock) — 16.9148 MHz, used by the Display Memory Control State Machine
- RAMSCLK-1 (RAM Shift Clock) — 16.9148 MHz, used by the RAM Shift Register
- SRLD-0 & SRLD-1 (Shift Register Load) — 16.9148 MHz, used by the Pixel Data Shift Registers (SRLD-0 has an ECL signal level)
- DCLK-1 (Data Clock) — 67.659 MHz, used by the Pixel Data Shift Register
- DACCLK-1 (Digital-to-Analog-Converter Clock) — 67.659 MHz, used by the Digital-to-Analog-Converters (ECL signal level)
- DCLKB-0 & DCLKB-1 (Data Clock B) — 67.659 MHz, used by the Pixel Data Pipe Line Registers (ECL signal levels)
- DCLKA-1 (Data Clock A) — 67.659 MHz, used by the Pixel Data Pipe Line Registers (ECL signal level)

Frame Buffer Control (DSPLCTL-3 & DSPLCTL-4)

The Frame Buffer Controller (FBC) DDA Gate Array (U226) contains the data paths necessary to provide the correct screen address, pixel data, and dash information for the graphics display. The FBC contains internal I/O registers at I/O addresses from 0000 to 0018, which contain the information for the X and Y address outputs (X0-1 through X10-1 and Y0-1 through Y10-1), the pixel data (PX0-1 through PX3-1, from U218B, the Pixel Register), and the Dash Mode Control (U148D and U128D).

The FBC is controlled by the X Counter (U140 and U122), the Y Counter (U338 and U113), part of the Bus I/F & Control Logic (U210A, U210B, and U124B), the State Machine (U214, U220, and U212), and their associated logic.

The X and Y Counters determine the length of a line, as well as the width and depth of a rectangle. The State Machine generates the FBC control signals while the counters are counting. The counters stop the State Machine when they reach the desired count.

The State Machine supports four drawing commands: draw line, draw line without first pixel (for XOR function), rectangle pixelate, and read data/move a predetermined distance (for pixel read operations).

The Major Extent/Rectangle X Extent Register (U138), which is accessed by a Write to I/O address 0042, determines the length of a line in Vector mode, the width of a rectangle in Rectangle mode, or the number of pixels to be moved in Pixel mode.

The Rectangle Y Extent Register (U338), which is accessed by a Write to I/O address 0044, specifies the height of a rectangle and starts the execution of that rectangle when written to. This register is used only in Rectangle mode.

The X Address Register (U438), which is accessed by a Read to I/O address 0042, allows the Terminal Control board processor to read back the current X-axis pixel address.

The Y Address Register (U438 and U440), which is accessed by a Read to I/O address 0044, allows the Processor to read back the current Y-axis pixel address, and also allows polling of FBCBUSY-1 (Frame Buffer Controller Busy).

The Command Register (U218A), which is accessed by a Write to I/O address 0046, controls the operating mode of the FBC (such as Rectangle, Vector, etc.).

Following are the definitions of the FBC Control and DDA Gate Array input signals:

- PD0-1 – PD15-1 (Processor Data) — Buffered Data from the Terminal Control board's processor
- WRCLR-1 (Write Clear) — Clears the flip-flops that load the X and Y Counters
- DDACLK-1 (DDA Clock), CHARCLK-0 (Character Clock), and DDACLKEN-0 (DDA Clock Enable) — Clocks for the State Machine
- MAJEXT-0 (Major Extent) — Enables the Major Extent/Rectangle X Extent Register when true
- RECYEXT-0 (Rectangle Y Extent) — Enables the Rectangle Y Extent Register when true
- C0-1 & C1-1 (Command 0 and 1) — Outputs of the Command Register that set the mode of the State Machine (Vector mode, Rectangle mode, etc.)
- PIXELRD-0 (Pixel Read) — Notifies the State Machine to enable the Pixel Register for a read when true
- XADDRD-0 (X Address Read) — Enables the X0-1 – X10-1 and Y0-1 – Y4-1 Address Read Back latches when true
- FBCBUSY-1 (Frame Buffer Controller Busy) — True when the FBC is busy and cannot be interrupted
- YADDRD-0 (Y Address Read) — Enables the Y5-1 through Y10-1 Address Read Back latches when true
- PA1-1 – PA4-1 (Processor Address 1 through 4) — Buffered Address information from the Terminal Control board's processor
- AD0-1 – AD15-1 (Address/Data Bus) — The Processor Address/Data Bus from the Terminal Control board
- DDARD-0 (DDA Read) — Enables FBC internal read registers when true
- DDAWR-0 (DDA Write) — Enables FBC internal write registers when true

- ADDCLK-1 (Address Clock), DDACLK-1 (DDA Clock), & SRCLK-1 (Shift Register Clock) — Clock outputs of the State Machine, used by the FBC
- XLD-1 (X Load) — Loads the X registers in the FBC
- YUPEN-0 (Y Up Enable) — Enables the Y registers in the FBC
- BCLK-1 (Bus Clock) — Bus clock signal from the Terminal Control board
- PIX-0 (Pixel) — Enables the Pixel Register when true
- RAS-0 (Row Address Strobe) — Strokes the row address into the RAMs; used by the FBC circuitry to load the Address Latches
- ILOADREN-0 (I/O Address Enable) — Enables the output of the Address Latches when true
- PCS0-0 (Peripheral Chip Select 0) — Goes true whenever an I/O Read or Write to any Display Control board register occurs
- FBCCMD-0 (Frame Buffer Controller Command) — Enables the Command Register when true

Cursor Board (CURSOR-1)

NOTE

Although the Cursor board is separate from the 670-8524-nn Display Control board, it functions as a Display Control circuit block. Therefore, this discussion will treat the Cursor board as though it was a functional block on the earlier version Display Control board.

X and Y Address Latches. The X and Y Address Latches (U16 and U14, respectively) latch the position where the crosshair cursor is to be moved (from the Processor on the Terminal Control board, via PD0-1 – PD9-1 (Processor Data 0 through 9). XCURSWR-0 (X Cursor Write) latches the X address and YCURSWR-0 (Y Cursor Write) latches the Y address.

X Address Counters. The X Address Counters (U20, U22, and U24) use DCLKB-0 (Display Clock B) and DCBLANK-0 (Display Control Blank) to provide the count for the X crosshair address. The Vertical Control Logic on the Display Control board supplies the Y count.

ECL X Address. U112, U114, and U116 converts the X address and the output of the Y Address Comparator from TTL levels to ECL levels.

X and Y Address Comparators. The X Address Comparator (U122 and U124) and the Y Address Comparator (U12) compare the position where the crosshair cursor is to be moved to the count for the appropriate axis.

The Y comparator compares the Y address to the count from the Vertical Control Logic on V0-1 – V9-1 (Vertical 0 through 9). When the Y comparison is equal, the output of the comparator forces the output of the X comparator to go true.

The X comparator compares the X address to the count generated by the X Address Counters. When the comparison is equal and DCBLANK-0 (Display Control Blank) is false, CURON-0 (Cursor On) goes true.

186 Pixel Read Back Latches (DSPLCTL-5)

U328 and U330 latch pixel data from the Frame Buffer to be read by the Processor. LTCH86-1 (Latch 80186) latches the data and PIXELRD-1 (Pixel Read) enables the outputs.

1 of 4 Pixel Selector (DSPLCTL-5)

The 1 of 4 Pixel Selector (part of U324) selects which one of the four pixels from the Frame Buffer is to be written/modified.

ALU Control Register (DSPLCTL-5)

The ALU Control Register (U334) sets the Pixel ALU for the correct mode needed by the vector generating circuitry when doing pixel operations. ALUWR-0 (ALU Write), ALURD-0 (ALU Read), and the data on D0-1 – D7-1 (Data 0 through 7) determine the mode.

Visibility and Write Mask Select Register (DSPLCTL-7)

The Visibility and Write Mask Select register is part of the ALU Control Register and uses the upper 8 bits of the Processor data (PD8-1 – PD15-1) to determine which pixels in a nibble will be visible (VIS0-1 – VIS3-1) and to enable the correct write control multiplexer.

FBI Pixel Data Path (DSPLCTL-5)

The Pixel Data Path contains the Pixel ALU and four buffers.

Buffers U314 and U318 buffer pixel data to/from the 186 Pixel Read Back Latches. The enable signals for the buffers come from the 1 of 4 Pixel Selector.

The Pixel ALU performs arithmetic operations on the outputs of U314 and U318 and sends the results to the Frame Buffer via buffers U320 and U322. The ALU Control Register sets the mode of the ALU.

Table 4-1 shows the ALU modes and the ALU Control Register inputs necessary to set these modes. In the table, D0-1 – D5-1 (Data 0 through 5) are ALU Control Register Inputs, F is the Pixel ALU output, A is the ALU input from the 186 Pixel Read Back Latches, and B is the ALU input from the 1 of 4 Write Mask Selector.

Table 4-1
ALU OPERATION

Mode	D5-1	D4-1	D3-1	D2-1	D1-1	D0-1	ALU Operation
SET	True or False	True	True	False	True	False	$F = A$
AND	True or False	True	True	False	True	True	$F = AB$
OR	True or False	True	True	True	True	False	$F = A \text{ OR } B$
XOR	True or False	True	False	True	True	False	$F = A \text{ XOR } B$
ADD	True	False	False	False	False	True	$F = A + B$
NOP	True or False	True	True	True	True	True	$F = A$
SUB	False	False	False	True	True	False	$F = A - B$

Horizontal & Vertical Counters and Control Logic (DSPLCTL-5)

The Horizontal and Vertical Counters use CNTRCLK-1 (Counter Clock) to generate the following signals:

- HSYNC-0 (Horizontal Synchronization)
- OVLYLDCLK-1 (Overlay Load Clock)
- SCRNTIM-0 (Screen Timing)
- IOADREN-0 (I/O Address Enable)
- RFSHREQ-0 (Refresh Request)
- VSYNC-0 (Vertical Synchronization)
- VBLANK-0 (Vertical Blanking)
- HBLANK-0 (Horizontal Blanking)

U378 and U478 generate the vertical control signals, and U470 and U481 generate the horizontal control signals. U472 and U474 use the output of the vertical control to produce the refresh address for the Display Memory.

Composite Sync/Blank Delay (DSPLCTL-6)

This logic delays VSYNC-0 (Vertical Synchronization), HSYNC-0 (Horizontal Synchronization), and VBLANK-0 (Vertical Blanking) to create the following:

- DCSYNC-0 (Display Composite Synchronization)
- DCBLANK-0 (Display Composite Blanking)

Display Memory Controller (DSPLCTL-6)

The Display Memory Control controls memory read cycles (performed by the Processor) and memory write cycles (performed by the Vector Generator circuitry) to the Display Memory.

The Display Memory Control circuitry uses the following inputs:

- RDMWR-0 (Read/Modify/Write) — When true, causes the state machine to perform a read/modify/write to Display Memory.
- RFSHREQ-0 (Refresh Request) — When true, causes the state machine to perform a refresh.
- IOADREN-0 (I/O Address Enable) — When true, allows the Vector Generator circuitry to address the Display Memory; when false, the address to the Display Memory is the refresh address.
- SCRNTIM-0 (Screen Timing) — When true, signifies that the address on the Address bus is for a refresh.
- PIXELRD-0 (Pixel Read) — Indicates that the Processor is requesting a Display Memory read cycle; also enables the acknowledge back to the Processor.
- Y10-1 (Y Address 10) — The most significant bit of the Y address; if true with RDMWR-0, a memory cycle will not occur. (This is to keep all writes to the Display Memory in a 1024 × 1024 bit map space.)
- X10-1 (X Address 10) — The most significant bit of the X address; if true with RDMWR-0, a memory cycle will not occur. (This is to keep all writes to the Display Memory in a 1024 × 1024 bit map space.)
- ALURD-0 (ALU Read) — When true, creates ALUACC-1 (ALU Access) to the State Machine.
- ALUWR-0 (ALU Write) — When true, creates ALUACC-1 (ALU Access) to the State Machine.
- OVLYCLK-1 (Overlay Clock) — Latches the next line address for the Alpha Overlay.
- DDACLK-1 (DDA Clock) — Used by the state machine to synchronize the memory cycle to the refresh cycles.
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock).
- RESET-0 (Reset) — System reset.
- IMAPWR-0 (Index Map Write) — Write strobe to the Index Map.
- CMAPWR-0 (Color Map Write) — Write strobe to the Color Map.
- BCLK-1 (Bus Clock) — Processor bus clock.
- IORDWR-1 (I/O Read/Write) — Signals an I/O read or write cycle.

The Display Memory Control has the following outputs:

- COL-0 (Column) — Selects the line for the Display Memory to pick either a row or column address
- RAS-0 (Row Address Strobe) — Strobes the row address into the Display Memory
- CAS-0 (Column Address Strobe) — Strobes the column address into the Display Memory
- TRQE-0 (Transfer/Queue Enable) — If true before RAS-0 goes true, signifies a register transfer or a refresh; if true after RAS-0 goes true, signifies a memory cycle. Always goes true when COL-0 goes true
- MW-0 (Memory Write) — Strobes data into Display Memory
- RAMSCLKEN-0 (RAM Shift Clock Enable) — Enable strobe for RAMSCLK-1
- DDACLKEN-0 (DDA Clock Enable) — Enable strobe for DDACLK-1
- EN86ACC-0 (Enable 80186 Access) — Acknowledge signal to the Processor; also used for gating read/write strobes into the I/O registers
- LTCH86-1 (Latch 80186) — Used to latch display data for a Processor read of the Display Memory
- IMAPWR-1 (Index Map Write)
- CMAPWR-1 (Color Map Write)

Address MUX and Driver (DSPLCTL-7)

The Address MUX and Driver multiplexes the frame buffer address into the correct row address for the Display Memory.

RAM Bank Select Logic (DSPLCTL-7)

The RAM Bank Select Logic decodes the two most significant bits of the frame buffer address (FB18-1 & FB19-1), I/OADREN-0 (I/O Address Enable), RAS-0 (Row Address Strobe), and CAS-0 (Column Address Strobe) to gate the following control signals for each RAM bank:

- CAS0-0 — CAS2-0 (Column Address Strobes 0, 1, and 2)
- RAS0-0 — RAS2-0 (Row Address Strobes 0, 1, and 2)
- SRCLK0-1 — SRCLK2-1 (Shift Register Clocks 0, 1, and 2)
- SOE0-0 — SOE2-0 (Shift Output Enables, 0, 1, and 2)

1 of 4 Write Select (DSPLCTL-7)

The 1 of 4 Write Select uses the two least significant bits (FB0-1 & FB1-1) to determine which pixel of the four pixel nibble from the Display Memory should be written.

Write Control Logic (DSPLCTL-7)

The multiplexers of the Write Control Logic (U413, U416, U420, and U422) produce the Write Enable signals for the correct bank of RAM in the Display Memory (WEA0-1 – WEA3-1, WEB0-1 – WEB3-1, WEC0-1 – WEC3-1, and WED0-1 – WED3-1).

Display Memory (DSPLCTL-8 & DSPLCTL-9)

The Display Memory (Frame Buffer) contains 48 TMS4161-20 high-speed, dual-port, 65536-bit, random-access video RAMs. Each bit plane contains twelve RAMs as follows:

- Plane 0 — U518, U520, U522, U524, U528, U530, U532, U534, U538, U540, U542, and U544
- Plane 1 — U614, U618, U620, U624, U628, U630, U632, U634, U638, U640, U642, and U644
- Plane 2 — U718, U720, U722, U724, U728, U730, U732, U734, U738, U740, U742, and U744
- Plane 3 — U813, U815, U819, U821, U827, U829, U831, U833, U837, U839, U841, and U843

The display screen is divided into 3 areas. Four RAMs in the Display Memory serve each area (Figure 4-8). The rows of RAMs shown for each bit plane on the schematic correspond to the 3 areas of the screen shown in Figure 4-8.

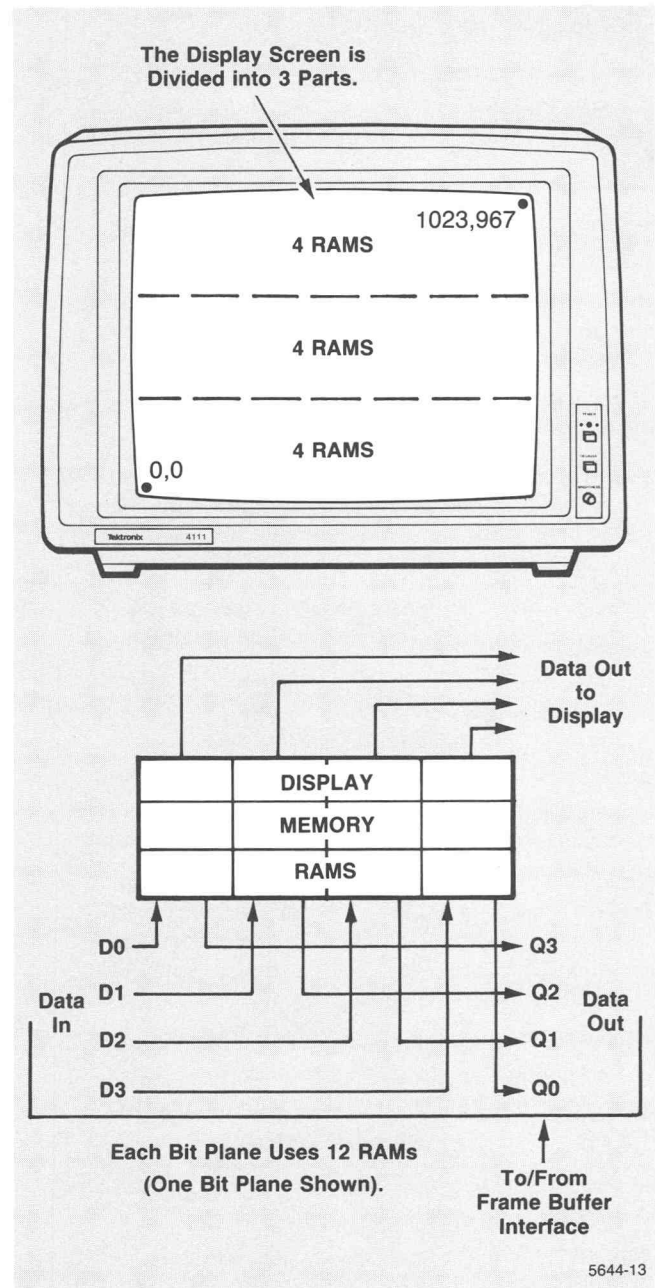


Figure 4-8. Display Memory Organization.

Alpha Overlay Circuitry (DSPLCTL-10 & DSPLCTL-11)

The Alpha Overlay circuitry allows the alphanumeric characters and the background of the dialog area to overlay the graphics display.

Alpha RAM Address Generator. The Alpha RAM Address Generator generates the address for the Alpha RAM during display refresh and Processor read/write cycles. During display refresh cycles, OVLYLDCLK-1 (Overlay Load Clock) latches the row address (V9-1 through V4-1 — Vertical 9 through 4) into U172 at the beginning of each line refresh. At the same time, the character line address (V3-1 through V0-1 — Vertical 3 through 0) is latched into U170. (The character line address goes to the Font ROMs to specify which of the 16 character cell lines is being refreshed.) Valid column addresses are from 0 to 131, while valid row addresses are from 0 to 47.

Three multiplexers (U168, U268, and U164) select whether the address source is the latched address from U172 (for display refresh cycles) or the latched address from LA2-1 through LA14-1 (Latched Address 2 through 14 — for Processor I/O cycles). Another multiplexer (U264) performs the address translation required to put the extra four characters per line (the dialog area extends beyond the graphics area by four characters) into the Alpha Memory Array without using extra ROMs.

Alpha Memory Array. The Alpha Memory Array consists of two banks of 4K × 4 static RAMs. Since each character requires two bytes of information (one byte for the character and one byte for the attributes), the RAM can store 8000 characters and their attributes.

In RAM Bank 0, U254 and U258 contains the characters, while U152 and U154 contain the attributes. In RAM Bank 1, U454 and U458 contain the characters, and U354 and U358 contain the attributes.

RAM Bank 0 contains even memory addresses, while RAM Bank 1 contains odd addresses. This allows the Alpha RAM Control to read two adjacent characters each memory cycle for display refreshing. This leaves alternate memory cycles open for the Processor to access the RAM if necessary.

To accommodate the extra four characters at the end of the line (the four characters that the Dialog area can write that extend beyond the Graphics area), the Alpha RAM Address Generator maps these characters into unused memory space (Table 4-2).

Table 4-2
RAM BANK ADDRESSES

Bank Number	Address	Column Numbers
Bank 0	0 — BFF	0 through 127
	C00 — FFF	128 through 131
Bank 1	0 — BFF	0 through 127
	C00 — FFF	128 through 131

Character and Attribute Output Registers. The four registers (U160, U260, U360, and U460) hold two characters and their attributes at one time. Each sixteen bit character word contains the following information:

- Bit 0 — The least significant bit of the character byte (FD0-1)
- Bit 1 — The second bit of the character byte (FD1-1)
- Bit 2 — The third bit of the character byte (FD2-1)
- Bit 3 — The fourth bit of the character byte (FD3-1)
- Bit 4 — The fifth bit of the character byte (FD4-1)
- Bit 5 — The sixth bit of the character byte (FD5-1)
- Bit 6 — The most significant bit of the character byte (FD6-1)
- Bit 7 — FD7-1 (Font Data 7). Selects alternate character set if true
- Bit 8 — ALTCOL2-1 (Alternate Color 2). Used with ALTCOL1-1 and ALTCOL0-1 to select one of eight Dialog area foreground/background color pairs
- Bit 9 — ALTCOL1-1 (Alternate Color 1)
- Bit A — ALTCOL0-1 (Alternate Color 0)
- Bit B — UDL-1 (Underline)
- Bit C — BLINK-1 (Blink)
- Bit D — INV 1 (Inverse)
- Bit E — OPAQ-1 (Opaque)
- Bit F — CURSOR-1 (Cursor)

THEORY OF OPERATION

Alpha RAM Control. The Alpha RAM Control contains a state machine (PAL U286), a decoder (U174 and U382A), a flip-flop (U380B), and associated logic gates.

The state machine PAL controls the reads and writes to the Alpha Memory Array: controlling the memory cycle switching, generating the control signals for the Alpha RAM Data Transceiver/Latches, and generating ACK-0 (Acknowledge). All memory cycles are available to the Processor during horizontal and vertical retrace and when the Dialog area is disabled. The Processor can use alternate memory cycles during refresh.

The decoder provides directional control for the data to/from the Alpha RAM Data Transceiver/Latches and the Alpha Memory Array.

The flip-flop enables the output of the Character and Attribute Output Registers.

Alpha RAM Data Transceiver/Latches. The four latches (U368, U370, U372, and U374) hold data going to/from the Processor and the Alpha Memory Array. During Alpha RAM writes (IOWC-0 true), the decoder in the Alpha RAM Control drives Pin 1 of the latches low, allowing data to flow from the Processor Data Bus to the Alpha Memory Array. During Alpha RAM reads (IORC-0 true), the latches hold the data from the Alpha Memory Array until IORC-0 goes false.

Font ROMs. The Font ROMs (U142 and U144) contain the characters, with each character occupying a 7×9 cell in an 8×16 matrix. Character scanning begins with Scan Line 0 at the top of the cell and progresses line-by-line downward through the cell. Scan Lines 0, 1, 2, and 15 are blank for spacing between lines and the leftmost column is blank for spacing between characters. Descenders on lower case characters (y, j, etc.) use Scan Lines 12 through 14. The cursor and character underline are NOT contained in the Font ROMs.

The 12 bits of the incoming font address are the seven character bits (FD0-1 through FD6-1 — Font Data 0 through 6), four character line bits (CL0-1 through CL3-1 — Character Line 0 through 3), and the eighth bit of the character word, which selects the font.

Character Generator. The Character Generator generates two character attributes (underline and blink) and the cursor. U274 uses VSYNC-0 (Vertical Synchronization) to generate the 75% duty cycle clock that controls the blink rate. PAL U348 uses this clock signal plus the following inputs:

- UDL-1 (Underline) — Enables character underline
- BLINK-0 (Blink) — Sets the character blink function
- CURSOR-1 (Cursor) — Turns on the cursor
- CURBLNK-0 (Cursor Blink) — Sets the cursor to blink
- ENBLNK-0 (Enable Blink) — Enables all blinking functions
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock) — Clocks the PAL
- DIALON-1 (Dialog On) — Enables the Dialog area
- CHLIN0-1 through CHLIN3-1 (Character Line 0 through 3) — Shows which scan line of a character cell is being displayed

The PAL has two outputs:

- The Pin 14 output turns on all of the pixels in an appropriate scan line for the cursor or an underline.
- The Pin 15 output enables the character output when the Dialog area is enabled and turns the characters on/off for character blinking.
- The Pin 16 output turns off the character/attribute outputs at the end of each line.

U432A uses INV-1 (Inverse) and CHARCLK-1 (Character Clock) to “reverse” Dialog area character and background colors.

Video Output Path. The output of the Font ROMs is an 8-pixel character pattern. The Video Output stage requires character pixels to be released four at a time, at twice the CHARCLK-1 (Character Clock) rate.

U344 (a dual 4-bit flip-flop) latches the 8-pixel character and releases the pixels four at a time. The two flip-flops in U344 are alternately clocked by CHARCLK-1. When CHARCLK-1 is true, the first four pixels are sent, and when CHARCLK-1 is false, the last four pixels go out. The Pin 14 output of PAL U348, in the Character Generator, turns on all outputs from U344 during a cursor or an underline.

Exclusive OR gates U448A, B, C, and D allow the Character Generator to “reverse” the character and background colors for an Inverse function.

Alpha Index Map (DSPLCTL-12)

The Index Map, like the color map, interprets the alpha data as an address into the Color Map. In this manner, the alpha data can assume one of eight colors.

The Alpha Overlay has only three attribute bits for alternate colors. These bits, combined with the pixel data, give a total of eight displayable colors at one time. The remaining attribute is the background color, and, when it is asserted, causes the background to be opaque in a color that is determined by the other three attribute bits.

Pixel Data Shift Registers (DSPLCTL-12)

U754, U758, U854, and U858 convert the four-pixel data from the Display Memory to one-pixel data for the pixel data pipeline.

Pixel Data Pipeline Registers (DSPLCTL-12)

U860 converts the outputs of the Pixel Data Shift Registers from TTL levels to ECL levels. U864 latches the outputs of U860, as well as CURON-0 and the output of Pin 14 of U872. U870 buffers the outputs of U864.

Pixel Data/Alpha Data Pipeline Register (DSPLCTL-12)

U872 latches the outputs of the Pixel Data Pipeline Registers, combined with the output address from the Index Map.

Attribute Generator (DSPLCTL-12)

U380A latches the character attributes for the character and background colors, as well as the opaque attribute. (Refer to the discussion of the Alpha Index Map for more information on these attributes.) CHARCLKD-1 (Character Clock Delayed) clocks the attributes in to U380A, while DIALON-1 enables the outputs.

Alpha Data Shift Registers (DSPLCTL-12)

Shift registers U650 and U654 combine the attribute data and the character data, while U760 converts the combined data from TTL levels to ECL levels for the Index Map.

186 Color Map Write Data Buffers (DSPLCTL-13)

U554, U558, and U560 buffer the data from PD0-1 – PD11-1 (Processor Data 0 through 11) and convert it from TTL to ECL levels.

Color Map (DSPLCTL-13)

Pixel data inputs to the Color Map (U772, U776, and U876) act as an address pointing to a specific 4-bit word. This 4-bit word (0 – 16) is the value of the percentage of the specific color corresponding to a pixel. U776 handles the red data, U772 the green data, and U876 the blue data. All three Color Map ICs see the same address, but can modify the intensity of the colors for that address separately.

186 Color Map Read Data Buffers (DSPLCTL-13)

U568, U574, U578, and U580 buffer the outputs of the Color Map and convert them to TTL levels for buffers U482 and U484. The Processor can read the output of these latches.

DAC (DSPLCTL-13)

The DAC (Digital-to-Analog-Converter) converts digital pixel data from the Color Map into analog red, green, and blue signals for the Display Module circuitry.

The following synchronization, blanking, and clock signals provide control for the DAC (U792):

- DACCKLK-1 (Digital-Analog-Conversion Clock)
- DACSYNC-0 (Digital-Analog-Conversion Synchronization)
- DACBLANK-0 (Digital-Analog-Conversion Blanking)
- DACCUR-0 (Digital-Analog-Conversion Cursor)

DISPLAY CONTROL BOARD CIRCUIT DESCRIPTION (670-9725-NN)

Introduction

The later version Display Control board circuitry can also be divided into 50 functional blocks. The following text explains the circuitry and operation of each block. Refer to the 26 schematic diagrams (referenced in the descriptions) and the Display Control board timing diagrams in Section 10 of this manual while reading the descriptions.

Figure 4-7 (for the earlier version Display Control board) also shows the general configuration and operation of the newer Display Control board.

Address & Data Buffers (NEWDC-5)

Data Buffers. U676 and U681 buffer the data to/from the Terminal Control board. The buffers use the following signals:

- AD0-1 – AD15-1 (Address/Data Bus 0 – 15) — Become PD0-1 – PD15-1 (Processor Data Bus 0 – 15). These lines carry data between the Terminal Control board and the Display Control circuitry.
- DT/R-1 (Data Transmit/Receive) — Controls the direction of data flow through the buffers. When true, data flows from the Terminal Control board to the Display Control circuitry; when false, data flows in the opposite direction.
- PCS0-0 (Peripheral Chip Select 0) and ARS-0 (Alpha RAM Select) — Enables the buffers when either is true.

Address Buffer. U675 buffers the lower half of the address information from the Terminal Control board. The buffer uses the following signals:

- LA0-1 – LA7-1 (Latched Address Bus 0 through 7) — Become PA0-1 – PA7-1 (Processor Address 0 through 7). These lines carry the lower half of the address information from the Processor.
- PCS0-0 (Peripheral Chip Select 0) — Enables the buffer when true.

I/O Address Decoder (NEWDC-5)

All I/O registers for the Display Control board reside in the address space 0000 to 007F. The Terminal Control board selects this section of memory by driving PCS0-0 true. U575, U571, and U552 decode the specific addresses in this range.

The I/O Address Decoder inputs are:

- PA1-1 – PA6-1 (Processor Address 0 through 6) — Contain the register address.
- IORC-0 (I/O Read Command) — True for an I/O read operation.
- IOWC-0 (I/O Write Command) — True for an I/O write operation.
- PCS0-0 (Peripheral Chip Select 0) — Terminal Control board drives PCS0-0 true when addressing the Display Control board I/O Registers. When either IORC-0 or IOWC-0 is true AND PCS0-0 is true, U575 is enabled. Depending on the address on PA1-1 through PA6-1, outputs of U575 combine with IORC-0 or IOWC-0 to enable U571 and/or U552.

The outputs of the I/O Address Decoder are:

- DDARD-0 & DDAWR-0 (DDA Read and DDA Write) — Enable internal registers of DDA Gate Array IC (U505)
- IMAPRD-0 & IMAPWR-0 (Index Map Read and Index Map Write) — Enable Index Map registers
- CMAPRD-0 & CMAPWR-0 (Color Map Read and Color Map Write) — Enable Color Map registers
- YADDRD-0 (Y Address Read) — Enables pixel address read register for Self-test
- MAJEXT-0 (Major Extent) — Enables major extent/rectangle X extent register
- XADDRD-0 (X Address Read) — Enables frame buffer control (FBC) busy/pixel address read register for Self-test
- RECYEXT-0 (Rectangle Y Extent) — Enables rectangle Y extent register
- FBCCMD-0 (Frame Buffer Control Command) — Enables mode control and FBC command register
- AOCTLRD-0 & AOCTLWR-0 (Alpha Overlay Read and Alpha Overlay Write) — Enable alpha overlay control register
- ALURD-0 & ALUWR-0 (ALU Read and ALU Write) — Enables frame buffer operation control register
- XCURSWR-0 (X Cursor Write) — Enables crosshair cursor X address register
- YCURSWR-0 (Y Cursor Write) — Enables crosshair cursor Y address register
- PIXELRD-0 (Pixel Read) — Enables pixel data register

Acknowledge Generator (NEWDC-5)

Since almost all of the I/O registers can be accessed by the Terminal Control board processor with no wait states, ACK-0 (Acknowledge) is true whenever PCS0-0 (Peripheral Chip Select 0) is true. However, there are two registers, the ALU Read/Write and the Pixel Read Registers, that the processor cannot always interrupt. These registers generate their own acknowledge signal, EN86ACC-0 (Enable 80186 Access).

The Acknowledge Generator logic prevents ACK-0 from following PCS0-0 true when the ALU or Pixel registers are accessed. This is accomplished by using PA1-1, PA3-1, and PA6-1 (Processor Address 1, 3, and 6) to disable the ACK-0 signal during an ALU or Pixel register access. When EN86ACC-0 becomes true, it drives ACK-0 true.

Overlay and Cursor Control Registers (NEWDC-6)

The Overlay and Cursor Control Registers are located at I/O address 0048. The registers use data on PD0-1 – PD7-1 (Processor Data 0 through 7) for Alpha Overlay and crosshair cursor control. YSYNC-0 (Y Synchronization) enables the output of the registers. (This insures that the control functions only change at the beginning of a frame, not in the middle of a frame.)

The outputs are:

- ENBLNK-0 (Enable Blink) — Enables the characters blink function
- CURBLNK-0 (Cursor Blink) — Enables cursor blinking
- ALPHAON-1 (Alpha On) — Enables character visibility
- XCURSEN-0 (X Cursor Enable) — Enable for the Cursor board

Clock Signal Generation (NEWDC-8)

Oscillator. The Oscillator circuit generates the 67.659 MHz clock that is the base for all Display Control board clock signals.

Clock Generator. The Clock Generator divides the output of the Oscillator into 33.8295 (divide-by-2), 16.9148 (divide-by-4), 8.4574 (divide-by-8), and 4.2287 (divide-by-16) MHz outputs.

THEORY OF OPERATION

Clock Drivers. The Clock Drivers buffer the outputs of the Oscillator and the Clock Generator and they convert these to TTL or ECL levels (ECL levels will be noted). The outputs of the Clock Drivers are as follows:

- DDACLK-1 (DDA Clock) — 4.2287 MHz, used by the Vector Generator circuitry
- CNTRCLK-1 (Counter Clock) — 8.4574 MHz, used by the horizontal and vertical counters
- CHARCLK-0 & CHARCLK-1 (Character Clock) — 8.4574 MHz, used by the Alpha Overlay circuitry
- 2XDCLK-1 (2 Times D Clock) — 33.8295 MHz, used by the blanking and sync delay registers (one half the frequency or twice the time of DCLK-1)
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock) — 16.9148 MHz, used by the Display Memory Control State Machine
- RAMSCLK-1 (RAM Shift Clock) — 16.9148 MHz, used by the RAM Shift Register
- SRLD-0 & SRLD-1 (Shift Register Load) — 16.9148 MHz, used by the Pixel Data Shift Registers (SRLD-0 has an ECL signal level)
- DCLK-1 (Data Clock) — 67.659 MHz, used by the Pixel Data Shift Register
- DACCLK-1 (Digital-to-Analog-Converter Clock) — 67.659 MHz, used by the Digital-to-Analog-Converters (ECL signal level)
- DCLKB-0 & DCLKB-1 (Data Clock B) — 67.659 MHz, used by the Pixel Data Pipe Line Registers (ECL signal levels)
- DCLKA-1 (Data Clock A) — 67.659 MHz, used by the Pixel Data Pipe Line Registers (ECL signal level)

Frame Buffer Control (NEWDC-21, 22, and 23)

The Frame Buffer Controller (FBC) DDA Gate Array (U505) contains the data paths necessary to provide the correct screen address, pixel data, and dash information for the graphics display. The FBC contains internal I/O registers at I/O addresses from 0000 to 0018, which contain the information for the X and Y address outputs (X0-1 through X10-1 and Y0-1 through Y10-1), the pixel data (PX0-1 through PX3-1, from U211, the Pixel Register), and the Dash Mode Control (U735 and U726).

The FBC is controlled by the X Counter (U625 and U722), the Y Counter (U626 and U725) part of the Bus I/F & Control Logic (U522, and U721), the State Machine (U611, U615, and U612), and their associated logic.

The X and Y Counters determine the length of a line, as well as the width and depth of a rectangle. The State Machine generates the FBC control signals while the counters are counting. The counters stop the State Machine when they reach the desired count.

The State Machine supports four drawing commands: draw line, draw line without first pixel (for XOR function), rectangle pixelate, and read data/move a predetermined distance (for pixel read operations).

The Major Extent/Rectangle X Extent Register (U622), which is accessed by a Write to I/O address 0042, determines the length of a line in Vector mode, the width of a rectangle in Rectangle mode, or the number of pixels to be moved in Pixel mode.

The Rectangle Y Extent Register (U626), which is accessed by a Write to I/O address 0044, specifies the height of a rectangle and starts the execution of that rectangle when written to. This register is used only in Rectangle mode.

The X Address Register (U716), which is accessed by a Read to I/O address 0042, allows the Terminal Control board processor to read back the current X-axis pixel address.

The Y Address Register (U716 and U521), which is accessed by a Read to I/O address 0044, allows the Processor to read back the current Y-axis pixel address, and also allows polling of FBCBUSY-1 (Frame Buffer Controller Busy).

The Command Register (U211), which is accessed by a Write to I/O address 0046, controls the operating mode of the FBC (such as Rectangle, Vector, etc.).

Following are the definitions of the FBC Control and DDA Gate Array input signals:

- PD0-1 – PD15-1 (Processor Data) — Buffered Data from the Terminal Control board's processor
- WRCLR-1 (Write Clear) — Clears the flip-flops that load the X and Y Counters
- DDACLK-1 (DDA Clock), CHARCLK-0 (Character Clock), and DDACLKEN-0 (DDA Clock Enable) — Clocks for the State Machine
- MAJEXT-0 (Major Extent) — Enables the Major Extent/Rectangle X Extent Register when true
- RECYEXT-0 (Rectangle Y Extent) — Enables the Rectangle Y Extent Register when true
- C0-1 & C1-1 (Command 0 and 1) — Outputs of the Command Register that set the mode of the State Machine (Vector mode, Rectangle mode, etc.)
- PIXELRD-0 (Pixel Read) — Notifies the State Machine to enable the Pixel Register for a read when true
- XADRRD-0 (X Address Read) — Enables the X0-1 – X10-1 and Y0-1 – Y4-1 Address Read Back latches when true
- FBCBUSY-1 (Frame Buffer Controller Busy) — True when the FBC is busy and cannot be interrupted
- YADRRD-0 (Y Address Read) — Enables the Y5-1 through Y10-1 Address Read Back latches when true
- PA1-1 – PA4-1 (Processor Address 1 through 4) — Buffered Address information from the Terminal Control board's processor
- AD0-1 – AD15-1 (Address/Data Bus) — The Processor Address/Data Bus from the Terminal Control board
- DDARD-0 (DDA Read) — Enables FBC internal read registers when true
- DDAWR-0 (DDA Write) — Enables FBC internal write registers when true
- ADDCLK-1 (Address Clock), DDACLK-1 (DDA Clock), & SRCLK-1 (Shift Register Clock) — Clock outputs of the State Machine, used by the FBC
- XLD-1 (X Load) — Loads the X registers in the FBC
- YUPEN-0 (Y Up Enable) — Enables the Y registers in the FBC
- BCLK-1 (Bus Clock) — Bus clock signal from the Terminal Control board
- PIX-0 (Pixel) — Enables the Pixel Register when true
- RAS-0 (Row Address Strobe) — Strobes the row address into the RAMs; used by the FBC circuitry to load the Address Latches
- IOADREN-0 (I/O Address Enable) — Enables the output of the Address Latches when true
- PCS0-0 (Peripheral Chip Select 0) — Goes true whenever an I/O Read or Write to any Display Control board register occurs
- FBCCMD-0 (Frame Buffer Controller Command) — Enables the Command Register when true

Cursor (NEWDC-19 and 20)

This circuitry controls the crosshair cursor with the following functional blocks:

X and Y Address Latches. The X and Y Address Latches (U472 and U475, respectively) latch the position where the crosshair cursor is to be moved. These addresses come from the Processor on the Terminal Control board, via PD0-1 – PD9-1 (Processor Data 0 through 9). XCURSWR-0 (X Cursor Write) latches the X address and YCURSWR-0 (Y Cursor Write) latches the Y address.

X Address Counters. The X Address Counters (U281, U276, and U275) use DCLKB-0 (Display Clock B) and DCBLANK-0 (Display Control Blank) to provide the count for the X crosshair address. The Vertical Control Logic on the Display Control board supplies the Y count.

ECL X Address. U365, U362, and U361 convert the X address and the output of the Y Address Comparator from TTL levels to ECL levels.

X and Y Address Comparators. The X Address Comparator (U722 and U721) and the Y Address Comparator (U471) compare the position where the crosshair cursor is to be moved to the count for the appropriate axis.

The Y comparator compares the Y address to the count from the Vertical Control Logic on V0-1 – V9-1 (Vertical 0 through 9). When the Y comparison is equal, the output of the comparator forces the output of the X comparator to go true.

The X comparator compares the X address to the count generated by the X Address Counters. When the comparison is equal and DCBLANK-0 (Display Control Blank) is false, CURON-0 (Cursor On) goes true.

186 Pixel Read Back Latches (NEWDC-9)

U411 and U412 latch pixel data from the Frame Buffer to be read by the Processor. LTCH86-1 (Latch 80186) latches the data and PIXELRD-1 (Pixel Read) enables the outputs.

ALU Control Register (NEWDC-9)

The ALU Control Register (U415) sets the Pixel ALU for the correct mode needed by the vector generating circuitry when doing pixel operations. ALUWR-0 (ALU Write), ALURD-0 (ALU Read), and the data on D0-1 – D7-1 (Data 0 through 7) determine the mode.

Visibility and Write Mask Select Register (NEWDC-13)

The Visibility and Write Mask Select register is part of the ALU Control Register and uses the upper 8 bits of the Processor data (PD8-1 – PD15-1) to determine which pixels in a nibble will be visible (VIS0-1 – VIS3-1) and to enable the correct write control multiplexer.

FBI Pixel Data Path (NEWDC-9)

The Pixel Data Path contains the Pixel ALU and four buffers. Buffers U405 and U401 buffer pixel data to/from the 186 Pixel Read Back Latches.

The Pixel ALU performs arithmetic operations on the outputs of U405 and U401 and sends the results to the Frame Buffer via buffers U205 and U206. The ALU Control Register sets the mode of the ALU.

Table 4-1 (previously presented) shows the ALU modes and the ALU Control Register inputs necessary to set these modes. In the table, D0-1 – D5-1 (Data 0 through 5) are ALU Control Register Inputs, F is the Pixel ALU output, A is the ALU input from the 186 Pixel Read Back Latches, and B is the ALU input from the 1 of 4 Write Mask Selector.

Horizontal & Vertical Counters and Control Logic (NEWDC-10)

The Horizontal and Vertical Counters use CNTRCLK-1 (Counter Clock) to generate the following signals:

- HSYNC-0 (Horizontal Synchronization)
- OVLYLDCLK-1 (Overlay Load Clock)
- SCRNTIM-0 (Screen Timing)
- IOADREN-0 (I/O Address Enable)
- RFSHREQ-0 (Refresh Request)
- VSYNC-0 (Vertical Synchronization)
- VBLANK-0 (Vertical Blanking)
- HBLANK-0 (Horizontal Blanking)

U456 and U461 generate the vertical control signals and U465 and U462 generate the horizontal control signals. U455 and U452 use the output of the vertical control to produce the refresh address for the Display Memory.

Composite Sync/Blank Delay (NEWDC-15)

This logic delays VSYNC-0 (Vertical Synchronization), HSYNC-0 (Horizontal Synchronization), and VBLANK-0 (Vertical Blanking) to create the following:

- DCSYNC-0 (Display Composite Synchronization)
- DCBLANK-0 (Display Composite Blanking)

Display Memory Controller (NEWDC-14)

The Display Memory Control controls memory read cycles (performed by the Processor) and memory write cycles (performed by the Vector Generator circuitry) to the Display Memory.

The Display Memory Control circuitry uses the following inputs:

- RDMWR-0 (Read/Modify/Write) — When true, causes the state machine to perform a read/modify/write to Display Memory.
- RFSHREQ-0 (Refresh Request) — When true, causes the state machine to perform a refresh.
- IOADREN-0 (I/O Address Enable) — When true, allows the Vector Generator circuitry to address the Display Memory; when false, the address to the Display Memory is the refresh address.
- SCRNTIM-0 (Screen Timing) — When true, signifies that the address on the Address bus is for a refresh.
- PIXELRD-0 (Pixel Read) — Indicates that the Processor is requesting a Display Memory read cycle; also enables the acknowledge back to the Processor.
- Y10-1 (Y Address 10) — The most significant bit of the Y address; if true with RDMWR-0, a memory cycle will not occur. (This is to keep all writes to the Display Memory in a 1024 × 1024 bit map space.)
- X10-1 (X Address 10) — The most significant bit of the X address; if true with RDMWR-0, a memory cycle will not occur. (This is to keep all writes to the Display Memory in a 1024 × 1024 bit map space.)
- ALURD-0 (ALU Read) — When true, creates ALUACC-1 (ALU Access) to the State Machine.
- ALUWR-0 (ALU Write) — When true, creates ALUACC-1 (ALU Access) to the State Machine.
- OVLYCLK-1 (Overlay Clock) — Latches the next line address for the Alpha Overlay.
- DDACLK-1 (DDA Clock) — Used by the state machine to synchronize the memory cycle to the refresh cycles.
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock).
- RESET-0 (Reset) — System reset.
- IMAPWR-0 (Index Map Write) — Write strobe to the Index Map.
- CMAPWR-0 (Color Map Write) — Write strobe to the Color Map.
- BCLK-1 (Bus Clock) — Processor bus clock.
- IORDWR-1 (I/O Read/Write) — Signals an I/O read or write cycle.

The Display Memory Control has the following outputs:

- COL-0 (Column) — Selects the line for the Display Memory.
- RAS-0 (Row Address Strobe) — Strokes the row address into the Display Memory.
- CAS-0 (Column Address Strobe) — Strokes the column address into the Display Memory.
- TRQE-0 (Transfer/Queue Enable) — If true before RAS-0 goes true, signifies a register transfer or a refresh; if true after RAS-0 goes true, signifies a memory cycle. Always goes true when COL-0 goes true.
- MW-0 (Memory Write) — Strokes data into Display Memory.
- RAMSCLKEN-0 (RAM Shift Clock Enable) — Enable strobe for RAMSCLK-1.
- DDACLKEN-0 (DDA Clock Enable) — Enable strobe for DDACLK-1.
- EN86ACC-0 (Enable 80186 Access) — Acknowledge signal to the Processor; also used for gating read/write strobes into the I/O registers.
- LTCH86-1 (Latch 80186) — Used to latch display data for a Processor read of the Display Memory.
- IMAPWR-1 (Index Map Write).
- CMAPWR-1 (Color Map Write).

Address MUX and Driver (NEWDC-11)

The Address MUX and Driver multiplexes the frame buffer address into the correct row address for the Display Memory.

RAM Bank Select Logic (NEWDC-11)

The RAM Bank Select Logic decodes the two most significant bits of the frame buffer address (FB18-1 & FB19-1), IOADREN-0 (I/O Address Enable), RAS-0 (Row Address Strobe), and CAS-0 (Column Address Strobe) to gate the following control signals for each RAM bank:

- CAS0-0 – CAS2-0 (Column Address Strobes 0, 1, and 2)
- RAS0-0 – RAS2-0 (Row Address Strobes 0, 1, and 2)
- SRCLK0-1 – SRCLK2-1 (Shift Register Clocks 0, 1, and 2)
- SOE0-0 – SOE2-0 (Shift Output Enables, 0, 1, and 2)

1 of 4 Write Select (NEWDC-13)

The 1 of 4 Write Select uses the two least significant bits (FB0-1 & FB1-1) to determine which pixel of the four pixel nibble from the Display Memory should be written.

Write Control Logic (NEWDC-13)

The multiplexers of the Write Control Logic (U306, U311, U305, and U301) produce the Write Enable signals for the correct bank of RAM in the Display Memory (WEA0-1 – WEA3-1, WEB0-1 – WEB3-1, WEC0-1 – WEC3-1, and WED0-1 – WED3-1).

Display Memory (NEWDC-12)

The Display Memory (Frame Buffer) contains 12 41264-15 high-speed, dual-port, 65536 × 4-bit, random-access video RAMs. Each bit plane contains three RAMs as follows:

- Plane 0 — U121, U122, and U125
- Plane 1 — U131, U132, and U135
- Plane 2 — U21, U22, and U25
- Plane 3 — U31, U32, and U35

The display screen is divided into 3 areas. Four RAMs in the Display Memory serve each area (refer back to Figure 4-8). The rows of RAMs shown for each bit plane on the schematic correspond to the 3 areas of the screen shown in Figure 4-8.

Alpha Overlay Circuitry

The Alpha Overlay circuitry allows the alphanumeric characters and the background of the dialog area to overlay the graphics display.

Alpha RAM Address Generator (NEWDC-1). The Alpha RAM Address Generator generates the address for the Alpha RAM during display refresh and Processor read/write cycles. During display refresh cycles, OVLYLDCLK-1 (Overlay Load Clock) latches the row address (V9-1 through V4-1 — Vertical 9 through 4) into U751 at the beginning of each line refresh. At the same time, the character line address (V3-1 through V0-1 — Vertical 3 through 0) is latched into U752. (The character line address goes to the Font ROMs to specify which of the 16 character cell lines is being refreshed.) Valid column addresses are from 0 to 131, while valid row addresses are from 0 to 47.

Three multiplexers (U776, U781, and U782) select if the address source is either the latched address from U751 (for display refresh cycles) or the latched address from LA2-1 through LA14-1 (Latched Address 2 through 14 — for Processor I/O cycles). Another multiplexer (U785) performs the address translation required to put the extra four characters per line (the dialog area extends beyond the graphics area by four characters) into the Alpha Memory Array without using extra ROMs.

Alpha Memory Array (NEWDC-3). The Alpha Memory Array consists of two banks of 4K × 4 static RAMs. Since each character requires two bytes of information (one byte for the character and one byte for the attributes), the RAM can store 8000 characters and their attributes.

In RAM Bank 0, U772 and U771 contains the characters, while U766 and U765 contain the attributes. In RAM Bank 1, U762 and U761 contain the characters, and U756 and U755 contain the attributes.

RAM Bank 0 contains even memory addresses, while RAM Bank 1 contains odd addresses. This allows the Alpha RAM Control to read two adjacent characters each memory cycle for display refreshing. This leaves alternate memory cycles open for the Processor to access the RAM if necessary.

To accommodate the extra four characters at the end of the line (the four characters that the Dialog area can write that extend beyond the Graphics area), the Alpha RAM Address Generator maps these characters into unused memory space (see the previously presented Table 4-2).

Character and Attribute Output Registers (NEWDC-4). The four registers (U655, U656, U661, and U662) hold two characters and their attributes at one time. Each sixteen bit character word contains the following information:

- Bit 0 — The least significant bit of the character byte (FD0-1)
- Bit 1 — The second bit of the character byte (FD1-1)
- Bit 2 — The third bit of the character byte (FD2-1)
- Bit 3 — The fourth bit of the character byte (FD3-1)
- Bit 4 — The fifth bit of the character byte (FD4-1)
- Bit 5 — The sixth bit of the character byte (FD5-1)
- Bit 6 — The most significant bit of the character byte (FD6-1)
- Bit 7 — FD7-1 (Font Data 7). Selects alternate character set if true
- Bit 8 — ALTCOL2-1 (Alternate Color 2). Used with ALTCOL1-1 and ALTCOL0-1 to select one of eight Dialog area foreground/background color pairs
- Bit 9 — ALTCOL1-1 (Alternate Color 1)
- Bit A — ALTCOL0-1 (Alternate Color 0)
- Bit B — UDL-1 (Underline)
- Bit C — BLINK-1 (Blink)
- Bit D — INV 1 (Inverse)
- Bit E — OPAQ-1 (Opaque)
- Bit F — CURSOR-1 (Cursor)

Alpha RAM Control (NEWDC-6). The Alpha RAM Control contains a state machine (PAL U555), a decoder (U556 and U551), a flip-flop (U632), and associated logic gates.

The state machine PAL controls the reads and writes to the Alpha Memory Array: controlling the memory cycle switching, generating the control signals for the Alpha RAM Data Transceiver/Latches, and generating ACK-0 (Acknowledge). All memory cycles are available to the Processor during horizontal and vertical retrace and when the Dialog area is disabled. The Processor can use alternate memory cycles during refresh.

The decoder provides directional control for the data to/from the Alpha RAM Data Transceiver/Latches and the Alpha Memory Array.

The flip-flop enables the output of the Character and Attribute Output Registers.

Alpha RAM Data Transceiver/Latches (NEWDC-7). The four latches (U672, U665, U666, and U671) hold data going to/from the Processor and the Alpha Memory Array. During Alpha RAM writes (IOWC-0 true), the decoder in the Alpha RAM Control drives Pin 1 of the latches low, allowing data to flow from the Processor Data Bus to the Alpha Memory Array. During Alpha RAM reads (IORC-0 true), the latches hold the data from the Alpha Memory Array until IORC-0 goes false.

Font ROMs (NEWDC-1). The Font ROMs (U651 and U652) contain the characters, with each character occupying a 7 × 9 cell in an 8 × 16 matrix. Character scanning begins with Scan Line 0 at the top of the cell and progresses line-by-line downward through the cell. Scan Lines 0, 1, 2, and 15 are blank for spacing between lines and the leftmost column is blank for spacing between characters. Descenders on lower case characters (y, j, etc.) use Scan Lines 12 through 14. The cursor and character underline are NOT contained in the Font ROMs.

The 12 bits of the incoming font address are the seven character bits (FD0-1 through FD6-1 — Font Data 0 through 6), four character line bits (CL0-1 through CL3-1 — Character Line 0 through 3), and the eighth bit of the character word, which selects the font.

THEORY OF OPERATION

Character Generator (NEWDC-2). The Character Generator generates two character attributes (underline and blink) and the cursor. U682 uses VSYNC-0 (Vertical Synchronization) to generate the 75% duty cycle clock that controls the blink rate. PAL U535 uses this clock signal plus the following inputs:

- UDL-1 (Underline) — Enables character underline
- BLINK-0 (Blink) — Sets the character blink function
- CURSOR-1 (Cursor) — Turns on the cursor
- CURBLNK-0 (Cursor Blink) — Sets the cursor to blink
- ENBLNK-0 (Enable Blink) — Enables all blinking functions
- FBISMCLK-1 (Frame Buffer Interface State Machine Clock) — Clocks the PAL
- DIALON-1 (Dialog On) — Enables the Dialog area
- CHLIN0-1 through CHLIN3-1 (Character Line 0 through 3) — Shows which scan line of a character cell is being displayed

The PAL has three outputs:

- The Pin 14 output turns on all of the pixels in an appropriate scan line for the cursor or an underline.
- The Pin 15 output enables the character output when the Dialog area is enabled and turns the characters on/off for character blinking.
- The Pin 16 output turns off the character/attribute outputs at the end of each line.

U531 uses INV-1 (Inverse) and CHARCLK-1 (Character Clock) to “reverse” Dialog area character and background colors.

Video Output Path (NEWDC-2). The output of the Font ROMs is an 8-pixel character pattern. The Video Output stage requires character pixels to be released four at a time, at twice the CHARCLK-1 (Character Clock) rate.

U635 (a dual 4-bit flip-flop) latches the 8-pixel character and releases the pixels four at a time. The two flip-flops in U635 are alternately clocked by CHARCLK-1. When CHARCLK-1 is true, the first four pixels are sent, and when CHARCLK-1 is false, the last four pixels go out. The Pin 14 output of PAL U535, in the Character Generator, turns on all outputs from U635 during a cursor or an underline.

The exclusive OR gates in U532 allow the Character Generator to “reverse” the character and background colors for an Inverse function.

Alpha Index Map (NEWDC-16)

The Index Map, like the color map, interprets the alpha data as an address into the Color Map. In this manner, the alpha data can assume one of eight colors.

The Alpha Overlay has only three attribute bits for alternate colors. These bits, combined with the pixel data, give a total of eight displayable colors at one time. The remaining attribute is the background color, and, when it is asserted, causes the background to be opaque in a color that is determined by the other three attribute bits.

Pixel Data Shift Registers (NEWDC-15)

U41, U42, U141, and U142 convert the four-pixel data from the Display Memory to one-pixel data for the pixel data pipeline.

Pixel Data Pipeline Registers (NEWDC-15)

U51 converts the outputs of the Pixel Data Shift Registers from TTL levels to ECL levels. U52 latches the outputs of U51, as well as CURON-0 and the output of Pin 14 of U61. U55 buffers the outputs of U52.

Pixel Data/Alpha Data Pipeline Register (NEWDC-15)

U61 latches the outputs of the Pixel Data Pipeline Registers, combined with the output address from the Index Map.

Attribute Generator (NEWDC-2)

U632 latches the character attributes for the character and background colors, as well as the opaque attribute. (Refer to the discussion of the Alpha Index Map for more information on these attributes.) CHARCLKD-1 (Character Clock Delayed) clocks the attributes in to U632, while DIALON-1 enables the outputs.

Alpha Data Shift Registers (NEWDC-16)

Shift register U242 combines the attribute data and the character data, while U151 converts the combined data from TTL levels to ECL levels for the Index Map.

186 Color Map Write Data Buffers (NEWDC-17)

U371, U366, and U372 buffer the data from PD0-1 – PD11-1 (Processor Data 0 through 11) and convert it from TTL to ECL levels.

Color Map (NEWDC-17)

Pixel data inputs to the Color Map (U72, U71, and U75) act as an address pointing to a specific 4-bit word. This 4-bit word (0 – 16) is the value of the percentage of the specific color corresponding to a pixel. U71 handles the red data, U72 handles green data, and U75 handles blue data. All three Color Map ICs see the same address, but can modify the intensity of the colors for that address separately.

186 Color Map Read Data Buffers (NEWDC-18)

U375, U382, U381, and U376 buffer the outputs of the Color Map and convert them to TTL levels for buffers U481 and U482. The Processor can read the output of these latches.

DAC (NEWDC-18)

The DAC (Digital-to-Analog-Converter) converts digital pixel data from the Color Map into analog red, green, and blue signals for the Display Module circuitry.

The following synchronization, blanking, and clock signals provide control for the DAC (U185):

- DACCLK-1 (Digital-Analog-Conversion Clock)
- DACSYNC-0 (Digital-Analog-Conversion Synchronization)
- DACBLANK-0 (Digital-Analog-Conversion Blanking)
- DACCUR-0 (Digital-Analog-Conversion Cursor)

VIDEO CONVERTER BOARD CIRCUIT DESCRIPTION**Introduction**

The Video Converter board amplifies, converts, and buffers the analog output of the Display Control board (Red, Green, and Blue) into a differential output for the Display Module and an external video output. The Video Converter consists of three identical three-stage amplifiers (one for each color).

Video Amplifiers (VIDCONV-1)**NOTE**

The following description describes the Red amplifier/converter; the other sections are identical except for component numbers.

The circuitry consists of three transistor amplifier stages and one operational amplifier.

Q211 amplifies the incoming signal by 2. R101 is the gain adjustment. Q110 and Q111 function together as a phase splitter for the differential output from the Video Converter to the Display. Q110 is the inverting amplifier of the pair. U121 buffers the external video output.

VSYNC and HSYNC Buffers (VIDCONV-1)

U181 buffers the VSYNC-1 and HSYNC-0 signals from the Display Control for the Display Module.

TERMINAL CONTROL CIRCUITRY

INTRODUCTION

The Terminal Control circuitry constructs or modifies images in digital form. It contains the system processor, system firmware, and system RAM. Figure 4-9 is a simplified block diagram of the Terminal Control board. The "Diagrams" section (Section 10) of this manual contains a detailed block diagram.

The Terminal Control board is the heart of the terminal. It contains the Processor, the interrupt and keyboard controllers, the host communications circuitry, and the peripheral interface circuitry.

The Low Voltage Power Supply connects directly to the Terminal Control board, which then supplies power to the other circuit boards.

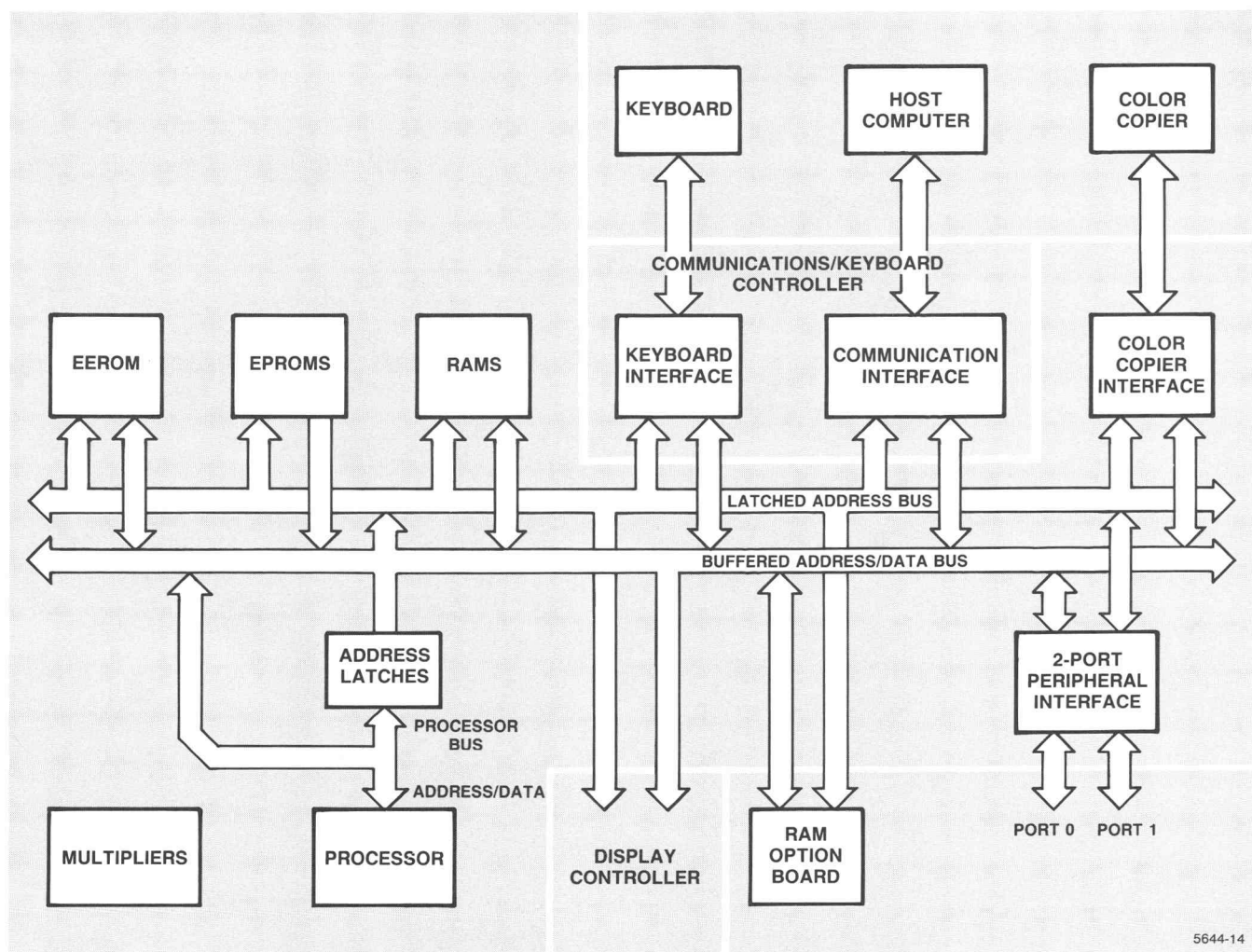


Figure 4-9. Terminal Control Board Simplified Block Diagram.

TERMINAL CONTROL BOARD CIRCUIT DESCRIPTION

Introduction

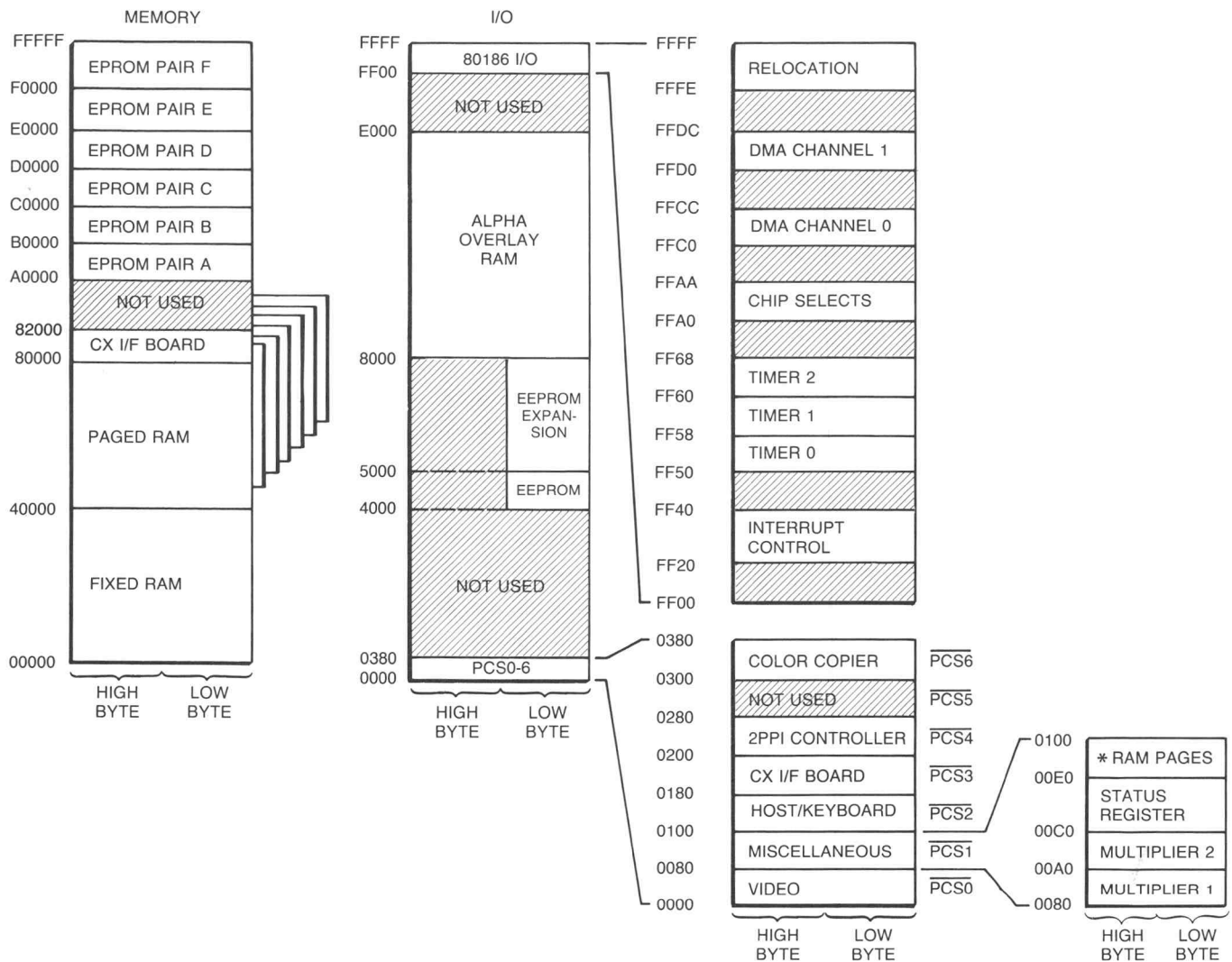
The Terminal Control circuitry consists of 35 functional blocks. The following text details the circuitry and operation of each block. Refer to the schematic diagrams (referenced in the descriptions) and the Terminal Control board timing diagrams in Section 10 on this manual while reading the descriptions.

Processor (TERMCTL-1)

The Processor is an Intel 80186¹ integrated microprocessor, operating at a frequency of 8 MHz. The 80186 contains an internal oscillator², bus arbiter, memory and peripheral I/O decoders, interrupt controller, DMA controller, and three timers. It uses a multiplexed address/data bus and has an address space of 1 Mbyte, with 64 kbyte of I/O space (Figure 4-10).

¹ Complete information on the 80186 can be found in the Intel Data Sheet *iaPX 186 High Integration 16-Bit Microprocessor*, October 1984.

² Not used. The Xtal Oscillator supplies the 16.00 MHz clock for the Processor.



* RAM PAGE REGISTER IS AT 00E0

5644-15A

Figure 4-10. Memory Map.

THEORY OF OPERATION

Reset Circuit (TERMCTL-1)

An RC network (R530, C860) provides an asynchronous reset signal to Pin 24 (RES) of the Processor and to J13, Pin 27C (RSTOUT-0), after a power-up or whenever the RESET button is pressed. The Processor uses the reset input signal to produce the system reset signal (Processor Pin 57).

Address Latches (TERMCTL-1)

U324, U430, and U530 demultiplex and latch address information from the Processor. The Processor supplies the latch enable signal (ALE/QS0-1) from Pin 61. Pin 1 of each latch is held low through R220 to chassis ground (R220 is present for automated testing only), permanently enabling the outputs of the latches.

The Address Latches latch and buffer the following signals:

- S0-0 – S2-0 (Status 0 through 2) — Become LS0-0 and LS1-0 (Latched Status 0 & 1), which clear the Wait State Generator and the Bus Timeout Circuit. S2-0 becomes M/I/O-1 (Memory or I/O), which tells all peripheral devices whether a memory or I/O cycle is in progress.
- AD0-1 – AD15-1 (Processor Address/Data Bus) and A16-1 – A19-1 (Processor Address 16 through 19) — AD0-1 through AD15-1 become LA0-1 through LA15-1 (Latched Address 0 through 15), and A16-1 through A19-1 become LA16-1 through LA19-1 (Latched Address 16 through 19). These signals convey address information to all peripheral devices.
- BHE-0 (Byte High Enable) — Becomes LBHE-0 (Latched Byte High Enable), which tells the Write Enable Logic to enable the high byte of RAM for a write cycle.

Data Buffers (TERMCTL-1)

U424 and U528 buffer data to/from the Processor and the System Data Bus. The DE (Data Enable) output of PAL U322, Pin 16, enables the buffers. DT/R-1 (Data Transmit/Receive) determines the direction of data flow. When DE is low and DT/R-1 is false, data flows from the System Data Bus to the Processor. When DE is low and DT/R-1 is true, data flows from the Processor to the System Data Bus.

The Data Buffers are disabled by U322 under the following conditions:

- A read or write to an address between 80000 and 9FFFF
- PCS3-0 is true (read or write to the EEROM)

U424 and U528 buffer the following signals:

- AD0-1 – AD15-1 (Processor Address/Data Bus)
- BAD0-1 – BAD15-1 (Buffered Address/Data Bus) — The Buffered Address/Data Bus is the System Data Bus from the peripheral devices.

Bus Timeout Circuit (TERMCTL-1)

The following signals enable/clear the bus timeout counter (U522):

- LS0-0 and LS1-0 (Latched Status 0 & 1) — During Processor HALTS and when no bus cycles are in process, these signals are both false, holding the counter cleared. During memory/I/O write cycles, S0-0 is true, and during memory/I/O read cycles, S1-0 is true. A Processor instruction fetch causes both signals to go true. Either or both signals becoming true enables the bus timeout counter.
- ALE/QS0-1 (Address Latch Enable/Queue Status 0) and RESET-1 (System Reset) — The bus timeout counter is held cleared when either or both of these signals are true (during a system reset or when the Address Latches are enabled).

When a memory or I/O read or write cycle is in process, the bus timeout counter CLEAR is released. This allows the timer to count VBLANK-0 (Vertical Blanking) pulses from the Display Control board. If the cycle is not completed before the count reaches sixteen, the counter overflows, generating an ACK-0 (Acknowledgement). If STAT7-1¹ is false at the same time, a Non-Maskable Interrupt (NMI) is sent to the Processor, a bus timeout occurs, ACK-0 goes true, and the cycle is terminated.

¹ STAT7-1 is externally maskable and is set low during Power-up Self-test.

Wait State Generator (TERMCTL-1)

The shift register (U220) generates timing signals for the EEROMs, which require 3 wait states for proper operation. The following signals hold the register cleared unless a read or write cycle is in progress:

- LS0-0 and LS1-0 (Latched Status 0 & 1) — During Processor HALTS and when no bus cycles are in process, these signals are both false, holding the counter cleared. During memory or I/O write cycles, S0-0 is true, and during memory or I/O read cycles, S1-0 is true. An interrupt acknowledge cause both signals to go true. When either or both signals are true, the shift register is enabled.
- ALE/QS0-1 (Address Latch Enable/Queue Status 0) and RESET-1 (System Reset) — The shift register is held cleared when either or both of these signals are true (during a system reset or when the Address Latches are enabled). During a long series of Processor code fetches, LS0-0 and LS1-0 remain true, causing an erroneous bus timeout. ALE-1 forces a reset of the bus timeout counter at least once per cycle.

RAMCLK-1 (RAM Clock) clocks the register when a cycle is in progress. WAIT3-1 (3 Wait States) qualifies the ACK-0 (Acknowledge) from the EEROM.

Interrupt Logic (TERMCTL-1)

The Processor has five levels of interrupts: NMI and INT 0 through INT 3. (NMI is discussed in the "Bus Timeout Circuit" description.) The assignments for the INT 0 through INT 3 interrupts are as follows:

- INT0-1 (Interrupt Level 0). This is the second highest level of interrupt (NMI is the highest) — generated by the host computer RS-232 receiver for communications use.
- INT1-1 (Interrupt Level 1). The third interrupt level — can be generated by the host computer as a lower-level interrupt (i.e., for error reporting), or by the keyboard.
- INT2-1 (Interrupt Level 2). The fourth interrupt level — generated by the 2PPI circuitry.
- INT3-1 (Interrupt Level 3). The lowest interrupt level — generated by the Color Copier Interface or by the Display Control during vertical blanking (VBLANK-0 true).

Control Signal Generation Logic (TERMCTL-1)

The Processor generates the actual control signals, while the Control Signal Generation Logic combines and buffers them.

The Control Signal Generation Logic creates the following signals:

- IOWC-0 (I/O Write Command) — When WR/QS1-0 (Write Strobe/Queue Status 1) is true and M/IO-1 (Memory or I/O) is false, IOWC-0 is true (an I/O write cycle is in progress).
- IORC-0 (I/O Read Command) — When RD/QSMD-0 (Read/Queue Status Memory Data) is true and M/IO-1 is false, IORC-0 is true (an I/O read cycle is in progress).
- MWRC-0 (Memory Write Command) — When WR/QS1-0 and M/IO-1 are both true, MWRC-0 is true (a memory write cycle is in progress).
- MRDC-0 (Memory Read Command) — When RD/QSMD-0 and M/IO-1 are both true, MRDC-0 is true (a memory read cycle is in progress).

U526 is permanently enabled through R610 (R610 is for ATE use only). U526 buffers the following processor signals:

- DEN-0 (Data Enable) — becomes BDEN-0 (Buffered Data Enable)
- DT/R-0 (Data Transmit/Receive) — becomes BDT/R-1 (Buffered Data Transmit/Receive)
- WR/QS1-0 (Write/Queue Status 1) — becomes BWR-0 (Buffered Write)
- RD/QSMD-0 (Read/Queue Status Memory Data) — becomes BRD-0 (Buffered Read)
- CLKOUT-1 (Clock Output) — becomes BCLK-1 (Buffered Clock) and RAMCLK-1 (RAM Clock)
- RESET-1 (Reset) — is buffered, but remains RESET-1¹
- PCS0-0 (Peripheral Chip Select 0) — becomes BPCS0-0 (Buffered Peripheral Chip Select 0)

The Processor generates PCS1-0, PCS2-0, PCS3-0, PCS4-0, and PCS6-0 (Peripheral Chip Selects 1, 2, 3, 4, and 6).

TMROUT0-1 (Processor Timer Output 0) is BELL-1 (Bell Tone).

¹ RESET-1 is also inverted by U422 to create RESET-0.

Address Decoding Logic (TERMCTL-2 & TERMCTL-5)

U292 and U322 are Programmed Array Logic circuits (PALs) used to decode memory and I/O addresses.

U322 uses the following signals to produce the Chip Selects for the EPROMs:

- LA13-1 – LA19-1 (Latched Address 13 through 19)
- M/IO-1 (Memory or I/O)
- STAT5-1 (Status 5)

U322 also decodes ARS-0 (Alpha RAM Select), PCS-3 (Peripheral Chip Select 3), DEN-0 (Data Enable), and the Pin 16 DE output (data enable for the Data Buffers).

U292 uses the following signals to decode the RAM Array addresses:

- LA1-1, LA5-1, LA6-1, LA14-1, LA15-1, LA18-1, and LA19-1 (Latched Address Bus)
- P0-1 – P2-1 (RAM Page Line 0, 1, & 2)
- PCS1-0 (Peripheral Chip Select 1)
- STAT5-1 (Status 5)
- M/IO-1 (Memory or I/O)

The 256K-1 and 1BNK-1 inputs (from the RAM Initialization Circuitry) are held low in the current memory configuration.

U292 also decodes MCS (Multiplier Chip Select), ECS (EEROM Chip Select), and SCS (Status Register Chip Select).

Refer to Appendix B of this manual for additional PAL information and equations.

EPROMs (TERMCTL-2)

The Terminal Control board has six pairs of EPROMs for system firmware:

- U130 and U330, pair “F”, address F0000 to FFFFF
- U140 and U340, pair “E”, address E0000 to EFFFF
- U142 and U342, pair “D”, address D0000 to DFFFF
- U150 and U350, pair “C”, address C0000 to CFFFF
- U152 and U352, pair “B”, address B0000 to BFFFF
- U162 and U132, pair “A”, address A0000 to AFFFF

The EPROMs with the U1XX series designations contain the high byte of memory, while the U3XX series contain the low byte.

The Chip Enable signals (from the Address Decoding Logic) select the EPROM to be read and LA1-1 through LA15-1 (Latched Address Bus) determine the data to be read. MRDC-0 goes true to enable EPROM output. (MRDC-0 enables all EPROMs when true, but only the EPROM whose chip select is also true will put data onto BAD0-1 through BAD15-1 (Buffered Address/Data Bus).

2 Port Peripheral Interface (2PPI) (TERMCTL-3)

U622 controls the communications to/from the two peripheral ports. Port 1 supports RS-232/C communications while Port 0 can support either RS-232/C or RS-422 communications.

U820 multiplexes the Port 0 input data from the RS-232 Receiver (U624) or the RS-422 Receiver (U724). STAT0-1 selects RS-232 or RS-422 communications for Port 0 (STAT0-1 true — RS-422, STAT0-1 false — RS-232).

RS-232 data from Port 1 goes directly from the RS-232 Receiver to U622.

Output data from U622 goes to the RS-232 Driver (U824) and the RS-422 Driver (U830). STAT-1 selects the driver to be used for Port 0 (STAT-1 true — RS-422, STAT-1 false — RS-232).

U622 produces a INT 2 level interrupt for 2PPI communications (refer to “Interrupt Logic” for further details).

The following signals provide data and control for U622:

- COMCLK-1 (Communications Clock) — 3.6864 MHz clock signal from the Communications Clock Circuit
- BAD0-1 – BAD7-1 (Buffered Address/Data Bus) — carries input/output data to/from the 2PPI Interface
- IORC-0 (I/O Read Command) and IOWC-0 (I/O Write Command) — indicate read or write cycle
- PCS4-0 (Peripheral Chip Select 4) — enables U622 when true
- LA1-1 & LA2-1 (Latched Address 1 & 2) — LA2-1, when true, selects Port 0; when false, selects Port 1. LA1-1, when true, enables the data register of the selected port; when false, enables the control register of the selected port.

DMA Logic. During a Direct Memory Access (DMA) using Port 0 in RS-422 configuration, U622 and the DMA Logic use DMAWRQ-1 (Direct Memory Access Write Request) and DMARRQ-1 (Direct Memory Access Read Request) to notify the Processor internal DMA controller when DMA writes/reads are to occur.

If LA1-1, LA2-1, PCS4-0, and IOWC-0 are all true (a write to the data register of U622 for Port 0), or if RESET-0 is true, U550 is held cleared (holding DMAWRQ-1 false).

Computer Port Interface (TERMCTL-4)

U462 is the controller for the host port communications circuitry and the Keyboard Interface. (For more information on the Keyboard Interface, refer to the “Keyboard Interface” circuit description.) U460 and U560 buffer the incoming RS-232 signals, while U464 drives the RS-232 outputs.

The following signals provide control and data transfer to/from U462:

- BAD0-1 – BAD7-1 (Buffered Address/Data Bus). Transfers data to/from U462
- LA1-1 – LA4-1 (Latched Address 1 – 4). Select U462 internal registers for read/write operations
- PCS2-0 (Peripheral Chip Select 2) and LA0-1 (Latched Address 0). When both are true, enable U462
- IORC-0 (IO Read Command) and IOWC-0 (IO Write Command). Signify whether a read or write operation is in progress

U462 generates a INT 0 level interrupt when data is received from the host. (For more information, refer to “Interrupt Logic”.)

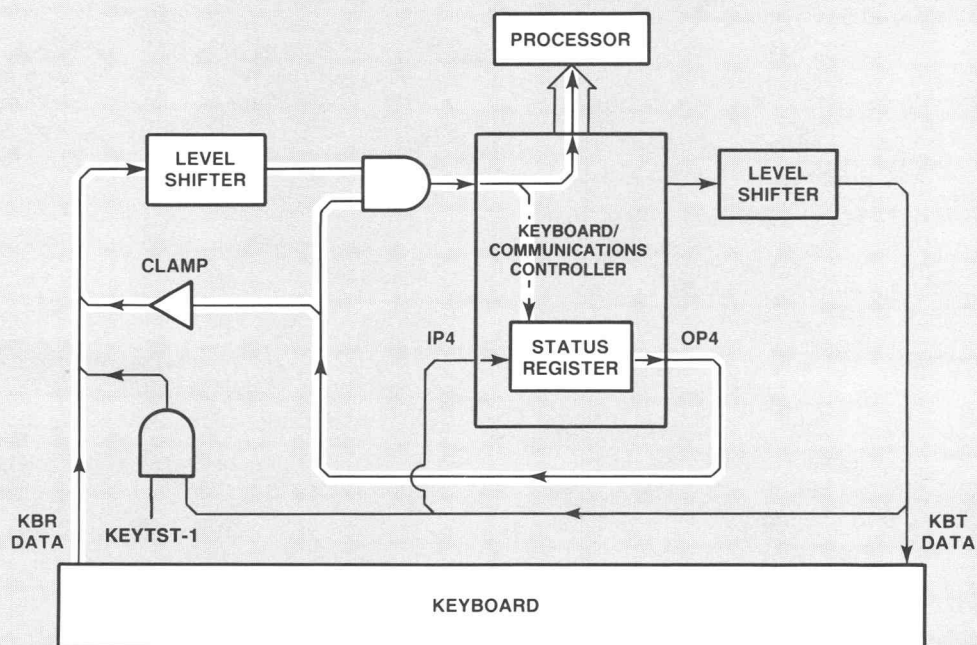
U462 can drive LED DS242 for Self-test error indication.

Communications Clock Circuit. The Communications Clock Circuit provides the 3.6864 MHz clock signal for U462 and U622.

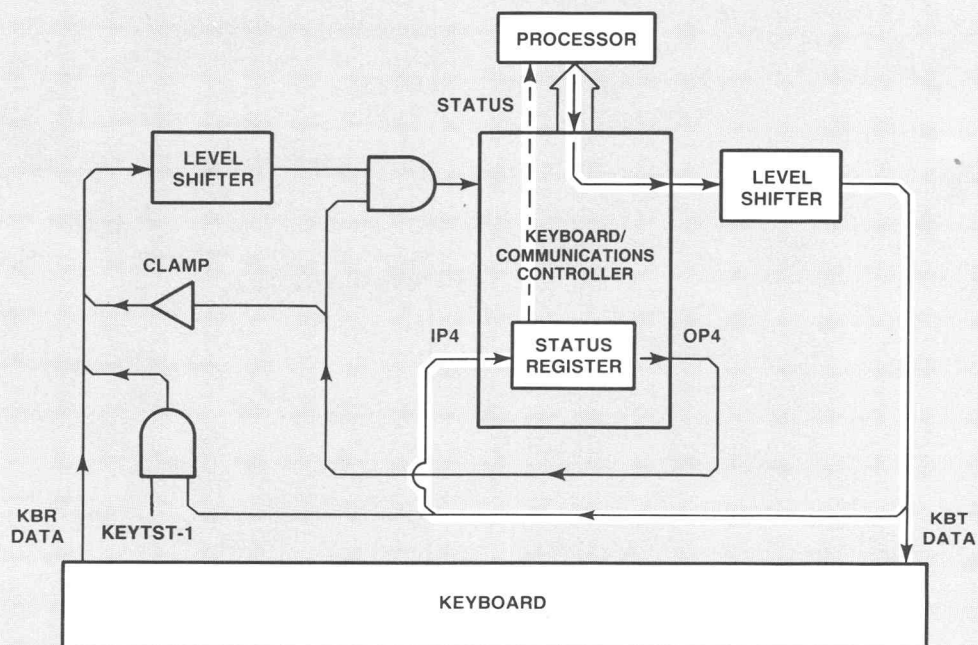
Keyboard Interface (TERMCTL-4)

U462 is the controller for the Keyboard Interface circuitry. Refer to Figure 4-11 (next page) for a functional diagram of the keyboard circuitry.

THEORY OF OPERATION



A. KEYBOARD INTERFACE, DURING RECEIVE CYCLE (FROM KEYBOARD).



B. KEYBOARD INTERFACE, DURING TRANSMIT CYCLE (TO KEYBOARD).

(4889)5644-16

Figure 4-11. Keyboard Interface.

Keyboard Signal Regeneration Circuit. The Keyboard Signal Regeneration Circuit contains level shifting circuitry that provides reliable data signal levels from the keyboard.

If U462 is not able to receive keyboard data on KBRDATA-1 (Keyboard Receive Data), the Keyboard Signal Regeneration Circuit can ground KBRDATA-1 (Keyboard Receive Data). This provides flagging that the keyboard can use to stop transmission of data when buffers are full.

KEYTST-1 (Key Test) provides a loopback path for transmitted signals for Self-test. When KEYTST-1 is true, transmitted data is duplicated on the receiving input of U462.

U666 buffers the output data to the keyboard.

Bell Circuit (TERMCTL-3)

NOTE

The Bell Circuit is not presently used.

A 910 Hz tone from internal timer 0 of the Processor provides the bell sound. STAT3-1 (Status 3) from the Status Register switches the "bell". An RC network (R632 and C534) give the tone a more true "bell" sound. Q630 is the switch and Q634 drives the speaker.

Color Copier Interface (TERMCTL-4)

U450 is the controller for the Color Copier Interface. The mode of operation U450 uses allows three groups of eight lines each for input/output (PA0 – PA7, PB0 – PB7, PC0 – PC7 on the schematic). The PA group is the output to the copier and the PB group is the control inputs. The PC group consists of an input (CACK-0 — Copier Acknowledge) and the following outputs:

- The enable to the Strobe Generation Circuit
- The signal to light LED DS244, used for Self-test error reporting
- COPINT-1 (Copier Interrupt) — a INT 3 level interrupt (for more information, refer to the "Interrupt Logic" circuit description in this section)
- INPRIME-0 (Input Prime) — notifies the copier that the interface is ready for operation
- KEYTST-1 (Key Test) — Self-test signal that allows the keyboard circuitry to test character transmission and reception without using the actual keyboard key circuitry

U450 uses the following input signals:

- LA1-1 & LA2-1 (Latched Address 1 & 2) — Determine which of the three ports of U450 is being addressed
- BAD0-1 – BAD7-1 (Buffered Address/Data Bus) — Carries copy pixel data to the interface circuitry
- IORC-0 & IOWC-0 (I/O Read Command and I/O Write Command) — Signify whether a read or write cycle is in progress
- RESET-1 (System Reset) — Resets U450 to power-up defaults
- LA0-1 & PCS6-0 (Latched Address 0 and Peripheral Chip Select 6) — Enables U450 when PCS6-0 is true and LA0-1 is false

U440 buffers the following input signals from the color copier before they go to U450:

- SELECT-1 (Select) — When true, indicates a hard copy unit is present.
- IR/SO-1 (Image Relationship/Serial Output) — Specifies image/medium relationship of color copier. In response to a STATUS command, sends a serial copier status report.
- FAULT-0 (Fault) — when true, indicates an error. Used in conjunction with BUSY-1 (Refer to Table 4-3).
- BUSY-1 (Copier Busy) — Hard copy unit is busy. Used in conjunction with FAULT-0 (Refer to Table 4-3).
- CACK-0 (Copier Acknowledge) — Copier acknowledges that it has received a COPY command.

Table 4-3

BUSY-0 AND FAULT-0 DEFINITIONS

Status	FAULT-0	BUSY-1	Description
Idle	1	0	Copier ready for data
Busy	1	1	Copier not ready — buffer full
Fault	0	0	Unexpected transmission or incorrect header
Hard Fault	0	1	Copier error — requires operator intervention

STEST-0 (Self-test) notifies U450 that the Self-test program has been initiated (S666 has been pressed). STEST-0 is also available at J13, Pin 15B, to notify logic external to the Terminal Control board that Self-test has been initiated.

U442 buffers the outputs of U450 before they go to the color copier.

THEORY OF OPERATION

Strobe Generation Circuit. The Strobe Generation Circuit consists of two monostable multivibrators that perform the following tasks:

- U654A and its associated circuitry holds STROBE-0 false for 1.1 μ s to allow output data to the color copier to stabilize.
- U654B and its associated circuitry drives STROBE-0 true for 2.9 μ s to strobe the output data into the color copier.

U440 is also used to buffer S0-0 – S2-0 (Status 0 through 2, from the Processor). These signals become BS0-0 – BS2-0 (Buffered Status 0 through 2) for use by the RAM Controller Circuitry and the Display Control board.

RAMs and RAM Controller Circuitry (TERMCTL-5 & TERMCTL-6)

The Terminal Control board has two banks of sixteen 64K RAMs each. U380 is an Intel 8208 fully integrated dynamic RAM controller that automatically refreshes these RAMs. The controller also contains internal data buffers that allow it to output data directly to the RAMs.

The Terminal Control board RAMs use an addressing concept called “bank-interleaving”. The address lines of the RAMs are arranged so that successive memory addresses (on word boundaries) are assigned to alternating banks of RAM. This allows faster operation as the time necessary to pre-charge the RAMs in one bank occurs at the same point as the access time for the other bank (one bank is pre-charged while the other is being accessed). As an example, address 00000 is physically located in the first word of Bank 0, while address 00002 is in the first word of Bank 1. (i.e., sequential addresses alternate between banks.)

U380 uses the following input signals:

- LA2-1 – LA17-1 (Latched Address 2 through 17) — Contain the address information for the RAMs.
- BS (Bank Select) and PE (Port Enable from U292 in the Address Decoding circuit) — Used to select the port and bank as needed.
- AL8 and AH8 (Address Low, bit 8 and Address High, Bit 8 from U292 in the Address Decoding circuit) — High bits of the address for each bank.
- BS0-0 – BS2-0 (Buffered Status 0 through 2) — BS0-0 is true during write memory requests and BS1-0 is true during read memory requests. BS2-0 is false after a RESET to configure U380 to accept the STATUS inputs from the Processor as valid (as opposed to bus commands).
- RAMCLK-1 (RAM Clock) — Clock signal for U380.
- PDI (Program Data Input) — Nine serial data bits from the RAM Initialization Logic.

The outputs of the RAM Controller are:

- AO0-1 – AO8-1 (Address Out, Bits 0 through 8) — Current RAM address.
- RAS0-0 & RAS1-0 (Row Address Strobe 0 and 1) — Row select signal for RAM refreshing and access latching.
- CAS0-0 & CAS1-0 (Column Address Strobe 0 and 1) — Column select signal for RAM access latching.
- WE (Write Enable) — Combines with outputs from the Write Enable Logic to create WEH-0 (Write Enable High Byte) and WEL-0 (Write Enable Low Byte).

RAM Initialization Circuit. The RAM Initialization Circuit initializes the RAM Controller (U380) at power-up. Pin 25 (WE) of U380 toggles nine times at power-up, clocking nine bits of serial data from shift register U190 of the RAM Initialization Circuit to U380. The connections on the inputs of U190 determine the values of the nine data bits.

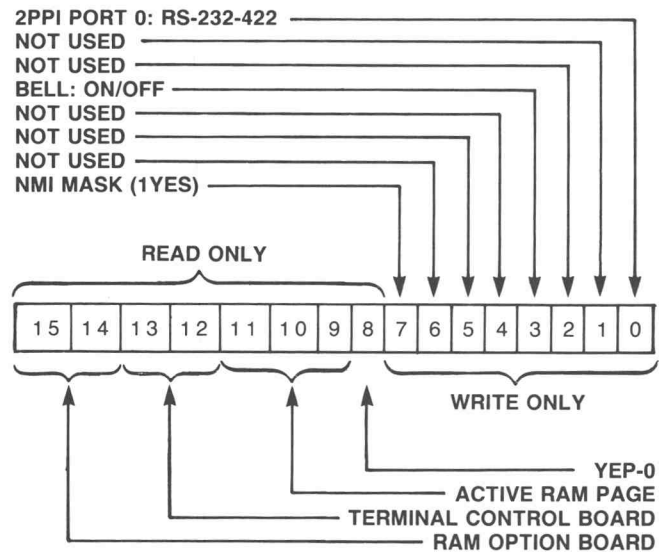
Write Enable Logic. The Write Enable Logic latches LA0-1 (Latched Address 0) and LBHE-0 (Latched Byte High Enable) to ensure that memory writes to the RAM are completed (the write time of the RAM is longer than the Processor cycle, allowing LA0-1 and LBHE-0 become invalid before the write is complete). The outputs of the latching flip-flop (U280) qualify the WE (Write Enable) signal from the RAM Controller and create WEL-0 (Write Enable Low Byte) and WEH-0 (Write Enable High Byte). LOWRAMACK-0 (Low RAM Acknowledge) clocks the flip-flops to latch LA0-1 and LBHE-0.

RAM Data Buffers. The RAM Data Buffers buffer data to/from the RAMs. When BDT/R-1 (Buffered Data Transmit/Receive) is true, data flow through U492 and U490 is from the Buffered Address/Data Bus to the RAMs; when false, from the RAMs to the Bus. The output of U282 in the Ready Circuit enables the buffers when BDEN-0 (Buffered Data Enable) and the PE (Port Enable) output from Address Decoder PAL U292 are both true.

Status Register (TERMCTL-5)

The Status Register, U392, provides circuitry for controlling and monitoring various functions of the Terminal Control board. The location of the register in memory is I/O Address 00C0.

The high byte of the register (BAD12-1 – BAD15-1) can be read but not written. The low byte (BAD8-1 – BAD11-1) can be written but not read. Figure 4-12 shows the definitions of the Status Register bits, Table 4-4 gives the code for interpreting Bits 12 and 13 (RAM configuration), and Table 4-5 decodes Bits 14 and 15 for the RAM Option board (if present).



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Figure 4-12. Status Register Bit Definitions.

Table 4-4
RAM CONFIGURATION BITS

Bit 13	Bit 12	Configuration
0	0	2 banks 64K RAMs — 256K bytes total (standard configuration)
0	1	Not used
1	0	2 banks 256K RAMs — 1 Mbyte total (Pages 0, 1, and 2)
1	1	1 bank 256K RAMs — 512K bytes total (Page 0)

Table 4-5
RAM OPTION BOARD RAM CONFIGURATION

Bit 15	Bit 14	Configuration
0	0	1 Mbyte RAM present (Pages 3, 4, 5, and 6)
0	1	Not used
1	0	Not used
1	1	No RAM Option board present

THEORY OF OPERATION

At power-up, the write-only portion of the register has all bits set to 0. The read-only portion is as follows:

- Bit 8 is low if an option is connected to the Option Interface Bus
- Bits 9 – 11 show (in binary) the currently active RAM page (Bit 11 is the MSB)
- Bits 12 – 15 show the RAM configuration for the Terminal Control and RAM Option boards as given in Tables 4-4 and 4-5

Input information for U392 comes from the following signals:

- P0-1 – P2-1 (Page 0 through Page 2)
- 2PAGE-0 & 4PAGE-0 (2 Pages of Memory Present and 4 Pages of Memory Present)
- YEP-0 (Yes, an Option is Present — is held true when an option is connected to the Option Interface Bus)

When IORC-0 (I/O Read Command) and the SCS output of Address Decoder PAL U292 are both true, U392 is enabled.

U390 in the Status Register latches selected address/data lines of the Buffered Address/Data Bus to create STAT0-1, STAT3-1, STAT5-1, and STAT7-1 (Status signals used for control). When IOWC-0 (I/O Write Command) and the SCS output of Address Decoder PAL U292 are both true, U390 latches the signals. RESET-0 clears the latch.

EEROM Circuitry (TERMCTL-5)

U382 is a 2K × 8 EEROM¹ used for non-volatile parameter storage. The EEROM requires three wait states, which the Processor supplies through WAIT3-1. The firmware must allow 30 ms after a write to the EEROM before another access, so an extra bit of the Color Copier Interface is used to allow the Processor to poll E2RDY-1 (the EEROM Ready signal).

The following signals control the EEROM:

- ECS (External Chip Select) output of Address Decoder PAL U292 — selects the EEROM
- IOWC-0 (I/O Write Command) — enables the EEROM for a write
- IORC-0 (I/O Read Command) — enables the EEROM to be read

EEROM Write Protection Circuit. Since the EEROM is subject to spurious write cycles during a power-up or power-down, the EEROM Write Protection Circuit holds the Chip Enable of U382 (Pin 20) high when the +5 Vdc power supply drops below +4 Vdc.

IOWC-0, IORC-0, the SCS and ECS outputs of Address Decoder PAL U292, WAIT3-1, and the output of the EEROM Write Protect Circuit are used by the Read Circuit to generate an ACK-0 (Acknowledge) for the EEROM and the Status Register (notify the Processor that the EEROM has completed a read or write command).

Multipliers (TERMCTL-7)

U110 and U120 Gate Arrays were developed to improve the transform speed of the 4111. The I/O address range for U110 is from 0080 to 0090, and the address for U120 is from 00A0 to 00B0. Normally, U110 is used for the X-axis and U120 for the Y-axis. However, during 90° rotation operations U120 handles X and U110 handles Y.

The Processor can read or write to the Multipliers with no wait states. If the Multipliers are busy, the acknowledge (ACK-0) to the Processor will not go true until the pending operation is completed.

The Multipliers use the following signals for control:

- LA1-1 – LA4-1 (Latched Address Bus 1 through 4) — The Multipliers decode these lines for internal register selection.
- MPCS-0 (Multiplier Chip Select) and LA5-1 (Latched Address Bus 5) — When LA5-1 is false and MPCS-0 is true, U120 is selected. U110 is selected when both are true.
- IORC-0 (I/O Read Command) and IOWC-0 (I/O Write Command) — Enable read or write operations, respectively.
- RESET-0 (System Reset) — When true, will stop multiplier operation and clear internal multiplier, decoder, latches and clock.

¹ May be expanded to 4K × 8 or 8K × 8 in future use.

Fan Power Circuit (TERMCTL-7)

The Terminal Control board provides + 12 Vdc for the cooling fan. C114 prevents transients from feeding back into the + 12 Vdc power, while CR120, CR124, and CR126 drop the voltage for quieter fan operation.

RAM OPTION BOARD CIRCUIT DESCRIPTION

Introduction

The RAM Option board increases the 4111 RAM memory from 256 Kbytes to 1.256 Mbytes. The RAM Option board is physically connected to the Display Control board, but is electrically part of the Terminal Control board (an extension of the Terminal Control board RAM).

The RAM Option board runs synchronously with the Processor, normally with no wait states. In the case of two sequential write cycles, one wait state is used.

Paged Memory. The RAM Option board exists in *page-switched* or *paged* Processor memory space at addresses 40000 to 7FFFF. Paging effectively increases memory space by allowing multiple banks of memory to reside in a single predefined block of address space.

The RAM Option board contains a Page Register that latches and decodes 8 bits of data to enable one of 256 possible memory pages (the RAM Option board contains four pages). Thus, all pages exist in the same memory space, but only the selected page can respond to the addresses.

Address Decoder (RAMOPT-1)

U110 is a Programmed Array Logic (PAL) IC that decodes the memory and I/O addresses for the RAM Option board. The PAL allows a memory access for addresses between 40000 and 7FFFF if the RAM Option board page has been selected.

U110 has the following inputs:

- LA0-1 – LA6-1, LA18-1 & LA19-1 (Latched Address Bus) — Contain address information
- BDEN-0 (Buffered Data Enable) — Goes true when the Data Buffers on the Terminal Control board are enabled
- IOWC-0 (I/O Write Command) — Identifies a write operation
- M/I/O-1 (Memory or I/O) — Identifies memory or I/O operation
- BDT/R-1 (Buffered Data Transmit/Receive) — Determines direction of data flow
- PCS-1 (Peripheral Chip Select 1) — Used by the Terminal Control board to select U110
- 1BNK (Pin-17) (1 Bank) — Identifies the amount of RAM memory present
- P0 – P2 (Pins 23, 14, and 13) (Port 0, 1, and 2) — Created from BAD0-1 – BAD2-1 (Buffered Address Bus 0, 1, and 2) — RAM Page register outputs

U110 has the following outputs:

- AH8 (Pin-22) (Address High Byte, Bit 8) and AL8 (Pin-21) (Address Low Byte, Bit 8) — High bits of the address
- BS (Pin-20) (Bank Select) — Selects the RAM bank
- PE (Pin-19) (Peripheral Enable) — Enables the RAM Controller
- BEN (Pin-18) (Buffer Enable) — Enables the Data Buffers through a 74ALS32
- RCK (Pin-15) (Register Clock) — Clocks the Page Register and creates ACK-0

RAM Page Register (RAMOPT-1)

The address of the RAM Page Register (U220) is 00E2 in I/O memory space. The register latches and decodes BAD0-1 – BAD7-1 (Buffered Address Bus) to enable the RAM pages as shown in Figure 4-13.

The status LED (DS110) can be used by Self-test for error reporting.

The RCK (RAM Clock) output of the Address Decoder PAL latches data into U220, while RESET-0 clears the register.

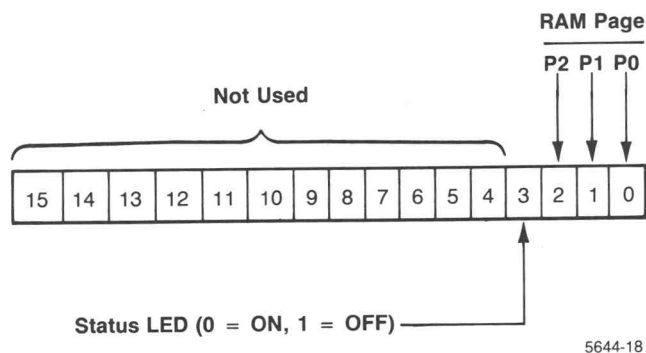


Figure 4-13. RAM Page Register Bit Definitions.

RAM Controller (RAMOPT-1 & RAMOPT-2)

Just as the Terminal Control board, the RAM Option board uses the Intel 8208 RAM Controller IC (U132). U132 is a fully integrated dynamic RAM controller that automatically refreshes the RAMs. The controller also contains internal data buffers that allow it to output data directly to the RAMs.

The RAM Option board uses the "bank-interleaving" address concept, exactly as the Terminal Control board does.

U132 uses the following input signals:

- LA2-1 – LA17-1 (Latched Address Bus) — Contain the address information for the RAMs.
- BS (Bank Select) and PE (Port Enable) — Selects the port and bank as needed.
- AL8 and AH8 (Address Low, bit 8 and Address High, Bit 8) — High bits of the address for each bank.
- BS0-0 – BS2-0 (Buffered Status 0 through 2) — BS0-0 is true during write memory requests and BS1-0 is true during read memory requests. BS2-0 is false after a RESET to configure U132 to accept the STATUS inputs from the Processor as valid (as opposed to bus commands).
- BCLK-1 (Bus Clock) — Clock signal for U132.
- PDI (Program Data Input) — Nine serial data bits from the RAM Initialization Logic.

The outputs of the RAM Controller are:

- AO0-1 – AO8-1 (Address Out, Bits 0 through 8) — Current RAM address
- RAS0-0 & RAS1-0 (Row Address Strobe 0 and 1) — Row select signal for RAM refreshing and access latching
- CAS0-0 & CAS1-0 (Column Address Strobe 0 and 1) — Column select signal for RAM access latching
- WE (Write Enable) — Combines with outputs from the Write Enable Logic to create WEH-0 (Write Enable High Byte) and WEL-0 (Write Enable Low Byte)

RAM Initialization Circuit. The RAM Initialization Circuit initializes the RAM Controller (U132) at power-up. Pin 25 (WE) of U132 toggles nine times at power-up, clocking nine bits of serial data from shift register U112 of the RAM Initialization Circuit to U132. The connections on the inputs of U112 determine the values of the nine data bits.

Write Enable Logic. The Write Enable Logic latches LA0-1 (Latched Address 0) and LBHE-0 (Latched Byte High Enable) to ensure that memory writes to the RAM are completed (the write time of the RAM is longer than the Processor cycle, allowing LA0-1 and LBHE-0 become invalid before the write is complete). The outputs of the latching flip-flop (U120) qualify the WE (Write Enable) signal from the RAM Controller and create WEL-0 (Write Enable Low Byte) and WEH-0 (Write Enable High Byte). RAMACK-0 (RAM Acknowledge) clocks the flip-flops to latch LA0-1 and LBHE-0.

RAM Data Buffers. The RAM Data Buffers buffer data to/from the RAMs. When BDT/R-1 (Buffered Data Transmit/Receive) is true, data flow through U210 and U212 is from the Buffered Address/Data Bus to the RAMs; when false, from the RAMs to the Bus. The BEN (Buffer Enable) output of the Address Decoder PAL enables the buffers.

CX INTERFACE BOARD CIRCUIT DESCRIPTION

This theory description starts with an overview of how the CX terminal operates with the Control Unit as part of 3270-type IBM system. This is followed by a general statement for each block on the CX Interface board.

NOTE

The CX Interface board is of a proprietary design. If this board requires component level repair, contact your nearest TEKTRONIX Service Center. They have access to more information (schematics, detailed theory, and parts lists) to help with repair of the board.

Overview

The CX-series terminals contain a special interface board and a coaxial connector. This allows the terminal to communicate with an IBM host via an IBM 3274 Control Unit. In this application, the user enters a Setup command to send all host I/O through the Coax Hostport (instead of the RS-232 port). The CX Interface board connects to the terminal's main processor via the main address and data bus. The interface board resides at address location 0180 to 018E in Processor I/O space. For more details about the terminal's interfacing process and connections, see Appendix C.

Figure 4-14 (next page) shows how the CX Interface board's command and status registers fit into the 80186 terminal processor's address map. There is 8K of screen buffer memory shared by the 80186 and 8X305. It is located at 80000h through 81FFFh in the 80186 address map (shown previously in Figure 4-10).

		HIGH BYTE	LOW BYTE	
18E			READ CURRENT FLAGS	READ WRITE
	PBA + 398		CLEAR ATTENTION REQUEST FLAGS	
18C			RESET CX BOARD	READ WRITE
	PBA + 396		SET COMMAND REQUEST FLAGS	
18A			RESERVED	
	PBA + 394		RESERVED	
188			RESERVED	
	PBA + 392		RESERVED	
186			R/W WORD 3	
	PBA + 390		R/W WORD 2	
184			R/W WORD 2	
	PBA + 388		R/W WORD 1	
182			R/W WORD 1	
	PBA + 386		MAIN STATUS	
180			COMMAND REGISTER	READ WRITE
	PBA + 384			
		D15	D8 D7	D0

NOTE: This address scheme mirrors at: 1A0-1AE, 1C0-1CE, 1E0-1EE

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Figure 4-14. CX Interface Board in Terminal Address Space.

Functional Description

Figure 4-15 shows how the IBM host passes data to and from the CX terminal. The host first sends commands and data from its front-end processor to a Control Unit via a "channel" or telecom line/modems to the Control Unit. The transmissions over this line are referred to as the "outbound" and "inbound" data streams and conform to the IBM 3270-series data stream format. Such data is encoded in EBCDIC¹, instead of ASCII, and enclosed in communications "packets." The Control Unit receives this data and converts it into the IBM coax code format, which it sends to the terminal. The CX Interface board then decodes this coax-formatted data and passes the information to the terminal's main processor.

In the IBM system, the terminal is a slave to the Control Unit (which assumes many of the intelligent functions of most modern RS-232 terminals). While the user is communicating with the host, the Control Unit is receiving host messages and passing them to the terminal. At the same time, the Control Unit is polling the terminal to see if the user wants to send a command or data back to the host.

¹ Extended Binary Coded Decimal Interchange Code.

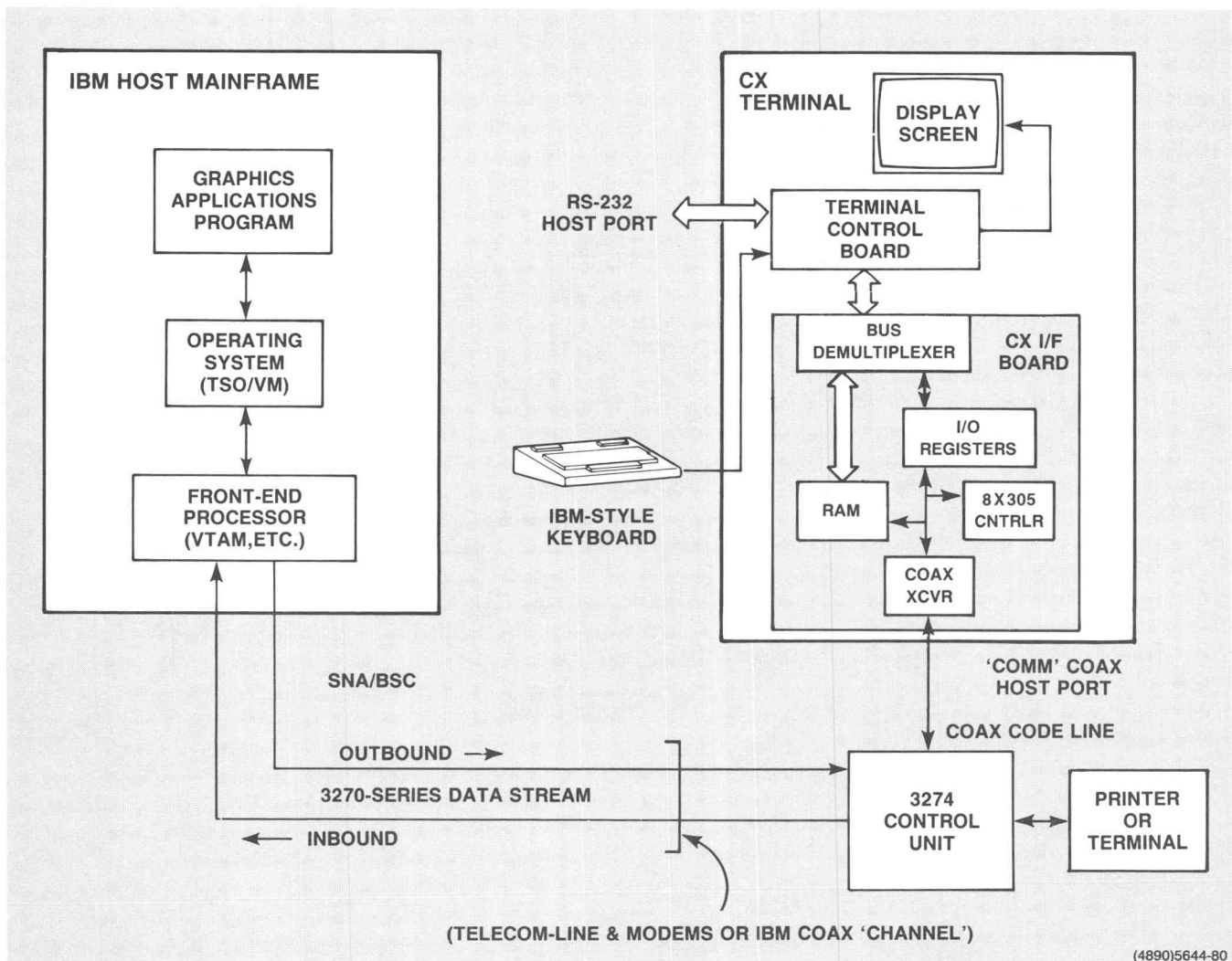


Figure 4-15. Block Diagram of CX Interface and IBM System.

THEORY OF OPERATION

When the user presses a key, the terminal sends a keyscan code in response to the next poll from the Control Unit. The Control Unit converts this code to a character code, using a special "coax code" character set (see NOTE). It sends the character code back to the terminal's "screen buffer." The terminal then displays on its screen any text that is stored in this screen buffer.

NOTE

This "character code" depends on which keyboard is installed. Each foreign language keyboard has its own unique set of character codes.

To send text onward to the host computer, the user presses the ENTER key. The Control Unit then reads text from the terminal's screen buffer and sends that text onward to the computer. In so doing, the Control Unit converts the characters from the coax code, stored in the terminal's screen buffer, into the EBCDIC code used by the host computer. The CX Interface board contains this screen buffer.

Circuit Block Descriptions

There are six functional blocks of circuitry that make up the CX Interface (see Figure 4-16):

- Microcontroller
- I/O Registers
- Dual-ported RAM
- Dual-ported RAM Control
- Coax Transceiver
- Bus Demultiplexer

The 8X305 microcontroller (on this board) manages the flow of data and commands between the I/O registers, dual-ported RAM, and coax transceiver.

The I/O registers are a set of 8-bit wide registers that pass command and status information back and forth from the main processor on the Terminal Control board to the 8X305 microcontroller.

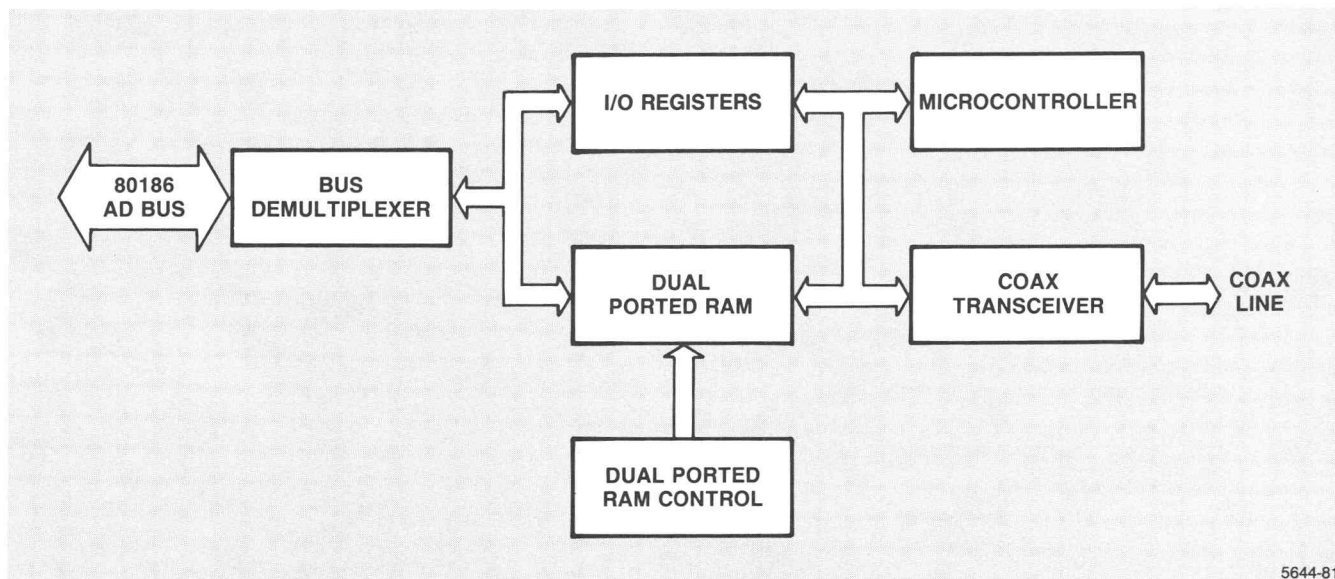


Figure 4-16. CX Interface Board Functional Block Diagram.

The dual-ported RAM is an 8K × 8-bit static RAM that is accessible to both the 80186 and 8X305. It stores the character codes, which are then read by the Terminal Control board and displayed on the screen.

The dual-ported RAM control consists primarily of the RAM Arbiter PAL and some other logic circuitry. The PAL generates the control signals that control access to the static RAM.

The coax transceiver passes the data to and from the coax connector (from the CX data bus). The primary elements of this block are a biphase transmitter and a biphase receiver. These chips connect to the coax connector via an isolation transformer.

The bus demultiplexer places address and data information from the 80186 on separate address and data busses.

Indicators

The CX Interface board has a green LED that lights when power is applied to the board. The LED is lit steadily when the board is idle, and blinks when the board is functioning in Control Unit Terminal (CUT) mode. The LED blinks rapidly in CUT mode. You can see the LED through the air vents in the right top side of the terminal's top cover.

Connectors

There are three connectors on the CX Interface board. They are a bus connector, a test connector, and a coaxial connector called COMM.

The bus connector is a 96-pin DIN connector that gives the CX Interface access to the CX4111's 80186 bus. It is on a small, break-off board that is connected to the CX Interface board by a 7" long, 50-conductor flex cable.

The test connector is a 60-pin connector used only for testing.

The COMM connector is on another smaller break-off board connected to the CX Interface board via a three-conductor flex cable. When installed in the CX4111, the COMM Connector is located in the bottom left quadrant of the CX4111 rear panel as viewed from the rear.

KEYBOARD CIRCUIT DESCRIPTION

For information regarding theory of operation, schematic diagrams, and replaceable parts for your specific keyboard, refer to the appropriate service manual. The three manuals are:

- The *4120 Series Serial Keyboard Service Manual* for the standard keyboard with thumbwheels.
- The *119-1989-00, 119-2315-00 Keyboards With Mouse Technical Data Manual* for the optional keyboard with the Joydisk.
- The *119-1990-00, 119-2307-00 CX Keyboards With Mouse Technical Data Manual* for the CX4111 keyboard.

TERMINAL LOW VOLTAGE POWER SUPPLY (TLVPS)

Introduction

The TLVPS is a continuous conduction flyback-type switching power supply that supplies the following voltages:

- + 12 Vdc
- - 12 Vdc
- + 5 Vdc
- - 5 Vdc

The TLVPS contains both overvoltage and overcurrent protection circuits.

The TLVPS circuitry can be divided into the following functional blocks:

- AC Power
- EMI Filtering
- Line Select
- Rectifier and Filter
- On Driver
- Switching Transistor
- Snubber
- Turn Off SCR
- Current Limit
- Holdoff
- Main Transformer
- Difference Amplifier
- Feedback Driver
- Over-voltage Protector
- Burp Circuit
- - 5.4 V Linear Regulator

Each of these blocks is discussed in this section.

AC Power (TLVPS-1)

The AC Power block consists of the ac plug, a fuse, and the power switch.

Power comes into the supply via a power cord connected to the ac plug. A 6 A fuse protects the TLVPS; the fuse is mounted on the circuit board and is not externally accessible. The power switch turns the supply on and off.

EMI Filters (TLVPS-1)

The EMI Filter block keeps high frequency noise (KHz range and up created by the switching of the supply) from getting back into the ac line. This filtering does not affect the 60Hz ac supply to the Rectifier and Filter block.

There are three inductor-capacitor EMI Filters:

- L6, which filters the Display Module's ac line
- L1, which filters the TLVPS ac line
- L5, which filters both

Line Select (TLVPS-1)

The Line Select consists of two switches. The setting of these switches enables the supply to run from either 120 or 230 Vac line voltages.

SW4 selects the GMA Display Module line voltage, while SW2 selects the operating voltage for the TLVPS. The setting of SW2 determines whether the diode bridge (CR1), in the Rectifier and Filter block, acts as a voltage doubler or a full-wave bridge.

Rectifier and Filter (TLVPS-1)

The Rectifier and Filter block rectifies the AC voltage to a high voltage DC signal (between 200 and 380 V). The Rectifier and Filter block consists of a diode bridge (CR1), two filter capacitors (C5 and C6), and a thermistor (RT1).

RT1 limits the surge current to C5 and C6 when the supply is first turned on. As RT1 heats during normal operation, its resistance lowers.

DS1 is a neon lamp that indicates when dangerous voltages are present at C5 and C6.

On Driver (TLVPS-1)

The On Driver functions as a “self-start” circuit. Current bleeding through R3 to Q1 and Q3 starts the supply. When Q1 turns on, driver Q3 and Switching Transistor Q5 turn on. The positive forward winding of T1 supplies regenerative turn-on gain.

The main function of the On Driver after start-up is to maintain the base voltage during the on time of the Switching Transistor. Q1 remains on until the Turn Off SCR shunts current away.

Switching Transistor (TLVPS-1)

Q5 chops the primary voltage, producing a square wave across the primary winding of T1.

Snubber (TLVPS-1)

The Snubber contains a capacitor (C14), four diodes (CR11, CR14, CR16, and CR17), and three resistors (R13, R14, and R45). The Snubber is in parallel with the Switching Transistor.

When Q5 is starting to turn off, a high voltage spike occurs. This spike is the result of energy stored in the primary leakage inductances. The Snubber draws current through C14 and CR14, attenuating the spike. When Q5 turns on, the resistors discharge C14.

Turn Off SCR (TLVPS-1)

The Turn Off SCR circuit actually contains two transistors (Q2 and Q4). These transistors are connected back-to-back to simulate an SCR. This circuit receives feedback from the current limit and the secondary circuits. The current shorts the base of Q5, causing it to turn off.

Current Limit (TLVPS-1)

R15 and R17 provide primary current limit. The base-emitter junction of Q6 senses voltage drop across these resistors and activates the Turn Off SCR.

Holdoff (TLVPS-1)

R6, R7, R10, C7, C8, CR5, and Q1 provide holdoff. When Q5 is on, Pin 7 of T1 goes negative, charging C7. Pin 5 of T1 goes positive, charging C8. When Q5 turns off, T1 flies back, making Pin 7 positive. The voltage across C7 discharges through R7, since R7 returns to ground. Q1 turns on before the transformer has emptied. This action produces a continuous conduction flyback switching power supply.

Main Transformer (TLVPS-1)

T1 has a flyback type of configuration. The primary winding stores energy during the on time and releases that energy to the secondary windings. The released is filtered to become the outputs.

THEORY OF OPERATION

Difference Amplifier (TLVPS-1)

The main element of the Difference Amplifier is U2. U2 is the heart of the feedback and regulation loop of the TLVPS.

A ripple regulation waveform is injected into Pin 4 of U2, via C25. The loop is set up as a simple ripple regulator with a controlled current turn off.

U2 has an internal reference supply on Pin 6. This reference voltage is divided down through R38 (the +5 V Adjust) and enters Pin 4 (the inverting output of the comparator). Pin 5 (the non-inverting input) is connected to the +5 V output via R36. The output of this comparator drives the Feedback Driver.

Feedback Driver (TLVPS-1)

Q10 conducts pulses through the control loop pulse transformer T2. The base of Q10 is connected to the outputs of both the Difference Amplifier and the Burp Circuit. Either of these circuits can send a pulse through T2 to the primary.

Over Voltage Protector (TLVPS-1)

SCR1, CR30, CR31, CR32, R40, R42, and R53 provide overvoltage protection. If the +5 V output rises above +5.6 V, CR30 conducts, triggering the gate of SCR1. This turns SCR1 on and sends pulses to T2 through CR32 and R53. These pulses cause the power supply to reduce its pulse width. Current to keep SCR1 on is provided by R41 and CR31.

Burp Circuit (TLVPS-1)

The Burp Circuit protects the secondary circuitry in the event of an overload or short circuit. The Burp Circuit becomes active when the +12 V output is pulled below 8 V, or when the +5 V output is pulled below +4.3 V. When the +12 V supply is below 8 V, the SCR action of Q8 and Q9 is off and C24 begins to be charged by Pin 11 of T1, via CR22. As C24 is charging, Q10 is held on, causing the supply to operate in the minimum pulse width mode. This reduces the output power to a small level. When C24 reaches 8 V, Q8 and Q9 fire, turning off Q10 and allowing the pulse width to increase. The supply then tries to run at full power, charging the outputs. If the +12 V output does not reach 8 V by the time that Q8 and Q9 turn off (the time constant of C24 and R27), the supply will return to minimum pulse width mode.

– 5.4 V Linear Regulation (TLVPS-1)

The –5.4 V output is a linear regulated output. U1-B is set up as a voltage reference, with U1-A as a difference amplifier and driver for Q7. The voltage drop across R28 and R37 provides the sensing for current limiting.

Section 5

CHECKS AND ADJUSTMENTS

INTRODUCTION

This section describes the checks and adjustments for the 4111 and CX4111 terminals. The Display Module is the main analog part of the terminal and is the focus of attention in this section. The only non-Display Module adjustment is for +5.1V and -5.4V on the Terminal's Low Voltage Power Supply (TLVPS) module.

The first part of this section lists the functional check procedures for the terminal. The remainder of the section deals with the adjustment procedures for the TLVPS and the two different Display Modules (GMA302 Display Module and 119-2387-00 Display Module).

FUNCTIONAL CHECK

The functional check procedures for the terminal consist of running the Diagnostic Self-test and using the Adjustment Self-test menus. You may also refer to either Section 3 (*Operating Information*) for further information about Self-test menus, or to Section 6 (*Maintenance*) for a listing of Self-test error codes.

To perform the functional check procedures, you will need a special test fixture; a loopback connector. Contact a service representative at your nearest TEKTRONIX Field Office for information about acquiring this test fixture.

4111 TERMINAL

The following procedure verifies operation of the terminal. *This procedure is the level of testing that is recommended by Tektronix, Inc., for customer acceptance testing or for testing the product after repair.*

1. Run the Diagnostic Self-test. (Press and hold both the SELF TEST and RESET buttons, then release the RESET button before releasing the SELF TEST button. When the bell sounds, press any character key.) The test takes approximately 4 to 6 minutes to run.
2. Call up the Adjustment Self-test menu. (Press and hold both the SELF TEST and RESET buttons, then release the RESET button before releasing the SELF TEST button. When the bell sounds, press Ctrl-C.) Press function key F1 to select the Processor board menu, then select the host port check routine by pressing F3.
 - a. Attach a loopback connector to the host RS-232 port.
 - b. Press the Space Bar. This checks the host port transmit, receive, control, and status lines, as well as communications at baud rates from 150 to 19.2 kbaud. If an error occurs, a message will be printed on the terminal screen. Refer to Section 6 of this manual for explanation of the error messages.
 - c. Remove the loopback connector.

CHECKS AND ADJUSTMENTS

3. Type Ctrl-C and press F2 to call up the display portion of the Adjustment Self-test menu. Perform the following checks:

NOTE

The right-most vertical line of the Grid pattern is not connected to the horizontal lines of the pattern.

- a. Press F1 to select the grid pattern. The pattern should be geometrically even, and the convergence should appear satisfactory.
 - b. Press F3 to select the gray scale pattern. The 16 shades of gray should vary from black to white.
 - c. Type Ctrl-E to exit from Self-test.
4. Enter Setup mode by pressing the Setup key. Enter the following command:

DAE^SPYES^CR

Press the Dialog key. The dialog area should now be visible and the "*" prompt should appear.

CAUTION

The command characters in Step 5 must be capitalized. To prevent entry errors, press the Caps Lock key to type these commands in upper-case.

5. Create a segment by entering the following commands:

E_CSO^SP1^CR
E_CMP^SP - 10^CR
E_CUR^SP1500^SP1000^SP3000^SP2500^CR
E_CMP^SP - 2^CR
E_CLP^SP1850^SP1250^CR
E_CLG^SP2250^SP2300^CR
E_CLG^SP2650^SP1250^CR
E_CLG^SP1650^SP1900^CR
E_CLG^SP2850^SP1900^CR
E_CLE^CR E_CSC^CR

The displayed segment should look like Figure 5-1 — a red star on a green background. When you page the screen, the segment should disappear for a moment, then repaint.

6. Using the segment just created, check the operation of the Zoom, Pan, and View keys.

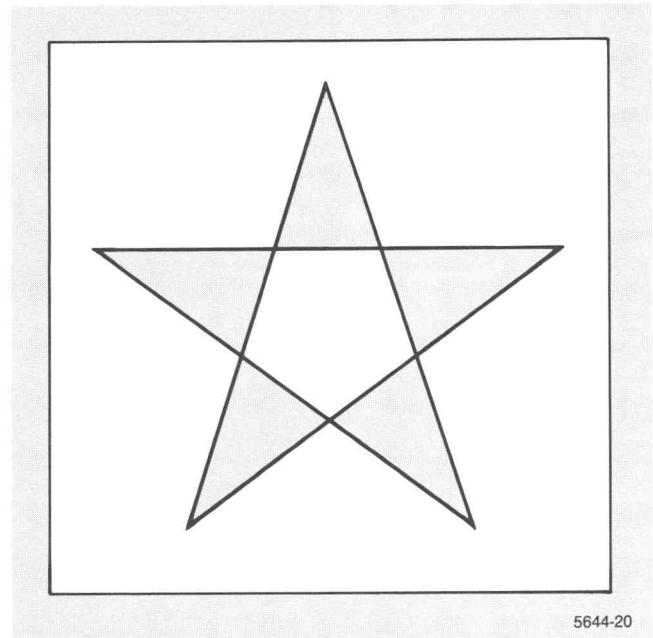


Figure 5-1. Segment.

2PPI

1. Call up the Adjustment Self-test menu. When the bell rings, press Ctrl-C to enter Adjustment Self-test. Press F1 to enter the Processor Board Menu, then press F4 or F5 (depending on the port to be tested).

2. Do the following:

- a. Connect the host port cable from the host port to the 2PPI port to be tested.

If an error occurs during the test, a message will be printed on the terminal screen. Refer to Section 6 of this manual for explanations of the error messages.

3. Remove the cable.

4. If a 4957 or 4958 tablet is connected to a 2PPI port, proceed with the following steps:

- a. Place the tablet's puck or stylus on the center of the tablet surface.

- b. Press F6 to run the tablet test.

- c. Enter the terminal port number that the tablet is connected to, then follow with a C_R .

- d. When the test is completed, a message will appear on the screen similar to the following:

```
Tablet test - Result = 4F
Tablet code - check = 2E2345413030
```

The "Tablet test" portion of the message is a hexadecimal code corresponding to the 8 bits shown in Tables 5-1 and 5-2. (Bit 7 is the most significant bit of the code.)

The "Code — check" portion of the message returns the checksum and version of the tablet ROMs.

Table 5-1**4957 TABLET TEST CODES**

Bit	High/Low (1 or 0)	Definition
0	1 (Pass)	Used for tablet ID code
1	1 (Pass)	Used for tablet ID code
2	1 (Pass) 0 (Fail)	RAM/ROM Check
3	1 (Pass) 0 (Fail)	Cursor on tablet Cursor not on tablet
4	1 (Pass)	Used in tablet ID code
5	0	Always 0 (Not used)
6	1 (Pass) 0 (Fail)	Total test
7	1 or 0	Odd parity bit

Table 5-2**4958 TABLET TEST CODES**

Bit	High/Low (1 or 0)	Definition
0	1	Always 1
1	1 (Pass) 0 (Fail)	Cursor connection — operating test
2	1 (Pass) 0 (Fail)	Digital memory test
3	1 (Pass) 0 (Fail)	Cursor on tablet Cursor off tablet
4	1	Always 1
5	0	Always 0
6	1 (Pass) 0 (Fail)	Total test
7	1 or 0	Odd parity bit

Color Graphics Copier Interface

1. Install the color copier loopback connector at the rear of the terminal.
2. Call up the Adjustment Self-test menu. When the bell sounds, press Ctrl-C. Press F1 to enter the Processor Board Menu and press F7. The test should pass without error. If an error occurs during the test, a message will be printed on the terminal screen. Refer to Section 6 of this manual for explanations of the error messages.

Display Memory

Call up the Adjustment Self-test menu. When the bell sounds, type Ctrl-C. Press F2 to select the Display menu and press function key F4 (color scale pattern). The grid pattern should contain 12 colors, black, white, and gray.

If a brief user application program is available, run it to verify operation.

CX4111 TERMINAL

The following procedure checks operation of a CX4111 terminal (with the CX Interface board installed). *This procedure is the level of testing that is recommended by Tektronix, Inc., for customer acceptance testing or for testing the product after repair.*

1. Perform the previous functional check procedures listed for the 4111 terminal.
2. Call up the Adjustment Self-test menu. (Press and hold both the SELF TEST and RESET buttons, then release the RESET button before releasing the SELF TEST button.) When the bell sounds, press Ctrl-C.) Press F3 to select the 4111 Coax Board test.

NOTE

The user should check that the terminal's coax cable is disconnected from the IBM 3274 Controller. Otherwise, the test could confuse the Controller.

The CX Interface board has an LED that is green. It blinks when the CX Interface board is in CUT (Control Unit Terminal) mode. During Self-test, the green LED goes through a sequence of blinking dimly and brightly.

3. If the CX Interface is installed, the following prompt will appear:

```
Coax Board Test
--
Disconnect Coax Cable Before Proceeding
--
Press Space Bar To Continue
```

4. If necessary, see Self-Test Error Messages in Section 6, *Maintenance* for descriptions of any error codes. Upon a successful completion of the 4111 Coax Board test, the following message appears:

```
Coax Board Test Complete
Selection
Function Key-Test Selection
^C 4111 Menu
^D Current Menu
^E End
*
```

ADJUSTMENTS

The adjustment procedures for the terminal pertain mostly to the Display Module; the only other adjustment is setting the +5.1V and -5.4V on the TLVPS module. Since two different types of displays can be used with the terminal, this section includes separate adjustment procedures for each of these Display Modules. You can easily recognize the earlier display (GMA302 Display Module) by its numerous circuit boards and more open chassis. The later version display (119-2387-00 Display Module) has a completely metal-enclosed chassis, fewer circuit boards, and an additional CONTRAST control on the terminal's front panel.

TERMINAL LOW VOLTAGE POWER SUPPLY**WARNING**

Lethal line voltages are present inside the TLVPS module. Use the adjustment holes (on the inner side panel) to make any adjustments to the + 5.1V and – 5.4V outputs.

For the following checks and adjustments use the terminal chassis for a ground reference:

+ 5.1 Volts

1. Check the + 5.1V level on the Terminal Control board at J11 (pin 10, 11, 12, or 13). The reading should be + 5.100 volts \pm 0.051 volts.
2. If needed, adjust the + 5.1V level (R38) on the TLVPS.

– 5.4 Volts

1. Check the – 5.4V level on the Terminal Control board at J11 (pin 1 or 2). The reading should be – 5.400 volts \pm 0.054 volts.
2. If needed, adjust the – 5.4V level (R49) on the TLVPS.

Checking + 12 Volts and – 12 Volts

The + 12V and – 12V voltages are not adjustable. These checks verify that the TLVPS module is operating properly.

1. Check the + 12V level on the Terminal Control board at J11 (pin 5). The reading should be + 12.00 volts \pm 1.200 volts.
2. Check the – 12V level on the Terminal Control board at J11 (pin 7). The reading should be – 12.00 volts \pm 1.200 volts.

GMA302 DISPLAY MODULE**WARNING**

The Service Adjustment Procedure can expose service personnel to voltage levels that are potentially lethal. To avoid a hazardous situation, all servicing should be done by authorized service personnel using proper servicing techniques and equipment.

The Display Module may need adjustment if the convergence or purity becomes unsatisfactory, or if repairs have been made. Use the following adjustment procedure only if your terminal has the GMA302 Display Module.

Tools Required

- Dual Trace Oscilloscope — Vertical: 100 mV/div, Time Base: 5 ns/div. TEKTRONIX Model 2236 or equivalent. Also required, 3 oscilloscope probes — Attenuation : 10:1, Resistance: 10 M Ω , Capacitance: 10 pF, Length: 1 meter. TEKTRONIX Model P6106 or equivalent.
- Digital Voltmeter — Range: 0 to 1000 VDC, Accuracy: 0.1%. TEKTRONIX DM501 or equivalent. Also required, high voltage probe — Range: 0 to 30 kV, Attenuation: 1000:1, Input Impedance: 1000 M Ω . Fluke Model 80K-40 or equivalent.
- Calibration Graticule (refer to the Accessories Parts List for part number)
- Photometer — TEKTRONIX Model J-16 with TEKTRONIX Model P6503 Luminance Probe or equivalent.
- Color Television Degaussing Coil
- Convergence Checker
- 50X Magnifying Eyepiece
- Adjustment Tool — Tip Width: 1/8", Length: 6", non-conductive
- Adjustment Tool — Hex head, non-conductive

Preliminary Notes

NOTES

A red, green, or blue field display should not show noticeable color shading if proper degaussing occurred at instrument turn-on. If color shading is apparent, manually degauss by pressing and holding the DEGAUSS switch for at least 10 seconds. ANY change of the physical location or orientation of the Display Module after degaussing will affect screen purity and will require manual degaussing. Allow at least five minutes between degauss cycles to ensure cooling of the degauss thermistors or incomplete degaussing will occur.

A WHITE FIELD DISPLAY in excess of 25 fL, if displayed for more than a few minutes, may cause temporary color shading which cannot be corrected by internal degaussing.

Allow the display to warm up at least 20 minutes before performing any adjustments.

Procedure

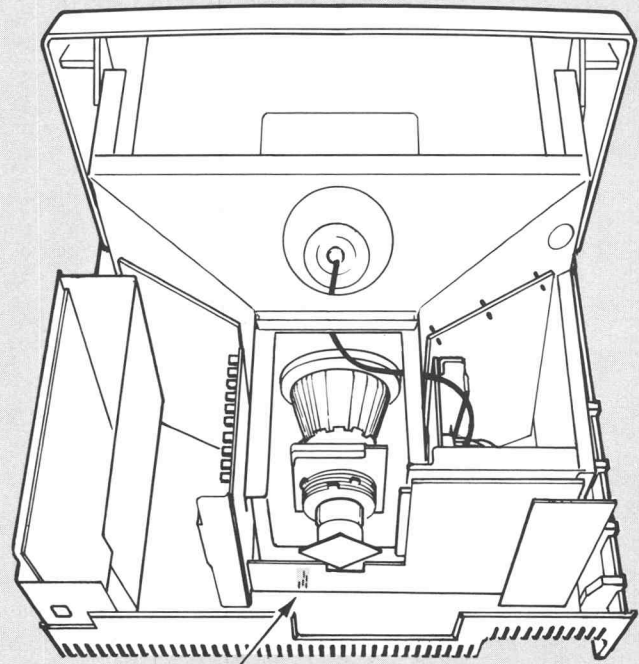
Perform the GMA302 adjustment on a sequence starting with Figure 5-2 and continuing up through Figure 5-13. The sequence of adjustments will be:

- Display Low Voltage Power Supply (DLVPS) Voltages
- LVPS Periodic and Random Deviation (PARC) Voltages
- High Voltage Power Supply
- Horizontal and Vertical Hold
- CRT Cutoff
- Video Amplifier and Colorimetry
- Display Control Board Output
- Horizontal and Vertical Deflection
- Focus
- Convergence
- Purity
- Offset

Display Low Voltage Power Supply (DLVPS) Voltages

VOLTAGE TOLERANCES

Output Voltage	Voltage Tolerance Limits	
	Minimum	Maximum
160V	152.0	168.0
75V	71.25	78.75
25V	23.75	27.50
19V	18.05	20.90
-19V	-18.05	-20.90
15V	14.25	15.75
-15V	-14.25	-15.75
11V	10.45	12.10
-11V	-10.45	-12.10
5V	4.75	5.25



- A** Connect positive DVM lead to test points for the Low Voltage Power Supply, connect negative lead to the chassis.
- B** Verify that the voltages are within the values shown.

5644-25A

Figure 5-2. DLVPS Voltages (for GMA302).

Periodic and Random Deviation (PARD) Voltages

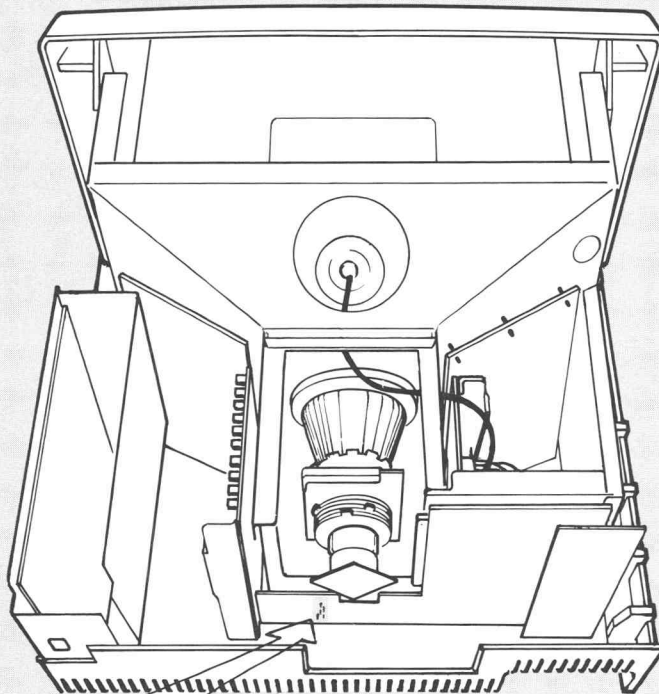
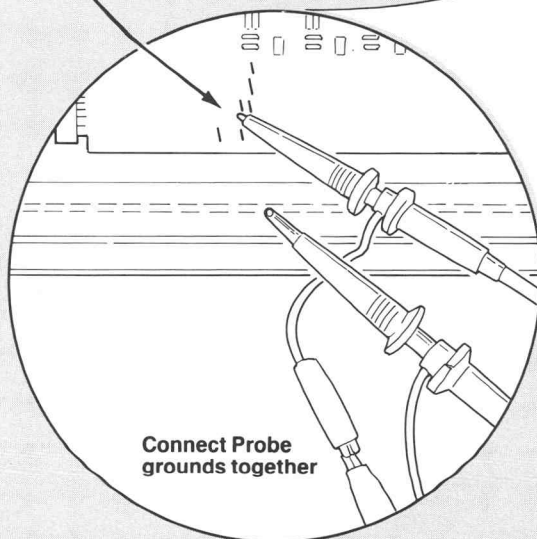
A Page the screen.

B Set Oscilloscope:

Sweep Rate: 5ms/div
 Volts: .5V/div
 (All except +15, -15, and +5V)
 50mV/div (+15, -15, and +5V)

CH 1: AC
 CH 2: AC, INVERT
 Vert Mode: ADD
 Bandwidth Limit: 20MHz
 Triggering: Source: LINE
 Slope: +
 Mode: AUTO
 Coupling: AC

C Hook one scope probe to GND test point and the other scope probe to a voltage test point. Verify that each PARD voltage (at the test points) is less than or equal to the NOISE LIMITS table.



NOISE LIMITS

Output	Maximum PARD Voltage
160V	1V
75V	500mV
25V	800mV
19V	200mV
-19V	200mV
15V	100mV
-15V	100mV
11V	300mV
-11V	300mV
5V	100mV

5644-26A

Figure 5-3. Periodic and Random Deviation (PARD) Voltages (for GMA302).

WARNING

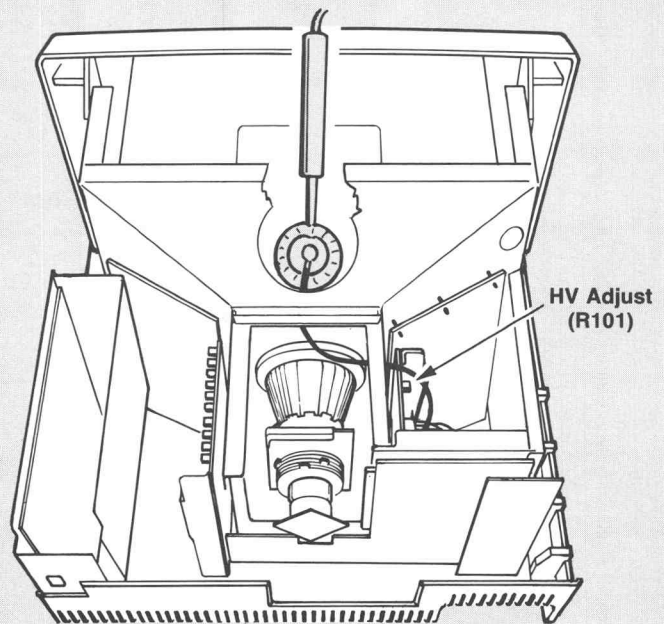
Keep hands clear of the anode connection to avoid risk of potentially **DANGEROUS** electric shock. Do **NOT** attempt to measure high voltage with the anode lead disconnected from the crt. Ensure that the anode connection is secure and properly covered by the protective rubber cap at all times that power is applied.

CAUTION

The probe connection should be protected by the anode insulating cap and **NO** exposed connection should be allowed. A high voltage arc can travel in excess of one inch through the air to the metal chassis, causing component damage.

High Voltage Power Supply

- (A)** Disconnect the power cord and connect the High Voltage Probe as shown.
- (B)** Set the DVM RANGE switch to 200 VDC.
- (C)** Connect the power cord and verify that after 1 minute the voltage is 24.5—25.5kV.
- (D)** If necessary adjust the H.V. adjustment (R101) for a reading of 25.0kV.
- (E)** Disconnect the power cord and remove the High Voltage Probe.
(Make certain that the Anode Connection is secure and properly covered by the Insulating Cap.)
- (F)** Connect the power cord.

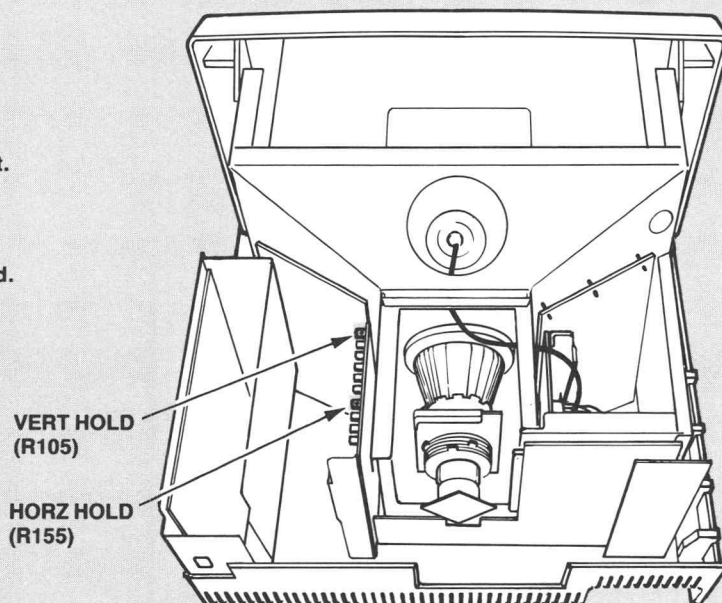


5644-27

Figure 5-4. High Voltage Power Supply (for GMA302).

Horizontal and Vertical Hold

- (A)** Call up a grid pattern.
- (B)** Adjust **HORZ HOLD (R155)** CW until the sync is lost.
Note the position of the potentiometer.
Now adjust (R155) CCW until the sync is lost.
Note the position of the potentiometer.
Center (R155) between the two positions just noted.
- (C)** Adjust **VERT HOLD (R105)** in the same manner.



5644-28

Figure 5-5. Horizontal and Vertical Hold (for GMA302).

CRT Cutoff

(A) Connect the scope probe to J31.

(B) Set Oscilloscope:

Sweep Rate: 10 μ s/div
 Volts: 10V/div
 Triggering: Source: CH-1
 Slope: +
 Coupling: AC
 Mode: AUTO

(C) Verify a signal of approximately 0 to -19V.

(D) Disconnect the power cord.

(E) Remove jumper J53.

(F) Turn the BRIGHTNESS control (on the Bezel) fully CCW, the three GAIN potentiometers fully CCW, the INT LIM potentiometer fully CW, and the SCREEN G2 adjustment fully CCW.

(G) Connect the power cord.

(H) Connect the probe to the red cathode output, (center conductor of coax cable). Adjust RED LEVEL for a reading of 100V.

(I) Check for a flat DC voltage. If a pulse is present, perform the 'Offset Adjustment' at the end of this section.

(J) Repeat steps 'h' and 'i' for each of the other cathodes.

(K) Adjust SCREEN G2 slowly CW until a dim horizontal line is just visible.

(L) Adjust the RED LEVEL, GREEN LEVEL, or BLUE LEVEL controls until the most pronounced color of the line observed in 'k' is just extinguished.

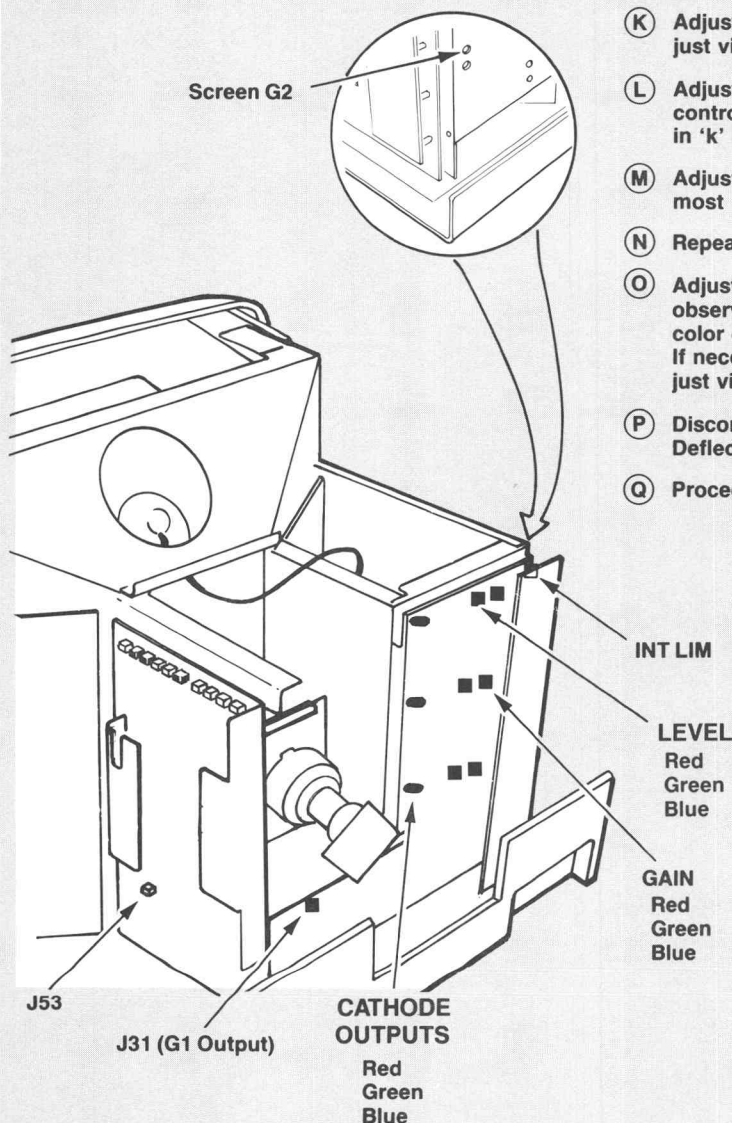
(M) Adjust SCREEN G2 slightly CW as required until the next most pronounced color is just visible.

(N) Repeat steps 'l' and 'm' until the third color is just visible.

(O) Adjust the LEVEL adjustment of the first two colors observed in parts 'l' and 'm' to match the intensity of the color observed in 'n' and the display becomes a gray line. If necessary, reduce SCREEN G2 adjustment until the line is just visible.

(P) Disconnect power cord. Reinstall Jumper J53 on the Deflection board. Connect power cord.

(Q) Proceed to Video Amplifier gain and Colorimetry Adjustment.

**CAUTION**

Since no vertical deflection is present with jumper J53 removed, care must be taken to prevent a bright horizontal line from being present on the CRT, except for a very short time. Make only small, slow adjustments of SCREEN G2 and video level controls while observing the display. Failure to observe this caution may result in permanent damage to the CRT.

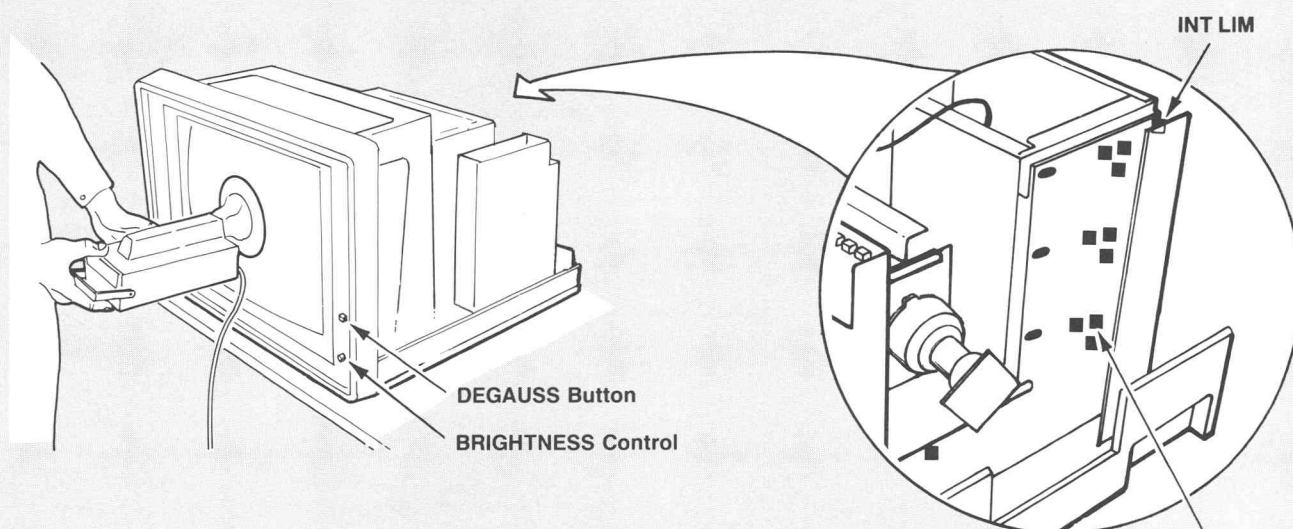
NOTE

The adjustments made with jumper J53 removed must be performed with a minimum ambient light level for accurate adjustment.

5644-29A

Figure 5-6. CRT Cutoff (for GMA302).

Video Amplifier and Colorimetry

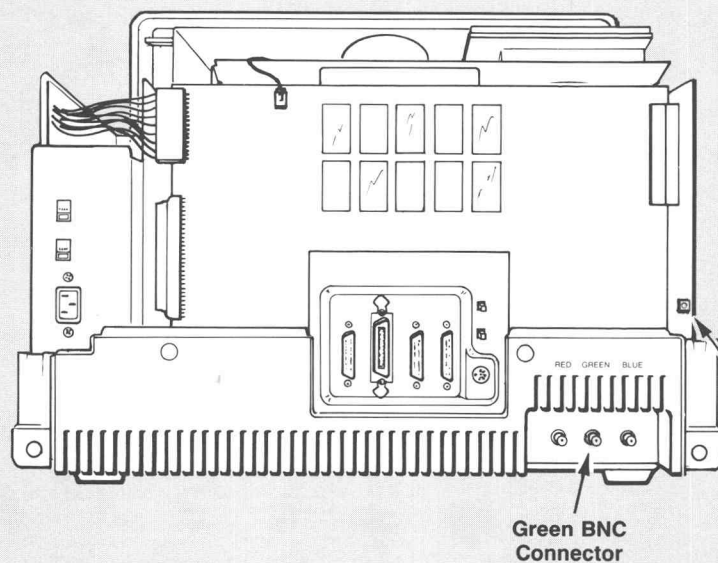


- (A)** Press and hold the DEGAUSS switch for at least 10 seconds.
- (B)** Call up a green screen and place the photometer in the center of the screen as shown with the BRIGHTNESS control and GREEN GAIN set fully CW.
Adjust the INT LIM for a photometer reading of 25 fL.
Adjust the GREEN GAIN for a photometer reading of 17.4 fL (± 0.8).
- (C)** Call up a red screen and adjust the RED GAIN for a photometer reading of 4.7 fL (± 0.5).
- (D)** Call up a blue screen and adjust the BLUE GAIN for a photometer reading of 2.9 fL (± 0.3).
- (E)** Call up a white screen and verify a photometer reading of 25 fL. Adjust the INT LIM, if necessary, to achieve this reading.
- (F)** Call up the GRAY SCALE pattern and perform the following checks:
 - a. The first level of the GRAY SCALE pattern is black, not visible under reduced ambient light. The second level should be clearly visible.
 - b. All other gray levels should have approximately equal visible differences in intensity.
 - c. The gray levels should appear uniform with no color tinging.
 If checks a, b, or c fail, repeat Steps (A) through (F).
- (G)** Call up a red screen and verify that no perceivable hue change is evident over the entire display area.
- (H)** Turn on the GREEN gun with the RED gun and verify that no perceivable hue change is evident over the entire display area.
- (I)** Turn on the BLUE gun with the GREEN gun and check that no perceivable hue change is evident over the entire display area.

5644-30A

Figure 5-7. Video Amplifier and Colorimetry (for GMA302).

Display Control Board Output



- Ⓐ Center potentiometers R203, R231, and R261 on the Video Converter board.
- Ⓑ Call up a white screen.
- Ⓒ Install a 75Ω terminator (if available) on the GREEN external video output on the rear of the terminal. Measure the waveform on the center conductor of the GREEN BNC connector. Set R698 on the Display Control board for a peak-to-peak reading of 1 V (with terminator — 2 V peak-to-peak if no terminator is installed).

5644-48

Figure 5-8. Display Control Board Output (for GMA302).

Horizontal and Vertical Deflection

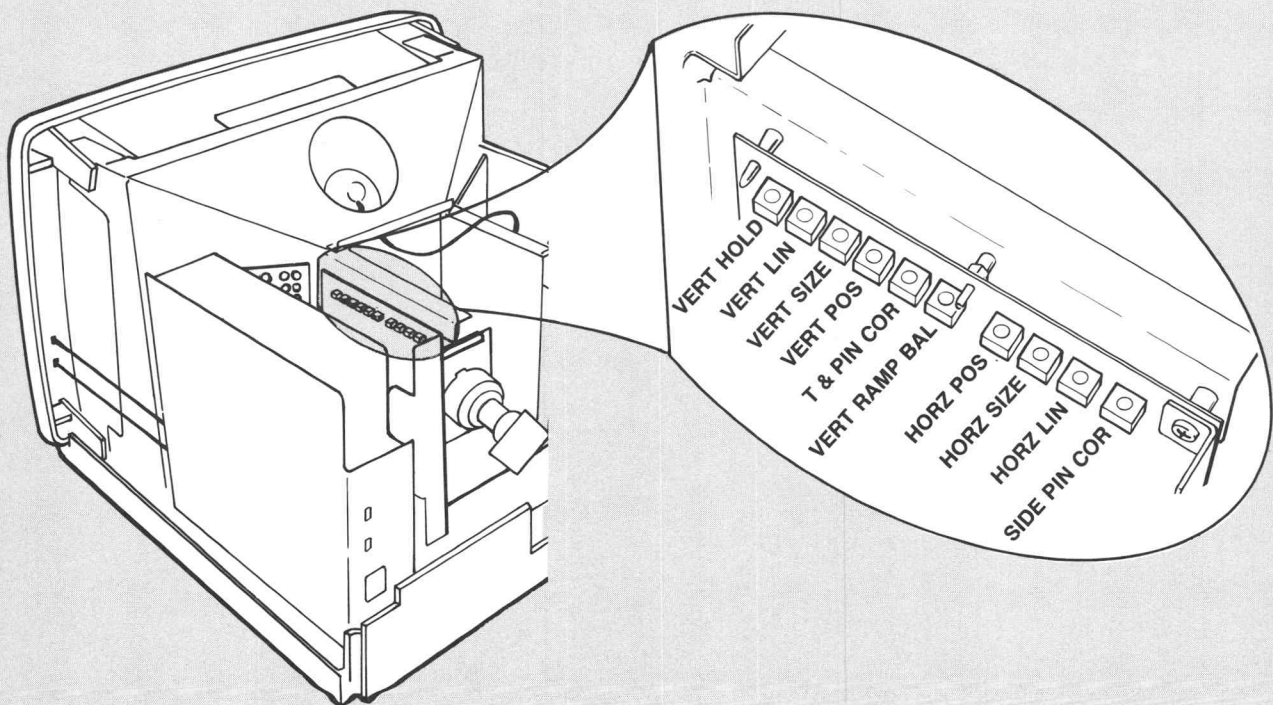
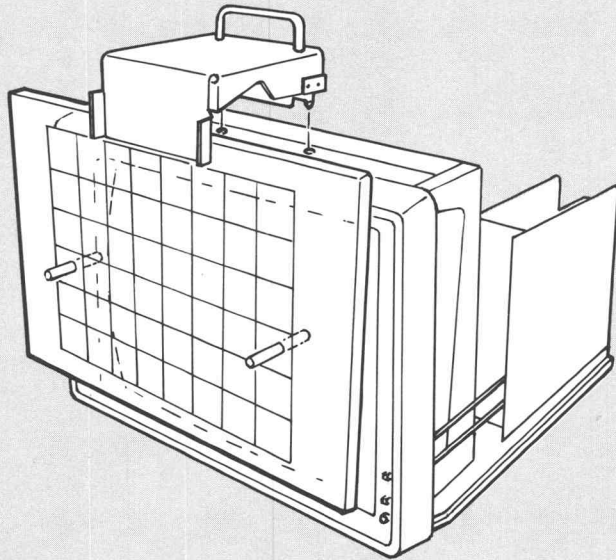
NOTE

There is some interaction between the deflection adjustments and the convergence. Verify that the convergence is roughly correct before adjusting the deflection.

1. Perform Steps (A), (B), and (C) (shown on Figure 5-9).
2. Call up the grid pattern.
3. Adjust the VERT POS so the horizontal center line of the displayed grid pattern is aligned with center line on the graticule.
4. Adjust the VERTICAL LINEARITY so the squares of the grid pattern appear symmetrical in the vertical direction.
5. Adjust the VERT SIZE so that the vertical size of the grid border aligns with the graticule grid border at the center of the graticule.
 - a. If the vertical size of the pattern is smaller than the graticule, adjust the VERT SIZE CW.
 - b. If the vertical size is larger than the graticule, adjust the VERT SIZE CCW.
6. Adjust the T & B PIN COR for the straightest possible top and bottom edge grid lines. (These lines may not be exactly horizontal at this time).
7. Repeat steps 3 through 6 for best vertical alignment of the grid pattern to the graticule.
8. Adjust the HORIZ POS so that the vertical center line of the grid pattern is aligned with the center line on the graticule.
9. Adjust the HORIZ LINEARITY coil so that the grid squares appear symmetrical in the horizontal direction. (Rotate the coil adjustment CW to maximum width, then continue CW rotation to reduce the left half of the square width.)
10. Adjust the HORIZ SIZE so that the vertical sides of the grid align with the graticule border.
 - a. If the horizontal size of the pattern is smaller than the graticule width adjust HORIZ SIZE CW.
 - b. If the horizontal size is larger than the graticule width adjust HORIZ SIZE CCW.
 - c. Adjust the SIDE PIN COR to achieve the optimum alignment of the sides of the grid pattern with the graticule.
11. Adjust the RAMP BALANCE so that the vertical lines of the grid are as perpendicular to the horizontal lines as possible.
12. Repeat steps 8 through 11 as necessary for the best possible alignment of the vertical grid lines with the vertical graticule lines.
13. Verify that the grid pattern line intersections are aligned with the graticule line intersections (within the box limits given on the graticule).

Horizontal and Vertical Deflection

- A** Install CRT Graticule and push handle to left to lock in position.
- B** Face CRT east or west
- C** Proceed with Step 2 of Text.



VERT HOLD
 VERT LIN
 VERT SIZE
 VERT POS
 T & PIN COR
 VERT RAMP BAL
 HORZ POS
 HORZ SIZE
 HORZ LIN
 SIDE PIN COR

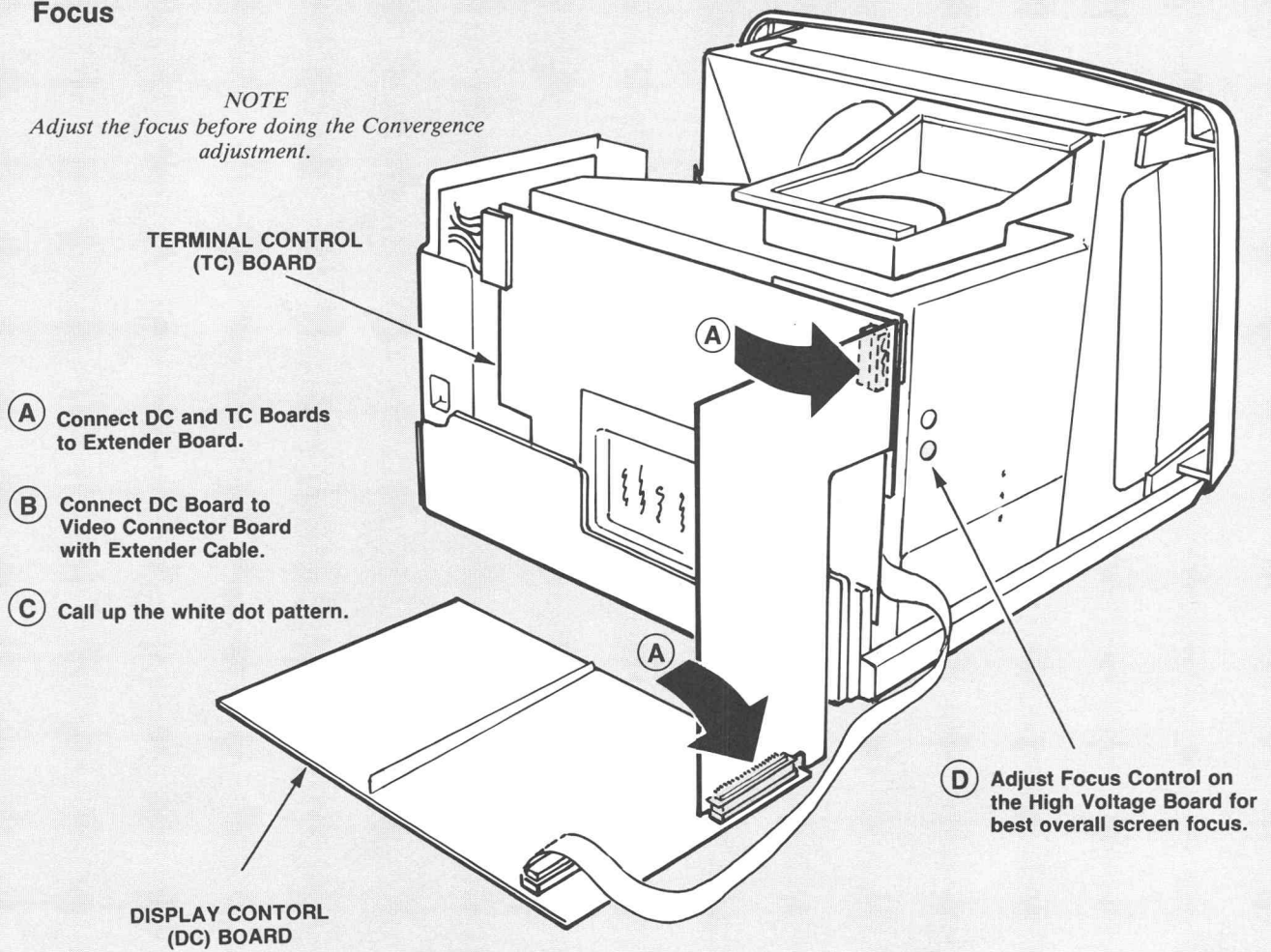
5644-31

Figure 5-9. Horizontal and Vertical Deflection (for GMA302).

CHECKS AND ADJUSTMENTS

Focus

NOTE
Adjust the focus before doing the Convergence adjustment.



5644-32A

Figure 5-10. Focus (for GMA302).

CAUTION

Improper adjustment of the convergence may result in an overload of the LVPS.

NOTE

Adjust the focus before adjusting the convergence. Do not readjust the focus after adjusting the convergence, or you may have to readjust the convergence.

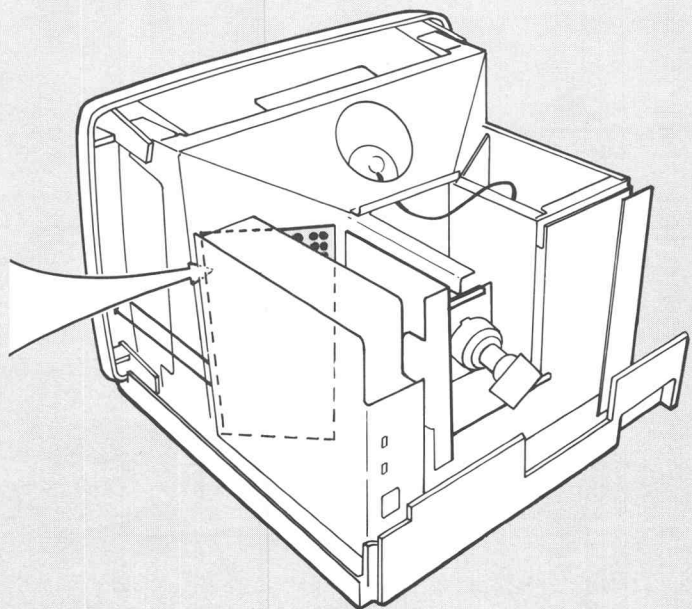
CONVERGENCE**Convergence Bd.**
(9 sets of controls)

Horizontal	Vertical	Horizontal	Vertical	Horizontal	Vertical	
						Red/Blue
9		4		8		Magenta/Green
						Red/Blue
2		1		3		Magenta/Green
						Red/Blue
6		5		7		Magenta/Green

Display Screen
(9 regions of adjustment)

9	4	8
2	1	3
6	5	7

A Face CRT east or west.



B Call up a grid pattern and turn off the green gun. (Press the SETUP key.)

C Adjust the RED/BLUE convergence potentiometer pairs in the sequence shown while observing the correspondence display position on the CRT.

D Turn on the green gun. (Press the SETUP key.)

E Adjust the MAGENTA/GREEN convergence potentiometer pairs in the sequence shown while observing the corresponding display position on the CRT.

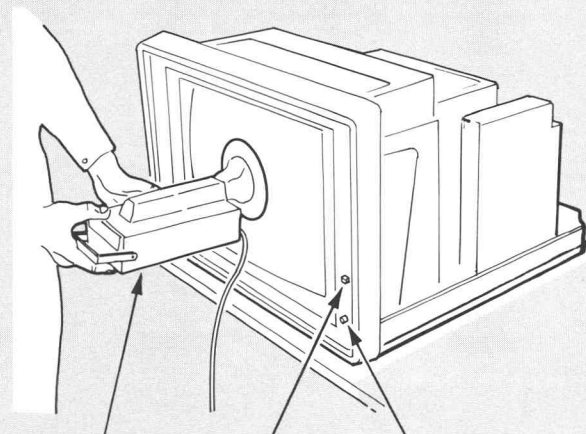
5644-33

Figure 5-11. Convergence (for GMA302).

Purity

NOTE

The purity magnet assembly is factory calibrated by the manufacturer and permanently sealed. If no unusual magnetic environment is present and thorough degaussing does not solve the problem, replace the CRT assembly.



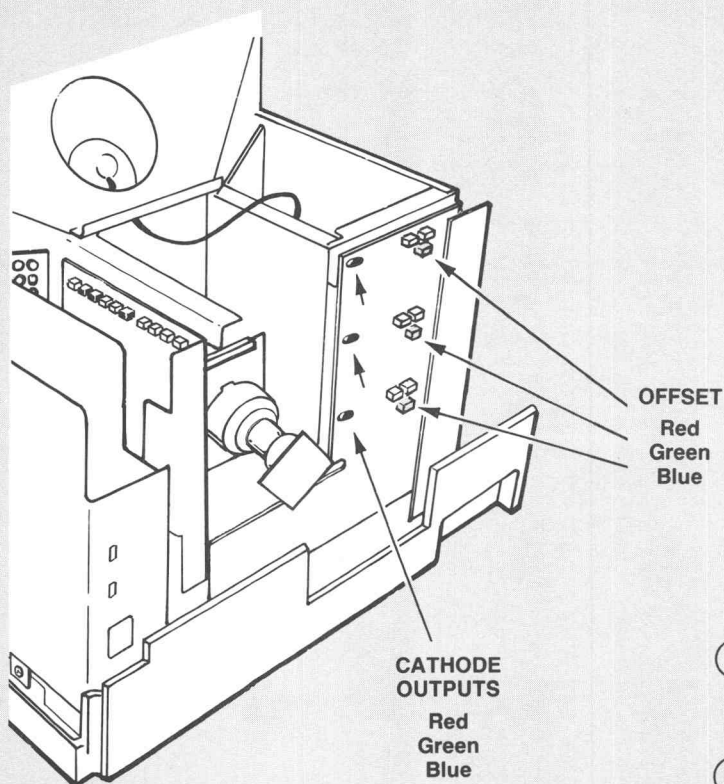
- A** Call a red screen.
- B** Position the photometer in the center of the screen.
- C** Adjust the BRIGHTNESS until a reading of 4.7fL is achieved.
- D** Remove the photometer and verify that the screen is pure red (no other hues present). If color is not pure, proceed to Step **E**. If color is pure, proceed to Step **I**.
- E** Verify that no unusual magnetic fields are near the display (magnetic screwdrivers, table magnets, etc.).
- F** Press and hold the Degauss switch for at least 10 seconds. If the displayed field is still not pure, proceed with Step **G**, otherwise, go to step **I**.
- G** Disconnect the power cord, wait five minutes, and connect the cord while pressing and holding the DEGAUSS button. If the displayed field is still not pure, proceed with Step **H**, otherwise go to step **I**.
- H** Align the crt in an east-west direction. Place an external degaussing coil at a right angle to the face of the crt and 8 to 10 feet away from the screen. Energize the coil and move it toward, over, and around the crt in circular motions, in all directions. Slowly move the coil away from the front of the crt to a distance of 8 to 10 feet, holding at right angles to the crt. Then turn off the coil.
- I** When the red screen is pure, repeat Steps **B**, **C**, and **D** for green and blue screens. Set the BRIGHTNESS to 17.4fL for the green screen and 2.9fL for the blue screen.

5644-34A

Figure 5-12. Purity (for GMA302).

Offset**NOTE**

Perform this adjustment only if indicated while performing the CRT Cutoff adjustment. Refer to "CRT Cutoff", in this section, for details.



There are three OFFSET potentiometers (R161, R361, and R561) on the Video board of the Display Monitor. You should not have to perform the Offset adjustment unless you have replaced U155, U355, or U555.

(A) Set the oscilloscope as follows:

Sweep Speed — 10 ms/div

Volts/Div — 10 V

Triggering:

Source — Input

Slope — -

Coupling — DC

Mode — AUTO

(B) Call up a white screen.

(C) Turn the BRIGHTNESS control on the bezel fully counterclockwise.

(D) Connect the scope probe to the RED cathode output on the Video board (refer to "CRT Cutoff", in this section, for the location).

(E) Adjust the RED OFFSET potentiometer so that there is no pulse visible (flat DC level).

(F) Repeat for the GREEN and BLUE outputs.

5644-49

Figure 5-13. Offset (for GMA302).

119-2387-00 DISPLAY MODULE

WARNING

The Service Adjustment Procedure can expose service personnel to voltage levels that are potentially lethal. To avoid a hazardous situation, all servicing should be done by authorized service personnel using proper servicing techniques and equipment.

The Display Module may need adjustment if the convergence or purity becomes unsatisfactory, or if repairs have been made. Use the following adjustment procedure only if your terminal has the 119-2387-00 Display Module.

Tools Required

- Dual Trace Oscilloscope — Vertical: 100 mV/div, Time Base: 5 ns/div. TEKTRONIX Model 2236 or equivalent. Also required, 3 oscilloscope probes — Attenuation : 10:1, Resistance: 10 M Ω , Capacitance: 10 pF, Length: 1 meter. TEKTRONIX Model P6106 or equivalent.
- Digital Voltmeter — Range: 0 to 1000 VDC, Accuracy: 0.1%. TEKTRONIX DM501 or equivalent. Also required, high voltage probe — Range: 0 to 30 kV, Attenuation: 1000:1, Input Impedance: 1000 M Ω . Fluke Model 80K-40 or equivalent.
- Calibration Graticule (refer to the Accessories Parts List for part number)
- Photometer — TEKTRONIX Model J-16 Photometer with a TEKTRONIX Model P6503 Luminance Probe or equivalent.
- Minolta Chroma Meter (Optional) — that reads chromaticity X and Y coordinates.
- Color Television Degaussing Coil
- Adjustment Tool — Tip Width: 1/8", Length: 6", non-conductive
- Adjustment Tool — Tip Width: 1/8", Length: 12", non-conductive
- Adjustment Tool — Hex head, non-conductive

Preliminary Notes

NOTES

The Display Module should face either east or west during calibration. A red, green, or blue field display should not show noticeable color shading if proper automatic degaussing occurred at instrument turn-on. If color shading is apparent, manually degauss by pressing the DEGAUSS switch (use when a white field is displayed on the screen. ANY change of the physical location or orientation of the Display Module after degaussing will affect screen purity and will require additional degaussing. Use an external degaussing coil any time the DEGAUSS switch does not remove color shading.

*A **WHITE FIELD DISPLAY** in excess of 25 fL, if displayed for more than a few minutes, may cause temporary color shading which cannot be immediately corrected by internal degaussing.*

Allow the Display Module to warm up at least 20 minutes before performing any adjustments.

Procedure

Perform the 119-2387-00 Display Module adjustment in a sequence starting with Figure 5-14 and continuing up through Figure 5-23. The sequence of adjustments will be:

- Display Low Voltage Power Supply
- High Voltage Power Supply
- Purity
- Focus
- Convergence
- Horizontal and Vertical Hold
- Horizontal and Vertical Deflection
- DC Contrast
- G2 Voltage and CRT Cutoff
- White Balance

Display Low Voltage Power Supply

CAUTION

The 90V and 24V voltages on the Display Low Voltage Power Supply (DLVPS) must be within specifications before proceeding with any Display Module adjustment.

Refer to Figure 5-14 to check or calibrate the DLVPS.

1. (A) Connect positive DVM lead to the indicated test points on the DLVPS. Connect negative lead to either the chassis or to TP92 (ground).
2. (B) Check that dc voltage at TP91 (on Deflection/HV board) is $90V \pm 0.5V$.
3. (C) Check that dc voltage at wire strap J800 (on Deflection/HV board) is $24V \pm 0.5V$.

WARNING

Take extreme care when working near the HV portion of the Deflection/HV board. Dangerous voltages are also exposed inside the DLVPS when the DLVPS side cover is opened. During the following procedure, make sure the DLVPS does not short out resistors or the power transistor on the Deflection/HV board.

4. (D) If the 90V or 24V outputs are not in tolerance, perform the following steps:
 - a. Unplug the terminal.
 - b. Remove the DLVPS module.
 - c. Remove the DLVPS side cover (three screws).
 - d. Locate RV1 and RV2 inside the DLVPS.
 - e. Rotate the DLVPS so the CN1 and CN2 connectors are facing up, and carefully position the DLVPS over the Deflection/HV board.
 - f. Reconnect the DLVPS cables and apply power to the Display Module.
 - g. Adjust the required voltages; (adjust 90V with RV1, adjust 24V with RV2).
 - h. Then unplug the terminal, disconnect the DLVPS cables, reassemble and reinstall the DLVPS in the normal location.
 - i. Perform Steps 1 through 3 again to recheck voltages.

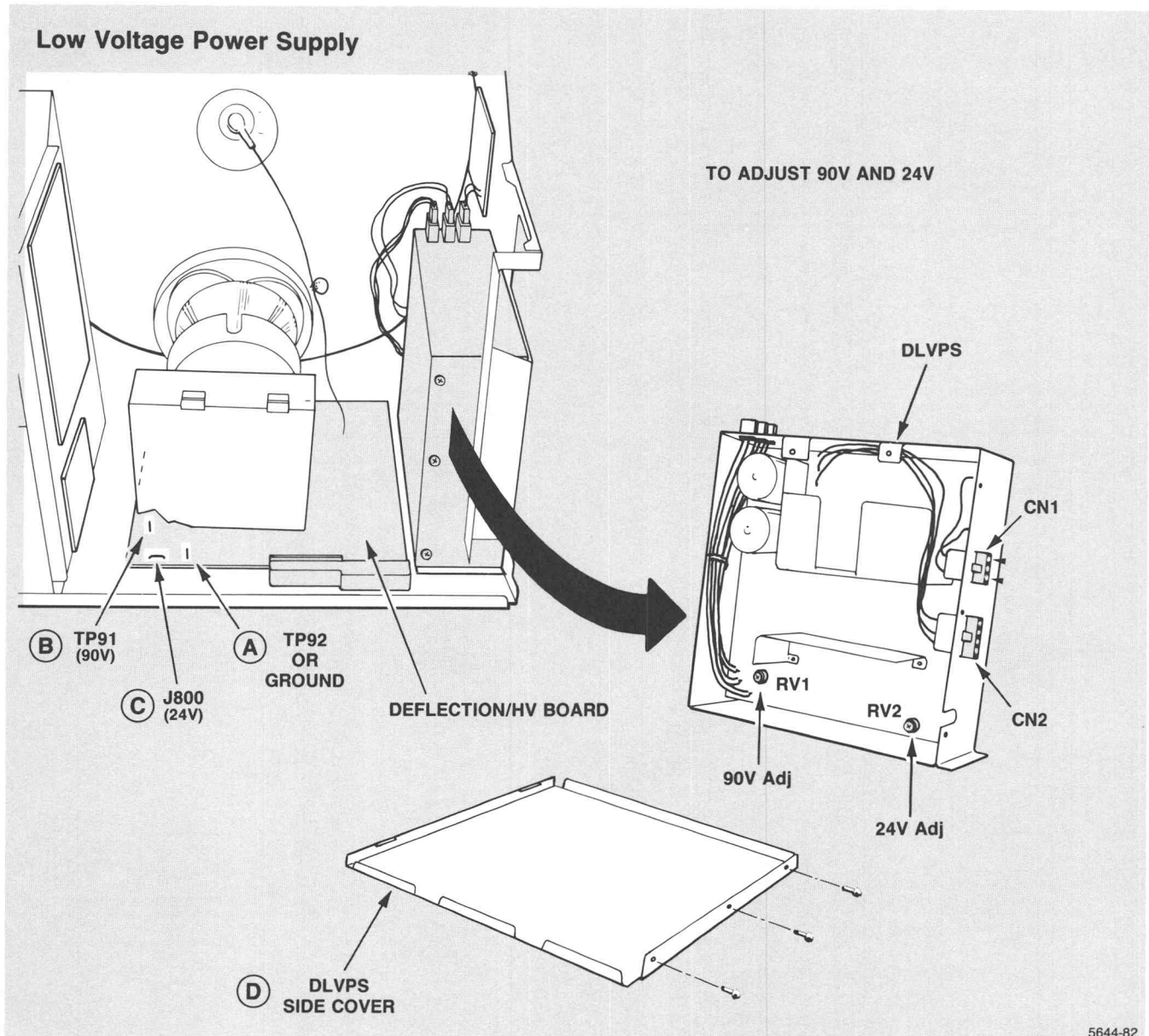
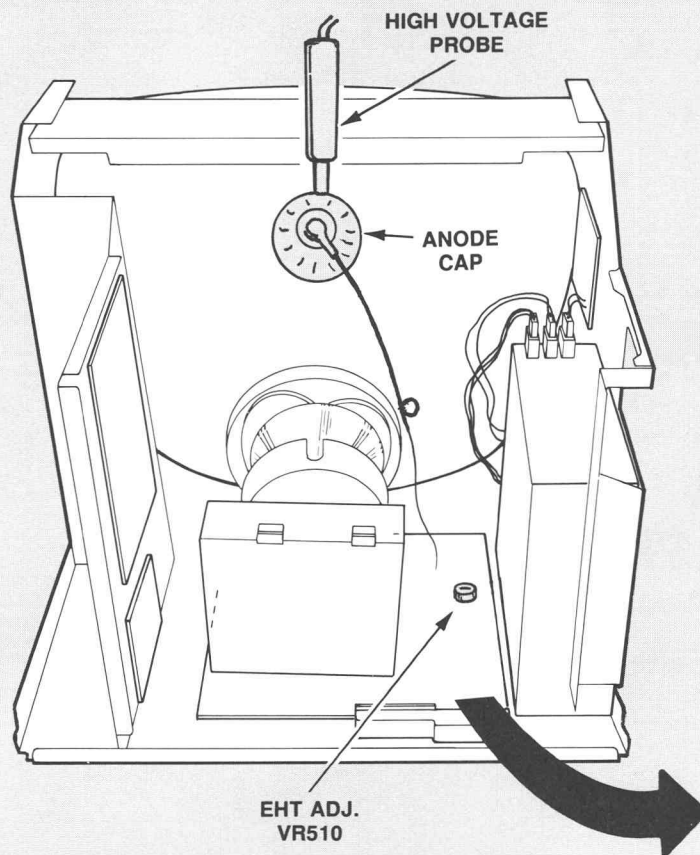


Figure 5-14. Display Low Voltage Power Supply (for 119-2387-00).

High Voltage Power Supply

**WARNING**

Keep hands clear of the anode connection to avoid risk of potentially **DANGEROUS** electric shock. Do NOT attempt to measure high voltage with the anode lead disconnected from the crt. Ensure that the anode connection is secure and properly covered by the protective cap during all times that power is applied.

CAUTION

The probe connection should be protected by the anode insulating cap and NO exposed connection should be allowed. A high voltage arc can travel in excess of one inch through the air to the metal chassis, causing component damage.

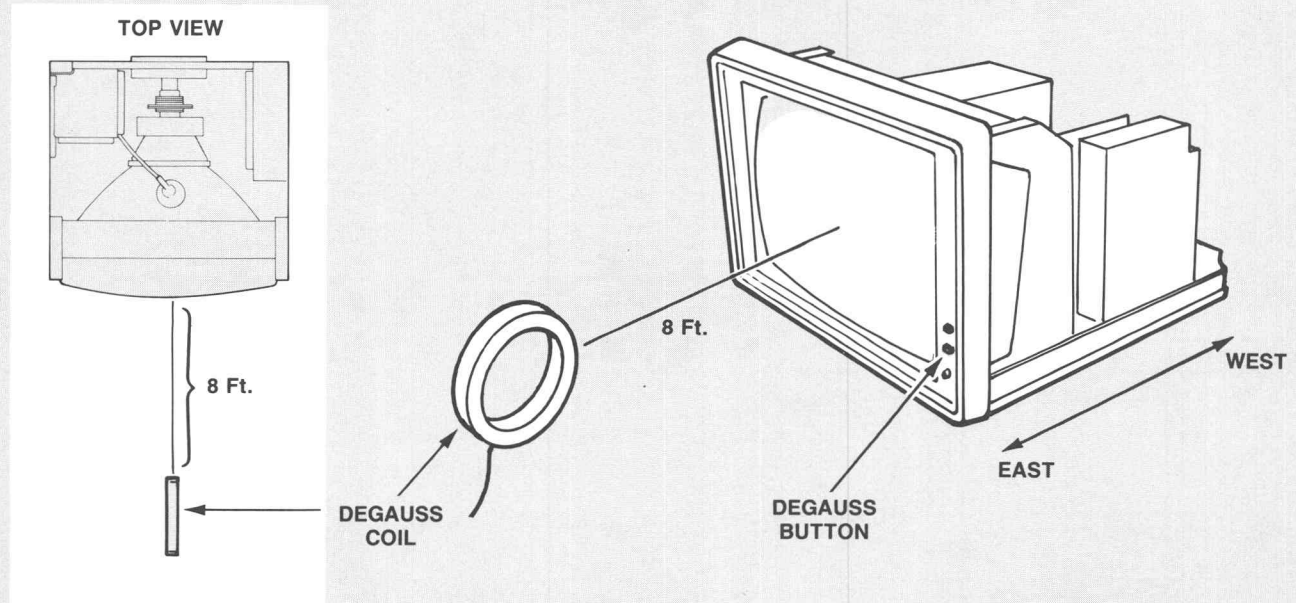
- A** Disconnect the power cord, discharge the crt anode to the chassis, and connect the High Voltage Probe (1000:1 attenuation) as shown.
- B** Set the DVM RANGE switch to 200 VDC.
- C** Set the front panel BRIGHTNESS control to the midrange (detent) position. Set the front panel CONTRAST control fully CCW.
- D** Connect the power cord and display a black screen with Self-test.
- E** Rotate SCREEN Control (on Deflection/HV board) CCW so the background raster just disappears (this control is very sensitive).
- F** Verify that after one minute the voltage is 26.5kV (± 0.25 kV).

- G** If necessary, adjust the EHT adjustment (VR510) for a reading of 26.5kV.
- H** Disconnect the power cord and remove the High Voltage Probe. Make certain that the Anode Connection is secure and properly covered by the insulating cap.
- I** Reconnect the power cord.

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Figure 5-15. High Voltage Power Supply (for 119-2387-00).

Purity



NOTE

The purity magnet assembly is factory calibrated by the manufacturer and permanently sealed. If no unusual magnetic environment is present and a thorough degaussing does not solve the problem, replace the crt assembly.

- A** Call up a red screen.
- B** If color is not pure, proceed to Step **C**. If color is pure, proceed to Step **F**.
- C** Verify that no unusual magnetic fields are near the display (magnetic screwdrivers, table magnets, etc.). If possible, use a wooden workbench for this procedure.
- D** Press the Degauss button. If the displayed field is still not pure, proceed with Step **E**, otherwise go to Step **F**.
- E** Align the crt in an east-west direction. Place an external degaussing coil at a right angle to the face of the crt and 8 to 10 feet away from the screen. Energize the coil and move it toward, over, and around the crt and chassis in circular motions, in all directions. Slowly move the coil away from the front of the crt to a distance of 8 to 10 feet, holding at right angles to the crt. Then turn off the coil.
- F** When the red screen is pure, check blue and green screen purity. Repeat Step **E** if colors are not pure.

5644-84

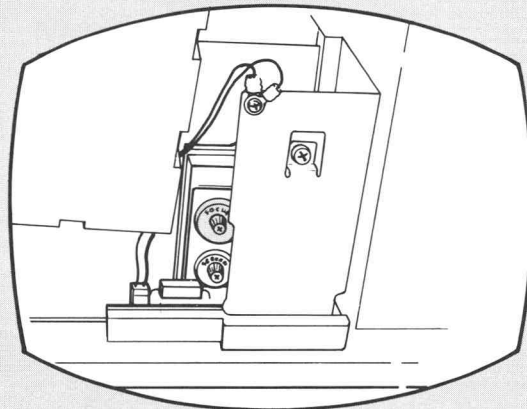
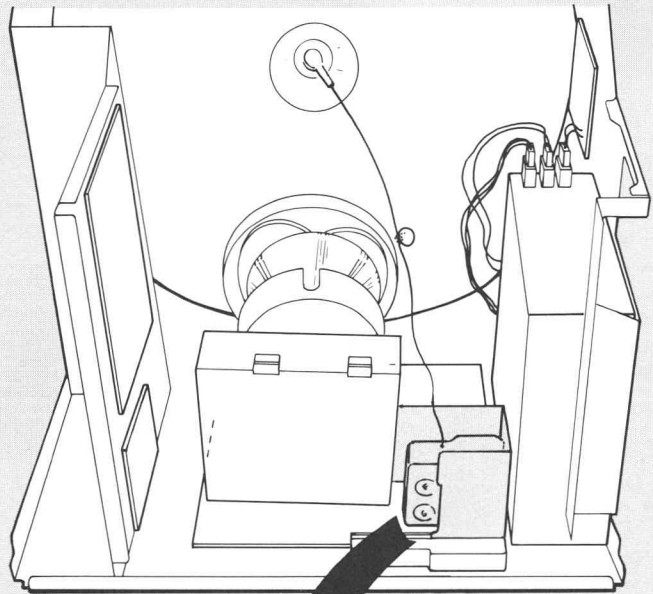
Figure 5-16. Purity (for 119-2387-00).

Focus

NOTE

Adjust the focus before doing the Convergence adjustments.

- A** Connect Display Control board to Extender board.
- B** Call up the text pattern.
- C** Adjust FOCUS control for best overall screen focus. Pay particular attention to the clarity of the hole in the upper case letter "B."



5644-85

Figure 5-17. Focus (for 119-2387-00).

Convergence Check

1. Face the crt screen either east or west.
2. Apply power to the terminal and press the front panel DEGAUSS button.
3. Run Self-test and display the grid pattern.
4. With the grid pattern, check convergence over the entire screen.

NOTE

The convergence specification is 0.35 mm or less between red and green, between green and blue, and between red and blue (over the entire screen).

5. If screen convergence meets the specification, go to the adjustment procedure for Horizontal and Vertical Hold. Otherwise, degauss the crt and cabinet with an external degaussing coil and recheck convergence (degaussing procedures are explained under the previous Purity Adjustment topic). If convergence problems still appear, proceed to adjust the convergence.

Convergence Adjustment

If the crt or deflection yoke is replaced, adjust the center convergence and peripheral convergence. Slight convergence deviations can be corrected by making a center convergence adjustment. Refer to Figure 5-18 for the following procedures.

WARNING

Lethal voltages are present in the adjustment area. Avoid contact with bare wires and exposed components on the Socket board and the yoke, because severe electrical shock can result.

CAUTION

Convergence was set at the factory using computer aided processes. There is a great deal of interaction between individual magnet sets; adjustment of any set affects other magnet sets. For this reason, field alignment of the sealed four-pole and six-pole magnet sets could take an excessive amount of time.

Note that the crt has three sets of convergence magnets (A) (B) (C) and one purity magnet set (D). Make sure you rotate the proper magnet set during adjustment.

CHECKS AND ADJUSTMENTS

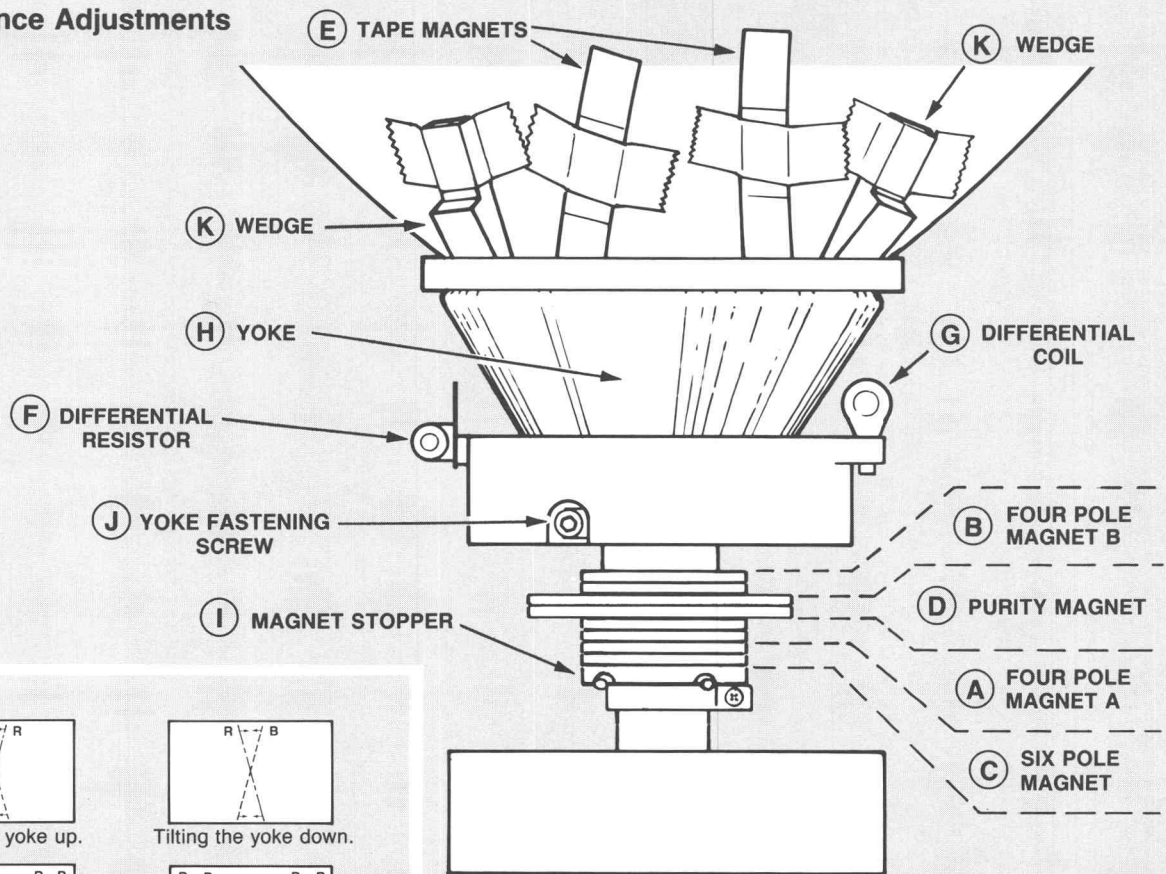
1. Inscribe an alignment mark on the ringsets with a marking pen before scraping off the paint that fastens the rings to each other. This aids in resetting the magnets to the factory settings if needed.
2. Loosen the threaded magnet stopper (I) on the crt neck by turning it CCW (as seen from the rear of the crt). This will allow smooth movement of the convergence rings.
3. Display the grid pattern (if it isn't already displayed).
4. Press the Setup key; this turns off the green gun (leaving only the red and blue guns on).
5. Match the red and blue images at the center of the screen by rotating the four-pole magnet (B) (the fourth pair of convergence rings, from the rear of the crt).
6. Turn on the green gun (press the Setup key).
7. Match up the red, green, and blue images at the center of the screen, by rotating the six-pole magnet (C) (rear pair of rings on crt).
8. Press the Setup key; this turns off the green gun (leaving only the red and blue guns on).
9. If necessary, loosen the yoke fastening screw (J) and gently nudge the yoke (H) from side to side, or up and down, to achieve the best overall convergence on the edges of the screen. (See the STEP-9 insert of Figure 5-18 for yoke positioning examples.) Secure the yoke in the optimum position by pressing in the five wedges (K) and by retightening the yoke fastening screw (J).
10. Install the calibration graticule. Check that the horizontal lines in the grid pattern match the horizontal lines on the graticule. If needed, rotate the yoke. When the pattern alignment is satisfactory, remove the graticule.
11. Recheck the purity adjustment. If purity was adversely affected, repeat the purity adjustment, then recheck convergence when finished.
12. Retighten the yoke fastening screw (J). Take care not to overtighten the screw and damage the crt.
13. Recheck horizontal line convergence at the center of the screen. If needed, realign with the differential coil (G). See the STEP-13 insert of Figure 5-18.
14. If lines are twisted either lefthand or righthand (see the STEP-14 insert of Figure 5-18 for examples) perform the following:
 - a. Use four-pole magnet (A) (the second pair of rings from rear of crt) to shift convergence of horizontal lines by 5 to 6 mm at the center of the screen. (For twisted righthand lines shift blue line upward and red line downward. For twisted lefthand lines shift red line upward and blue line downward. Do not shift convergence of vertical lines.)
 - b. Then realign convergence with four-pole magnet (B) (the fourth pair of convergence rings, from the rear of the crt).
15. Recheck horizontal line convergence at the top and bottom of the screen. If needed, realign with the differential resistor (F). See the STEP-15 insert of Figure 5-18.
16. Recheck convergence at the center of the screen. If needed, realign with the four-pole-magnet (B) and the six-pole-magnet (C). Retighten the magnet stopper (I) after alignment.
17. Insert wedges (K) as shown in the STEP-17 insert of Figure 5-18 (at the bottom, left top, right top, left side, and right side of the deflection yoke. Secure them with silicone adhesive and glass cloth tape. Remove any temporary wedges while keeping convergence aligned.

CAUTION

In the following step, DO NOT place the tape-magnets (E) closer than 20 mm from the HV anode cap. Do not tape them over any paper labels or secure them with silicone adhesive.

18. If the convergence on the fringe areas is still not acceptable, place one or more thin tape-magnets around the funnel to achieve the best effect. Then press these magnets onto the funnel. Verify convergence around all edges of the screen.
19. After completion of adjustment, apply locking paint on the movable portions of the deflection and convergence yokes to secure them.

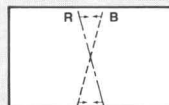
Convergence Adjustments



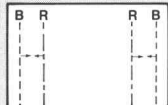
STEP - 9



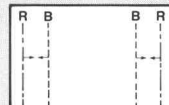
Tilting the yoke up.



Tilting the yoke down.

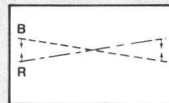
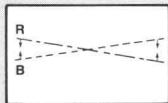


Tilting the yoke left.

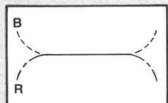


Tilting the yoke right.

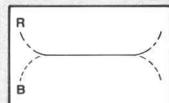
STEP - 13



STEP - 14

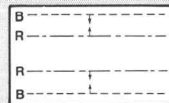
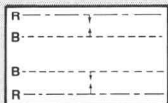


Beams are twisted lefthand.

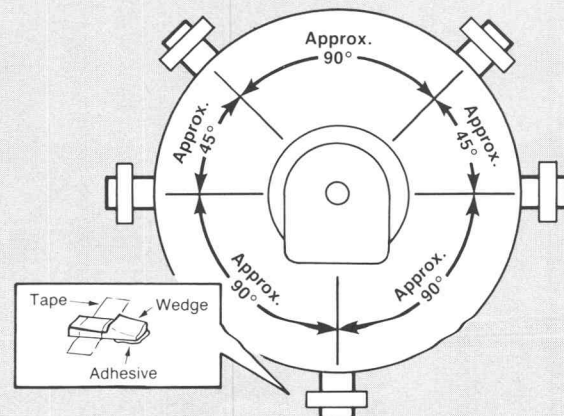


Beams are twisted righthand.

STEP - 15



STEP - 17 WEDGE SPACING AND HOW TO TAPE

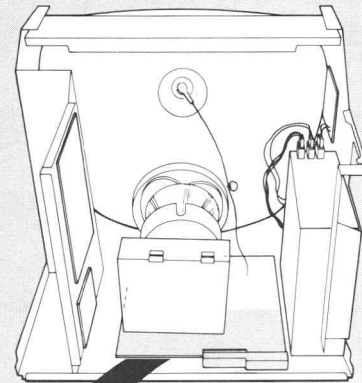


5644-86

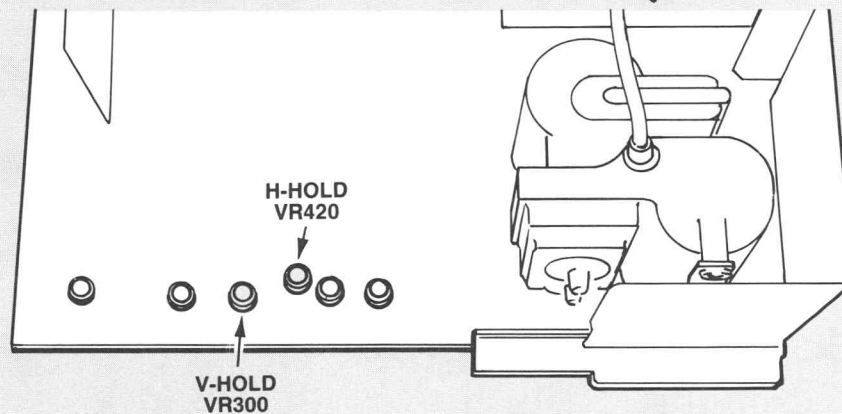
Figure 5-18. Convergence Adjustments (for 119-2387-00).

Horizontal and Vertical Hold

- A** Call up a grid pattern.
- B** Adjust H-HOLD (VR420) CW until the sync is lost. Note the position on the potentiometer. Now adjust VR420 CCW until the sync is lost. Again note the position on the potentiometer. Center VR420 between the two positions just noted.
- C** Adjust V-HOLD (VR300) in the same manner.



DEFLECTION/HV BOARD ADJUSTMENTS



5644-87

Figure 5-19. Horizontal and Vertical Hold (for 119-2387-00).

Horizontal and Vertical Deflection

NOTE

There is some interaction between the deflection adjustments and the convergence. Verify that the convergence is roughly correct after adjusting the deflection.

1. Perform Steps (A), (B), and (C) (shown on Figure 5-20 on next page).
2. Call up the grid pattern.
3. Adjust V-CENTER (VR440) so the horizontal center line of the displayed grid pattern is aligned with center line on the graticule.
4. Adjust V-LIN (VR321) so the squares of the grid pattern appear symmetrical in the vertical direction.
5. Adjust HEIGHT (VR320) so that the vertical size of the grid border aligns with the graticule grid border at the center of the graticule.
 - a. If the vertical size of the pattern is smaller than the graticule, adjust VR320 CW.
 - b. If the vertical size is larger than the graticule, adjust VR320 CCW.
6. Repeat steps 3 through 5 for best vertical alignment of the grid pattern to the graticule.
7. Adjust SCREEN control (at the rear of the HV transformer) to make the background raster faintly visible on the screen.
8. Adjust H-CENTER (VR441) to center the background raster horizontally on the screen. Reset the SCREEN control back to normal.
9. Adjust H-PHASE (VR400) so that the vertical center line of the displayed grid pattern is aligned with the center line on the graticule.
10. Adjust WIDTH (VR450) so that the vertical sides of the grid pattern align with the left and right borders of the graticule.
 - a. If the horizontal size of the pattern is smaller than the graticule width adjust VR450 CW.
 - b. If the horizontal size is larger than the graticule width adjust VR450 CCW.
11. Adjust SIDE-PIN (VR830) to achieve the optimum alignment of the sides of the grid pattern with the graticule.

NOTE

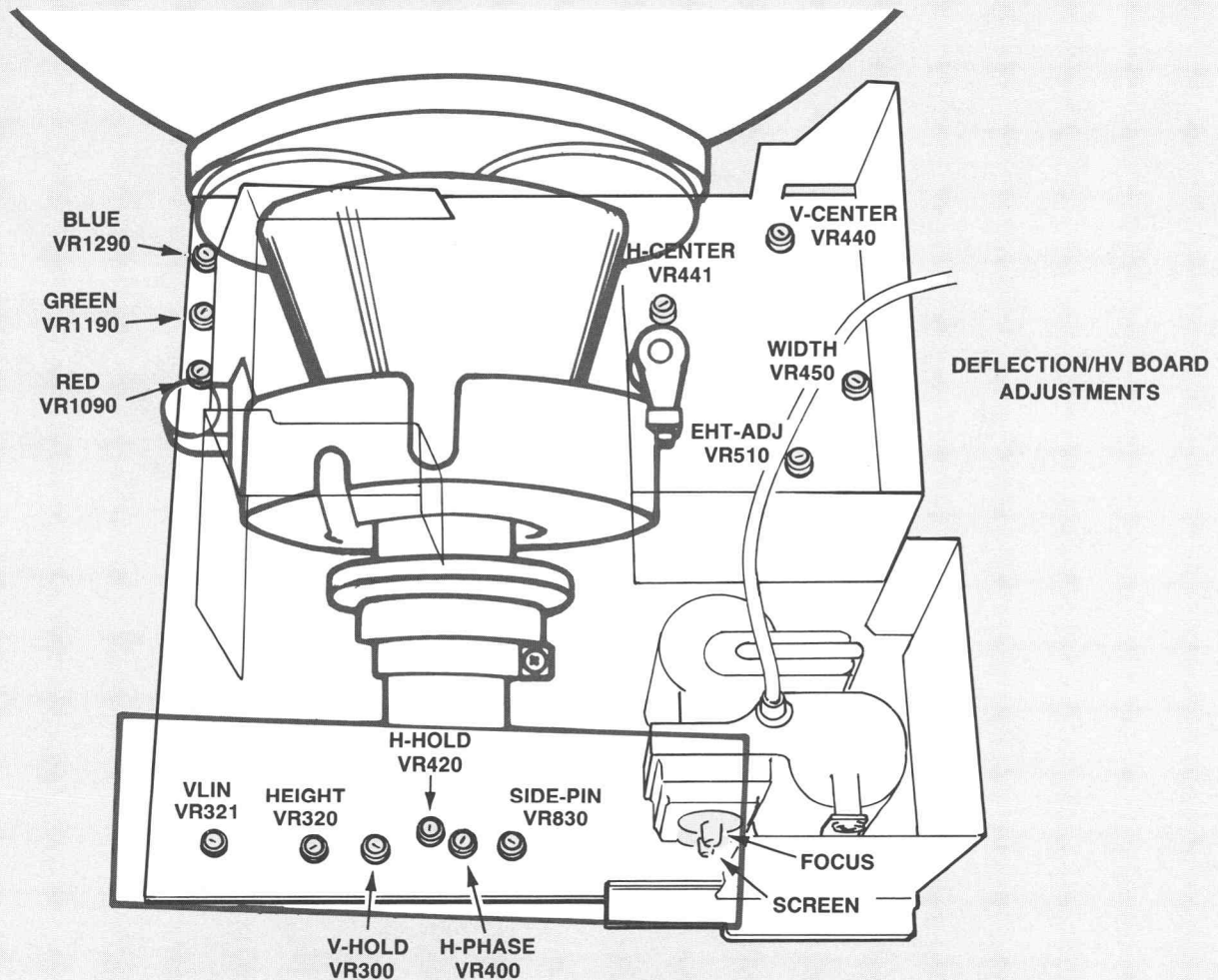
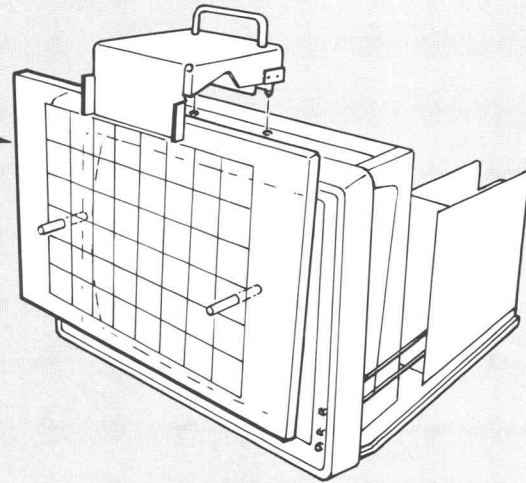
Adjustments between SIDE-PIN (VR830) and WIDTH (VR450) interact. Repeat the Side-Pin-Cushion and the Horizontal Width adjustments several times.

12. Repeat steps 8 through 11 as necessary for the best possible alignment of the vertical grid lines with the vertical graticule lines.
13. Verify that the grid pattern line intersections are aligned with the graticule line intersections (within the box limits given on the graticule).

Horizontal and Vertical Deflection

- A** Install CRT Graticule and push handles to left to lock in position.
- B** Face crt east or west.
- C** Proceed with Step 2 of Text.

CRT GRATICULE



5644-88

Figure 5-20. Horizontal and Vertical Deflection (for 119-2387-00).

Contrast Adjustments on Video Board

- (A)** Before attempting any adjustment, call up the GRAY SCALE pattern and perform the following checks:
- The first level of the GRAY SCALE pattern is black, not visible under reduced ambient light. The second level should be clearly visible.
 - All other gray levels should have approximately equal visible differences in intensity.
 - The gray levels should appear uniform with no color ringing.

If checks a, b, or c fail, perform Steps **(B)** through **(G)**. If the checks were ok, skip on to the G2 Voltage and CRT Cutoff adjustment procedure.

- (B)** Preset the following Video board adjustments as indicated:

- Fully CW (VR1010, VR1110, VR1210)
- Fully CCW (VR1011, VR1111, VR1211)
- Centered (VR1030, VR1130, VR1230)

- (C)** Call up a full white raster as a screen display.

- (D)** Set an oscilloscope as follows:

- Sweep Rate: .1ms/div
- Volts: .2V/div
- Triggering: Source: CH-1
Slope: +
Coupling: AC
Mode: AUTO

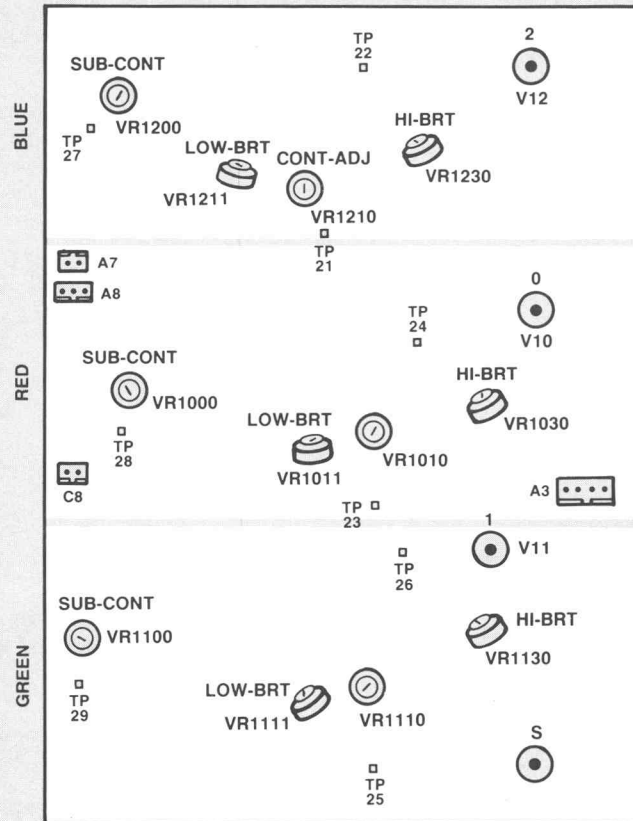
- (E)** Connect scope probe to appropriate test point and adjust as follows:

- TP27 and adjust VR1200 for 0.6V p-p
- TP28 and adjust VR1000 for 0.6V p-p
- TP29 and adjust VR1100 for 0.6V p-p
- TP23 and adjust CONTRAST control (VR1070) for 0.4V p-p

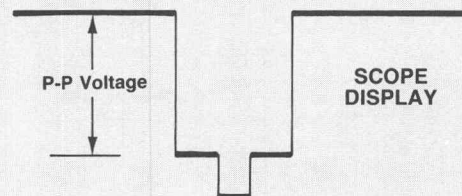
- (F)** Record voltage levels at TP21 and TP25.

- If TP21 is lowest, set its value to 0.4V p-p using the CONTRAST control (VR1070). Then adjust VR1010 (TP23) and VR1110 (TP25) back to 0.4V p-p.
- If TP25 is lowest, set its value to 0.4V p-p using the CONTRAST control (VR1070). Then adjust VR1210 (TP21) and VR1010 (TP23) back to 0.4V p-p.

VIDEO BOARD ADJUSTMENTS (TOP)



- (G)** Recheck the adjustments by performing Step **(A)**.

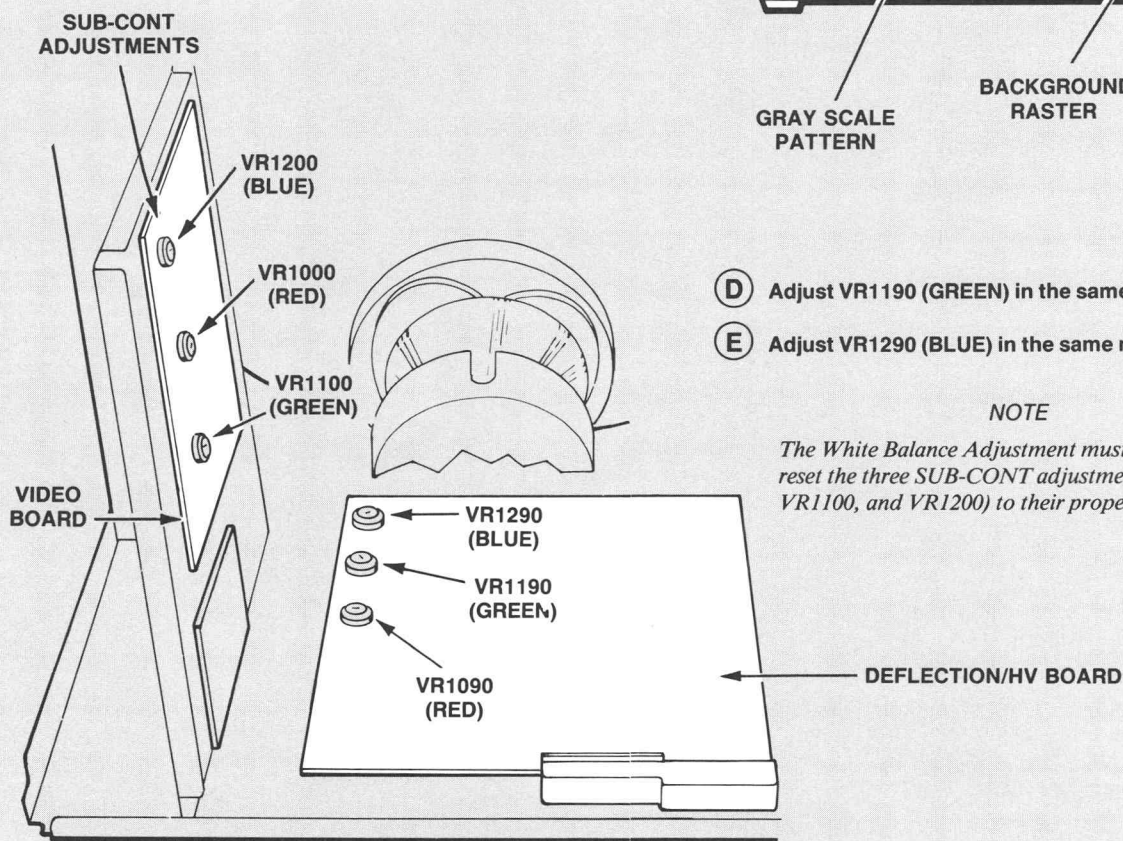


5644-89

Figure 5-21. Contrast Adjustments on Video Board (for 119-2387-00).

G2 Voltage and CRT Cutoff

- A** On the Video board, preset the three SUB-CONT adjustments (VR1000, VR1100, and VR1200) fully clockwise.
- B** Call up the GRAY SCALE pattern on the screen.
- C** Set VR1090 (RED) fully CCW. Note that horizontal and vertical overscan backgrounds appear to the right of the gray scale pattern. Slowly adjust VR1090 CW until both backgrounds just disappear (the horizontal overscan disappears last).



- D** Adjust VR1190 (GREEN) in the same manner.
- E** Adjust VR1290 (BLUE) in the same manner.

NOTE

The White Balance Adjustment must now be done to reset the three SUB-CONT adjustments (VR1000, VR1100, and VR1200) to their proper settings.

5644-90

Figure 5-22. G2 Voltage and CRT Cutoff (for 119-2387-00).

White Balance**NOTE**

Two adjustment procedures are presented for the White Balance adjustment. The first procedure uses only a TEKTRONIX Model J-16 Photometer with a TEKTRONIX Model P6503 Luminance Probe or equivalent. The second procedure provides an alternate procedure and requires additional test equipment; a Minolta Chroma Meter that reads chromaticity X and Y coordinates. Refer to Figure 5-23 on next page for both procedures.

NOTE

The three SUB-CONT adjustments (VR1000, VR1100, and VR1200 on the Video board) were preset fully CW during the previous "G2 Voltage and CRT Cutoff" procedure. Make sure these adjustments are preset as described before beginning the "White Balance" adjustment.

NOTE

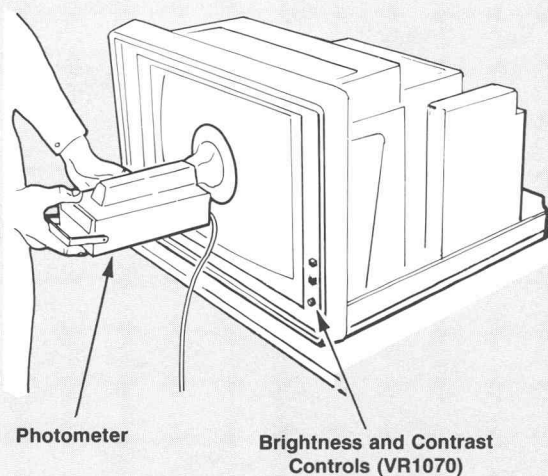
For the remaining steps (Steps 3 through 12) take photometer measurements in the center of the screen as shown in Figure 5-23.

3. Call up a green screen. ADJUST the green HI-BRT (VR1130) adjustment on the Video board for a photometer reading of 16.8 fL.
4. Call up a red screen. ADJUST the red HI-BRT (VR1030) adjustment on the Video board for a photometer reading of 4.8 fL.
5. Call up a blue screen. ADJUST the blue HI-BRT (VR1230) adjustment on the Video board for a photometer reading of 2.4 fL.
6. Call up a white screen and VERIFY a photometer reading of 24.0 fL. If necessary, repeat Steps 3 through 6 to achieve this reading.

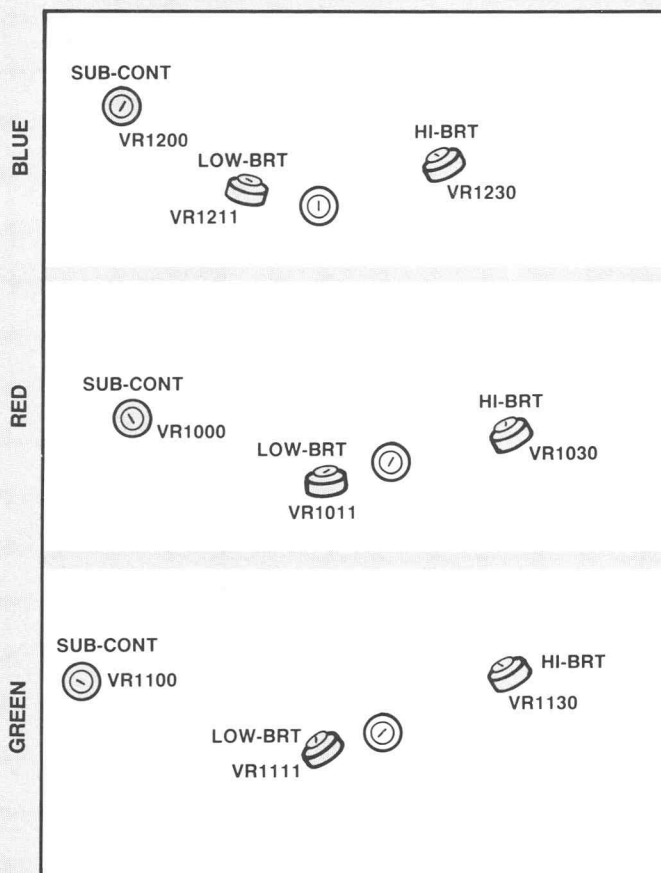
White Balance (Using J-16 Photometer). Perform the following procedure if you only have a J-16 Photometer:

1. Set BRIGHTNESS on the Display Module front panel to the center detent position.
2. Set CONTRAST on the front panel to a full CW position.

White Balance



VIDEO BOARD ADJUSTMENTS (TOP)



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Figure 5-23. White Balance (for 119-2387-00).

7. Call up a green screen. ADJUST the green SUB-CONT (VR1100) adjustment on the Video board for a photometer reading of 14.0 fL.
8. Call up a red screen. ADJUST the red SUB-CONT (VR1000) adjustment on the Video board for a photometer reading of 4.0 fL.
9. Call up a blue screen. ADJUST the blue SUB-CONT (VR1200) adjustment on the Video board for a photometer reading of 2.0 fL.
10. Call up a white screen and VERIFY a photometer reading of 20.0 fL. If necessary, repeat Steps 7 through 10 to achieve this reading.
11. Now, with the photometer still against the screen, PRESET the front panel's CONTRAST (VR1070) adjustment to give a photometer reading of 4.0 fL.
12. Then ADJUST the green, red, and blue LOW-BRT controls (VR1111, VR1011, and VR1211) to visually obtain a white screen.

White Balance (Using Minolta Chroma Meter). Perform the following procedure if you wish to use X and Y chromaticity coordinates to adjust white balance:

NOTE

This procedure provides an alternate method for setting colorimetry, but requires additional test equipment; a Minolta Chroma Meter that reads chromaticity X and Y coordinates.

1. Set BRIGHTNESS (VR1070) on the Display Module's front panel to the center detent position.
2. Call up a grid pattern.
3. Focus the center portion of the screen with the FOCUS adjustment on the Deflection/HV board.
4. Call up a white screen.
5. Set CONTRAST (VR1070) on the front panel to a full CW position.
6. Visually adjust the picture to white using the red, green, and blue HI-BRT adjustments (VR1030, VR1130, and VR1230). CIE Chromaticity coordinates must be at $X = 0.281$ and $Y = 0.311$ after adjustment.
7. Place the photometer in the center of the screen as shown and adjust the front panel CONTRAST control (VR1070) for a photometer reading of 31.0 fL.
8. Visually adjust the picture to white using the red, green, and blue SUB-CONT adjustments (VR1000, VR1100, and VR1200). CIE Chromaticity coordinates must be at $X = 0.281$ and $Y = 0.311$ after adjustment.
9. Place the photometer in the center of the screen and adjust the front panel CONTRAST control (VR1070) for a photometer reading of 4.4 fL.
10. Visually adjust the picture to white using the red, green, and blue LO-BRT adjustments (VR1011, VR1111, and VR1211). CIE Chromaticity coordinates must be at $X = 0.281$ and $Y = 0.311$ after adjustment.
11. Set CONTRAST (VR1070) on the front panel to a full CCW position. Check if the CIE Chromaticity coordinates are in the range of $X = 0.281 \pm 0.015$ and $Y = 0.311 \pm 0.015$. If the coordinates are out of the proper range, go to Step 5 and repeat all adjustments up through Step 11.
12. Set CONTRAST (VR1070) on the front panel to a full CW position. Check if brightness is in the range of $31.0 \text{ fL} \pm 1.5 \text{ fL}$. If brightness is out of the proper range, go to Step 5 and repeat all adjustments up through Step 12 while holding brightness to $31.0 \text{ fL} \pm 1.5 \text{ fL}$.

Section 6

MAINTENANCE

INTRODUCTION

This section contains the following major topics:

- Cleaning and preventive maintenance procedures for the terminal and keyboard.
- Disassembly and reassembly procedures required for trouble shooting, calibration, and repair access to the terminal.
- A summary of troubleshooting and corrective maintenance procedures for the terminal logic, low voltage power supply, and the Display Module.
- Self-test error messages for the Terminal Control board, Display Control board, and CX Interface board (for CX4111 terminal only).

More detailed servicing procedures, for component access, calibration, and troubleshooting are located in additional service manuals or technical data manuals. This additional information covers the GMA302 Display Module, the 119-2387-00 Display Module, the 4111 keyboard with thumbwheels, the 4111 keyboard with Joydisk, and the CX4111 keyboard. See "Related Documents," in Section 1, for a list of these manuals.

SAFETY CONSIDERATIONS

Before performing any of the maintenance procedures listed in this section, carefully read the Service Safety Summary at the front of this manual.

PREVENTIVE MAINTENANCE

The 4111 and CX4111 are designed to require very little routine or preventive maintenance. No routine lubrication or cleaning is required. If cleaning or maintenance is necessary (due to an adverse operating environment), perform these procedures on a yearly Preventive Maintenance schedule.

CLEANING AND PREVENTIVE MAINTENANCE

Read ALL warnings and cautions for this cleaning section before attempting any of the cleaning procedures given here.

CAUTION

To avoid damage to the plastics used in the Display Module and keyboard, do NOT use cleaning agents that contain benzene, acetone, toluene, xylene, or similar chemicals.

CAUTION

The following cleaning procedures use water with a mild detergent. Avoid getting water on any parts susceptible to water damage. Dry all parts thoroughly before applying power to the terminal. Drying times may be shortened by forced air drying at a maximum temperature of 165° F (60° C).

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Cleaning the Terminal and CRT Screen

Clean the external covers and crt face using a soft cloth dampened with a solution of mild detergent and water. A treated anti-static cloth applied to the crt face after cleaning may inhibit dust attraction and lengthen the interval between cleanings.

WARNING

Disconnect the line power cord before cleaning any parts inside the terminal. Dangerous voltages exist inside the terminal covers and may cause injury if contacted.

Occasionally, remove any accumulated dust from inside the terminal. Dust conducts electricity under high humidity conditions. The terminal interior is best cleaned with a vacuum cleaner. Remove any remaining dust with a soft bristle brush (paint brush) or a cloth dampened with a mild detergent and water solution. To clean narrow spaces, use a cotton-tipped applicator.

CAUTION

Static charges can be generated by a brush with synthetic bristles. Such static charges will damage solid state components, so use a brush with natural soft bristles. (Read the static protection tips in the Removal/Replacement Procedures, later in this section.)

Cleaning the Keyboards and Optional Mouse

Clean all loose debris from the keyboard and mouse by directing clean, dry, regulated, compressed air around all key pads, thumbwheels, Joydisk, mouse buttons, and the mouse ball cavity. See the Mouse Ball removal procedure (next heading), for instructions on removing the ball from its cavity. Clean all external cover surfaces of the keyboard and mouse by applying a soft cloth dampened with a solution of mild detergent and water. If liquids, such as coffee or soft drinks have entered the keyboard, refer to the Keyboard Technical Data manuals to open the keyboard for a more thorough cleaning.

Removing the Mouse Ball. The following steps are shown in Figure 6-1:

1. Loosen the ball retaining ring by turning the mouse upside down and inserting your fingers into the two recesses provided in the retaining ring.
2. Rotate the retaining ring CCW (in the direction of the arrows), until the ring stops, (about 45°).
3. Turn the mouse right side up over a soft protective pad, and gently tap on the top of the mouse until the retaining ring and ball fall out.
4. To reassemble, place the ball into the cavity; then, replace the retaining ring and rotate the ring CW (against the arrows) until you feel it enter the detent.

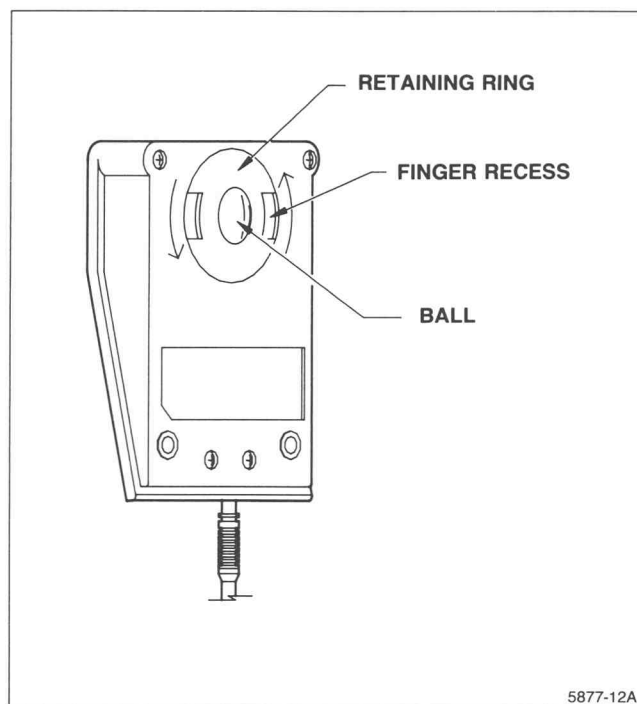


Figure 6-1. Removing the Mouse Retaining Ring and Ball.

ROUTINE VISUAL INSPECTION

Inspect the terminal occasionally for such defects as broken connections, damaged circuit boards, loose connectors, heat damaged parts, broken structural mounting features (circuit board retainers), and general mechanical fitness. If the terminal is used in a high vibration environment, pay particular attention to connectors, cable strain relief, and the crt mounting bracket.

The corrective procedure for most visible defects is repair or replacement; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the unit. It is important to correct the cause of overheating to prevent a recurrence of the damage.

POWER SUPPLY MAINTENANCE

The terminal's Low Voltage Power Supply (TLVPS) module contains automatic current limiting protection, and does not require routine maintenance. Normally, field repair of the TLVPS module means exchanging or replacing the entire module.

FUSE REPLACEMENT

Terminals with the GMA302 Display Module contain two line fuses. The TLVPS has a 6A fuse for fire protection. The Low Voltage Power Supply board on the GMA302 Display Module has a 4A fuse for its incoming AC power.

Terminals with the newer 119-2387-00 Display Module have only the 6A line fuse on the TLVPS.

Replacing the TLVPS Fuse

The line fuse in the TLVPS module is located at the bottom-rear corner of the module's circuit board. This fuse's only function is that of fire protection, in the event of a malfunction or overload. If the fuse burns out, first check for a possible overload that should be corrected. Then replace the fuse with a 6A (250A medium-blow) fuse. See Table 6-1. This fuse is referred to as F1 on the circuit board, in the schematic, and in the Replaceable Electrical Parts list (Section 8).

Replacing the Line Fuse in the GMA302 Display Module

The GMA302 Display Module's Low Voltage Power Supply board has a line fuse for incoming AC power. See Table 6-1. This fuse (F125) is located in the top-left corner of the Low Voltage Power Supply board (next to the J3 connector). When replacing this fuse, use only a 4A (250V fast-blow) fuse.

The 119-2387-00 Display Module

The 119-2387-00 Display Module does not have a line fuse. It takes its AC power from the TLVPS module.

Table 6-1
LINE FUSE REPLACEMENT VALUES

Fuse Location	Voltage Selected	Fuse Amperage
TLVPS Module (F1)	115V (nominal)	6A (med-blow)
	230V (nominal)	6A (med-blow)
GMA302 Low Voltage Power Supply Board (F125)	115V (nominal)	4A (fast-blow)
	230V (nominal)	4A (fast-blow)

REMOVAL/REPLACEMENT PROCEDURES

This part of the maintenance section describes procedures for removing and disassembling modules or major parts of the terminal. Some procedures follow a specific order that prepares for the next removable assembly. The following procedures tell you how to:

- Access ROMs behind the ROM access door
- Access the interior of the terminal
 - Terminal top cover removal
 - Terminal rear cover removal
- Remove the terminal's logic boards
 - Terminal Control board
 - RAM Option board (mounted on the Terminal Control board)
 - Display Control board
 - Crosshair Cursor board (mounted on early versions of the Display Control Board)
 - Terminal Low Voltage Power Supply (TLVPS)
 - CX Interface board (for CX4111 terminals only)
- Open the GMA302 Display Module for calibration
 - Fan assembly
- Remove the GMA302 Display Module's replaceable assemblies
 - Video and Video Converter boards
 - Convergence board
 - Deflection board
 - Low Voltage Power Supply board
 - High Voltage Power Supply board
 - Front Bezel
 - CRT Socket board
 - CRT Assembly
- Open the 119-2387-00 Display Module for calibration
 - Fan assembly
 - Display Module Top Panel
 - Display Module Rear Panel
- Remove the 119-2387-00 Display Module's replaceable assemblies
 - Display Low Voltage Power Supply (DLVPS)
 - AC Distribution board
 - CRT Socket board
 - Front Bezel
 - CRT
 - Video board
 - Deflection/HV board
 - Degauss Control board
- Open the Keyboards
 - Keyboard with thumbwheels
 - Keyboards with Joydisk

These procedures require only those tools common to a service tool kit. An additional set of procedures at the end of this section describes repair and replacement of components or smaller assemblies in the terminal.

Unless a specific reassembly procedure is given, perform assembly by following the disassembly procedure in reverse order.

NOTE

Unless otherwise stated, all screws mentioned in these procedures are POZIDRIVE®.

ELECTROSTATIC DISCHARGE PRECAUTIONS

This product contains components that are highly sensitive to electrostatic discharge. To prevent damage to such components and to maintain product reliability, **DON'T** touch or remove the circuit boards or components from the terminal until the following conditions are met.

Safe Handling of Static-Sensitive Components

Handle all static-sensitive components (such as RAMs, ROMs, EEPROMs, custom logic arrays, etc.) in a static-safeguarded area capable of controlling static charge on conductive materials, people, and non-conductive materials.

Transportation of Static-Sensitive Components

Transport all static-sensitive components in static-shielded containers/packages. A "static shield" container will protect its contents from static discharge and from electrostatic fields.

ROM ACCESS DOOR AND ROM REPLACEMENT

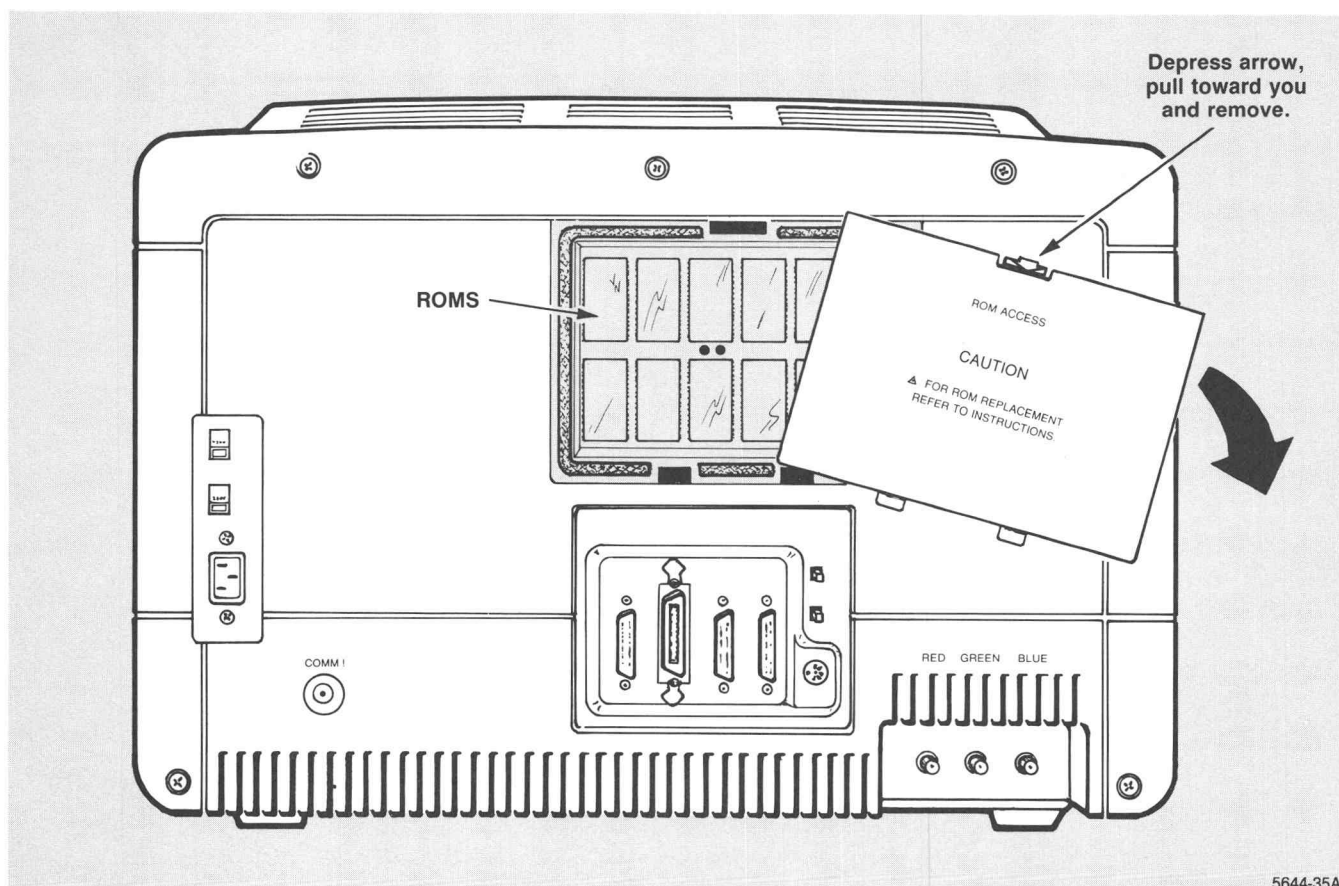
The ROM access door is located on the rear panel of the terminal. To open this door, press on the tab (in the direction of the arrow) and pull the door toward you. See Figure 6-2. To remove ROMs, use a flat tip screwdriver to pry the top and bottom of the ROMs from their holders. Replacement ROMs are keyed so they cannot be installed upside down.

CAUTION

The ROMs are highly sensitive to electrostatic discharge. Before touching the ROMs, remove the static electricity from yourself by touching the silver metal plate on the rear of the terminal with your finger.

NOTE

The first time you change the ROMs, it may be difficult to remove them from their sockets. However, with gentle pressure, the ROMs should come free.



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Figure 6-2. ROM Access Door.

ACCESSING THE INTERIOR OF THE TERMINAL

Removing the Terminal's Top Cover

The terminal's wrap-around top panel is fastened by five screws in the rear, and retainer tabs in the front. The top panel is a three-piece unit, but is designed for removal as one piece. Remove the five screws shown in Figure 6-3. Then pull the top panel back and up; this will release the retainer tabs in front. Now, lift off the cover.

Removing the Terminal's Back Panel

To repair and service the terminal you must also remove the back panel. This panel contains the ROM Access door. The panel attaches to the terminal with two screws as shown in Figure 6-4.

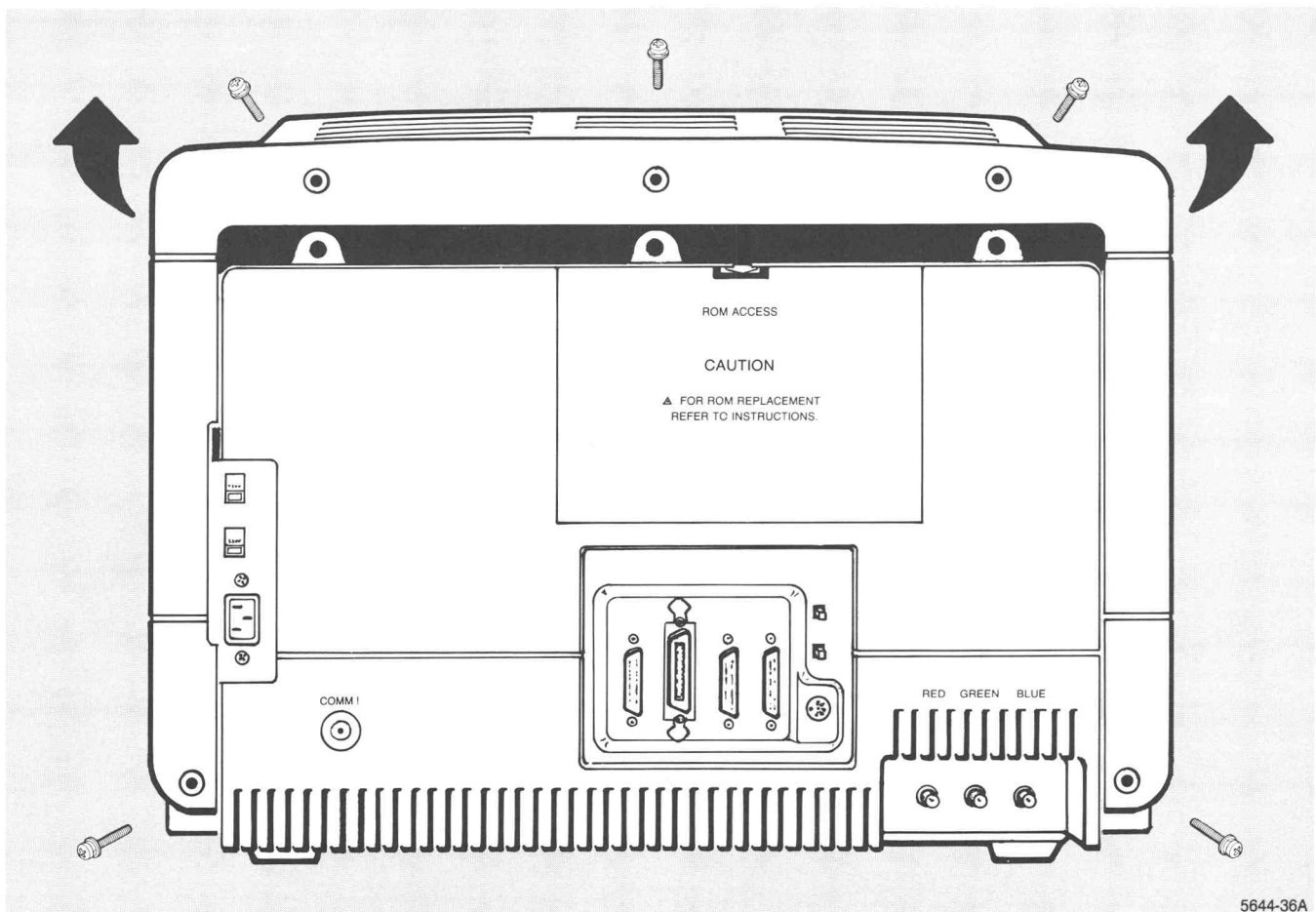


Figure 6-3. Top Cover Removal.

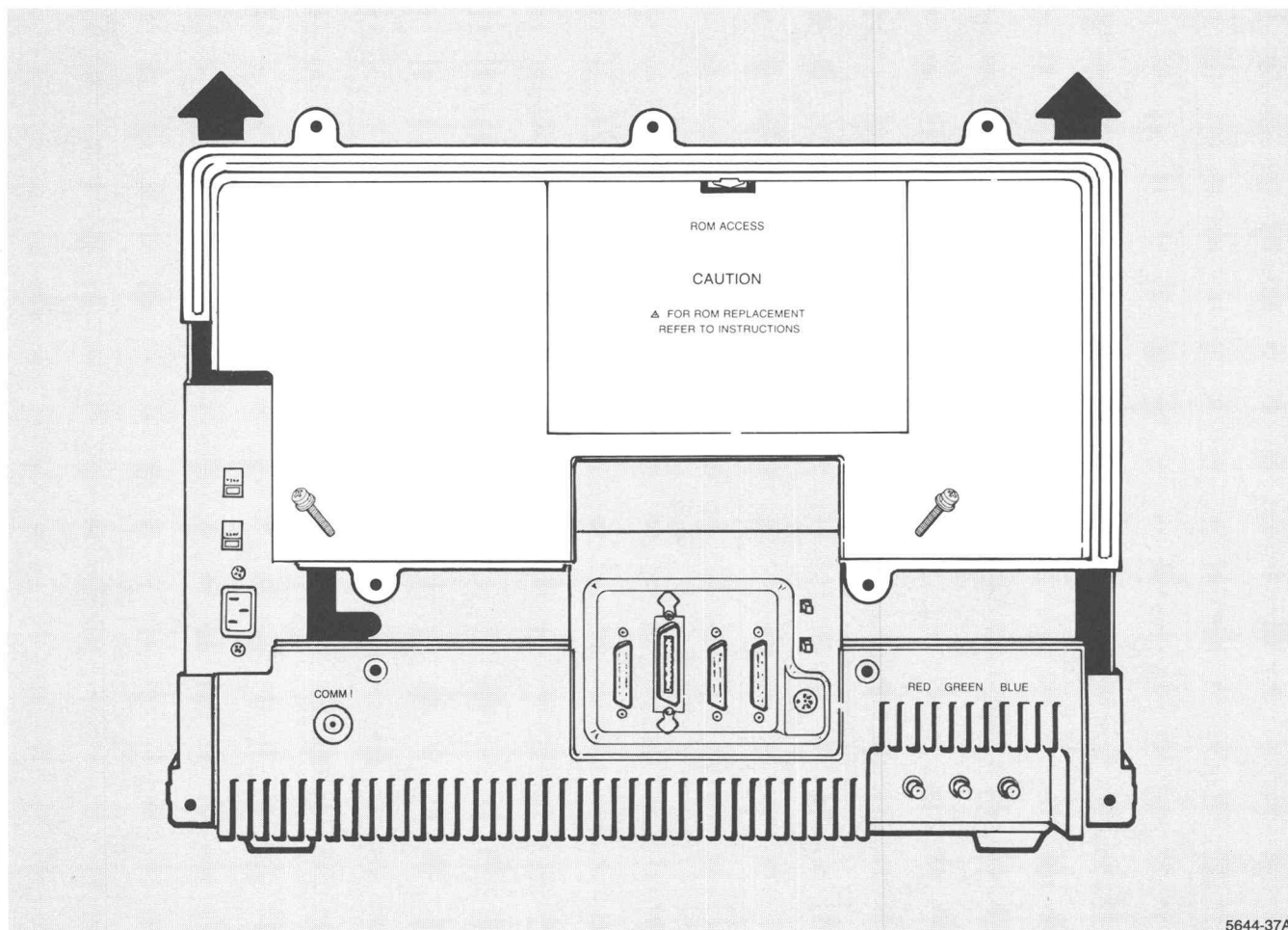


Figure 6-4. Back Panel Removal.

REMOVING THE TERMINAL'S LOGIC BOARDS AND POWER SUPPLY

Removing the Terminal Control, RAM Option, Display Control, and Crosshair Cursor Boards

CAUTION

Read "Safe Handling of Static-Sensitive Components" (previous heading) before performing this and the following procedures.

The Terminal Control and Display Control boards are mounted across the rear and side of the terminal (instead of in a card cage). The RAM Option board is mounted to the rear of the Terminal Control board. The Crosshair Cursor board is mounted to the front of the early version Display Control board. Either the Terminal Control or Display Control board may be removed first. The removal procedures are depicted in Figures 6-5 through 6-7. To remove a board:

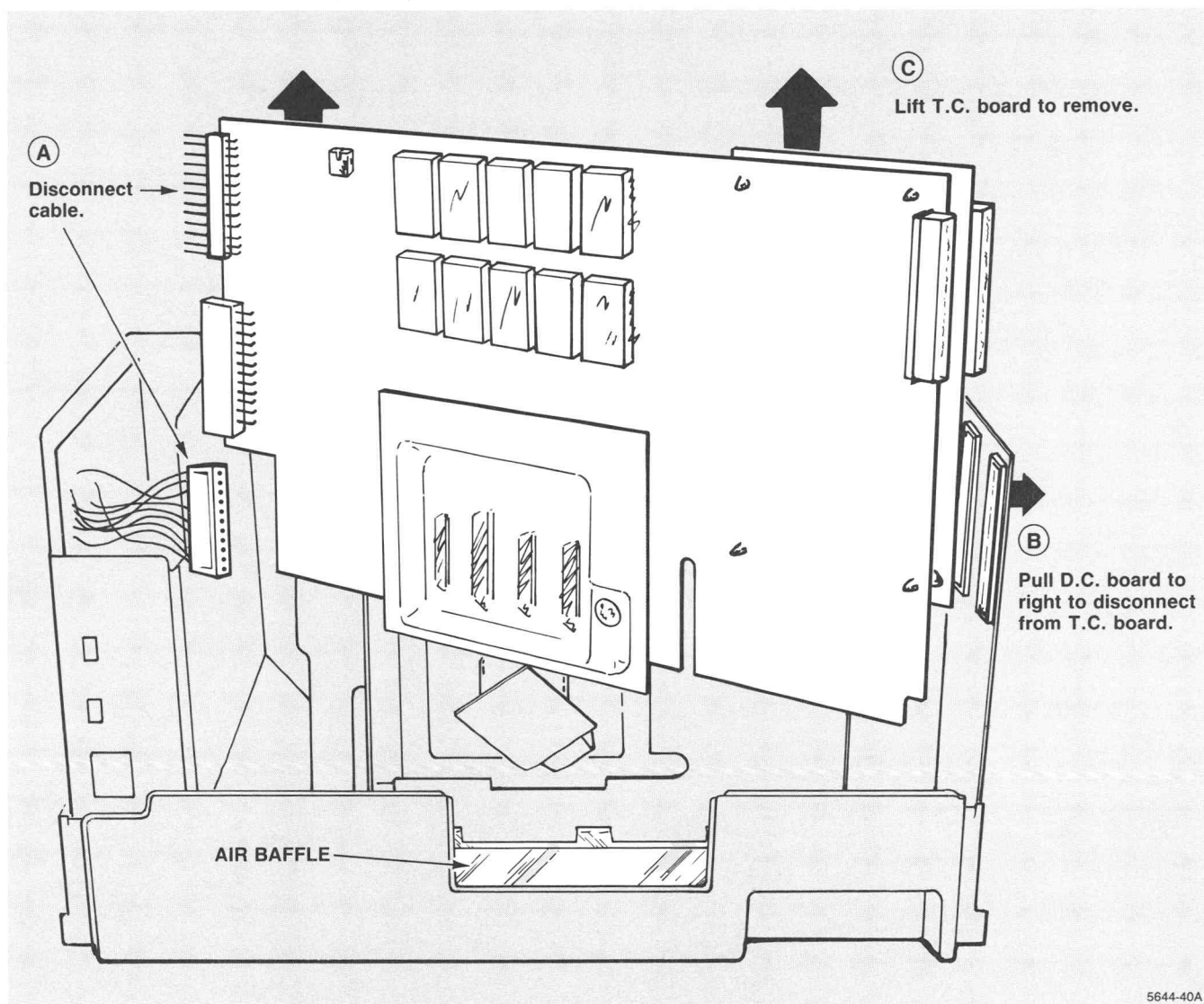


Figure 6-5. Removal of the Terminal Control Board.

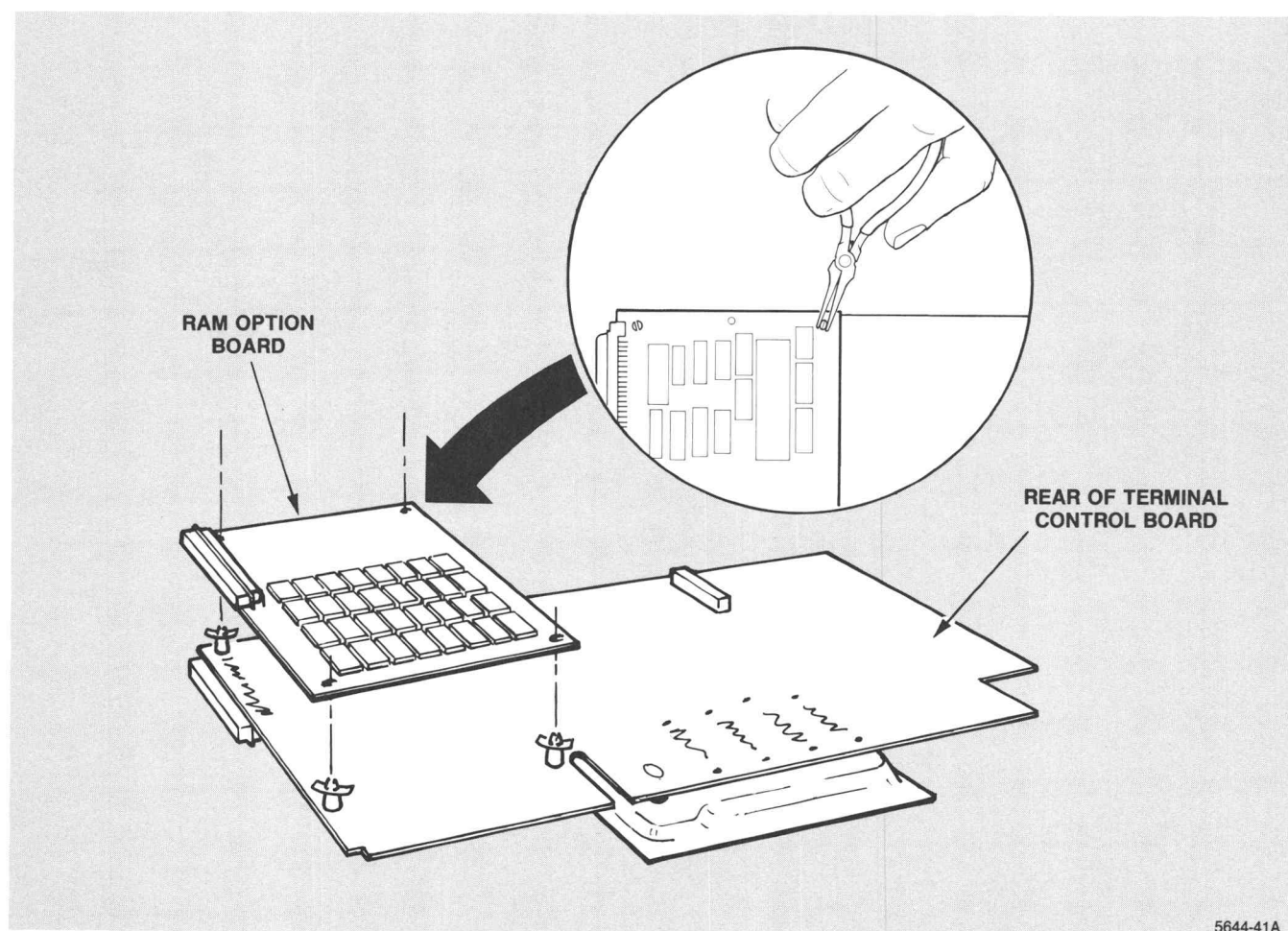
1. Refer to the appropriate figure and unplug any ribbon cables or plugs that connect to the board.
2. Lift the board up out of its retainer slots, and then remove from the terminal.

CAUTION

Before reinstalling the Terminal Control, RAM Option, or Display Control boards in the terminal, observe the following. First, see that all pins on the 96-pin connectors are straight. Then, place the boards in the terminal, align the connectors, and carefully push them together. Carelessness can easily result in bent pins, which may cause the power supply to "crowbar" (which shuts down the supply).

NOTE

If you are removing the Terminal Control board, lift it straight up and out of the terminal. (The rear connector panel is mounted to this board, and will slide in vertical grooves that secure it to the back of the terminal cabinet.)



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Figure 6-6. Removal of the RAM Option Board.

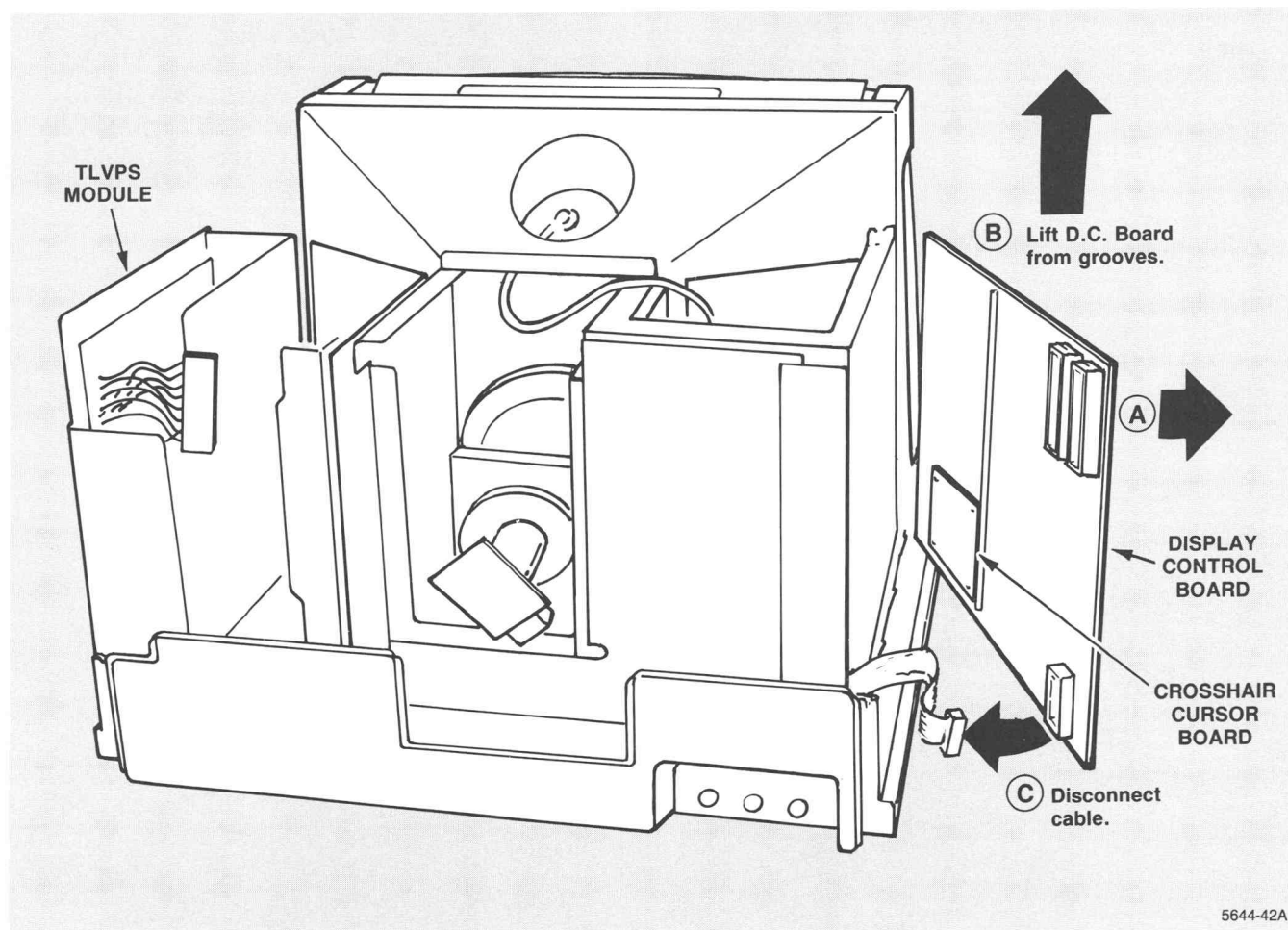


Figure 6-7. Removal of the Display Control and Crosshair Cursor Boards.

Removing the Terminal Low Voltage Power Supply (TLVPS) Module

Remove the Terminal Control board first. The TLVPS module removal procedure is depicted in Figure 6-8.

NOTE

You may remove the rod that connects the POWER switch (mounted on the TLVPS module) to the power button (on the front of the terminal). This rod attaches to the switch via a fork that straddles the switch plunger. Pull forward and the fork will release from the switch.

Removal of the rod for the DEGAUSS switch is done in the same manner.

To remove power connectors, squeeze both catch-levers and pull the connector away from the receptacle.

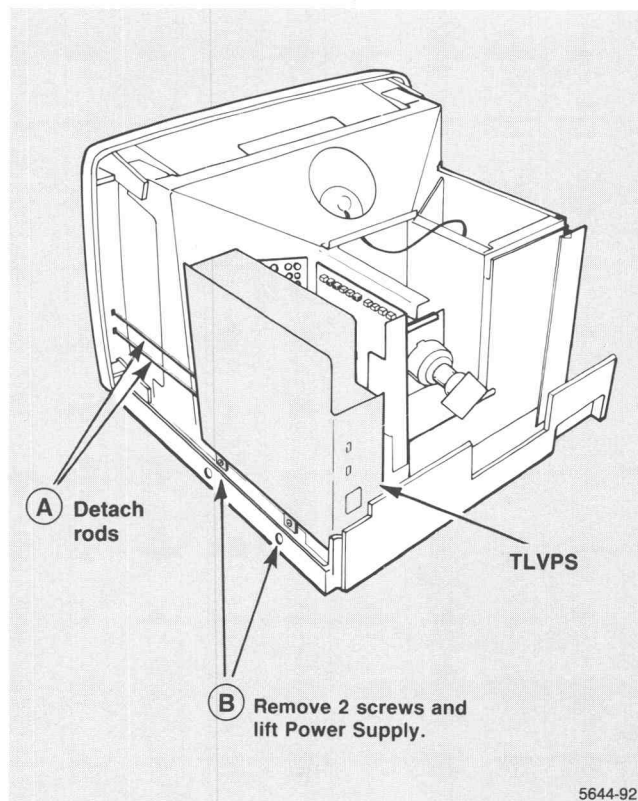


Figure 6-8. Removal of the Terminal Low Voltage Power Supply.

Removing the CX Interface Board

The CX Interface board (in the CX4111 only) is mounted between the Terminal Low Voltage Power Supply and the Display Module (see Figure 6-9). To remove the CX Interface board, disconnect the CX Interface connector (P13) from the Terminal Control board. Then unscrew the mounting nut for the coax connector labeled "COMM"; push this connector with its attached board into the terminal. Remove the Terminal Low Voltage Power Supply as shown in Figure 6-8. Then detach the CX Interface board by removing the four screws. Lift the CX Interface board assembly out of the terminal.

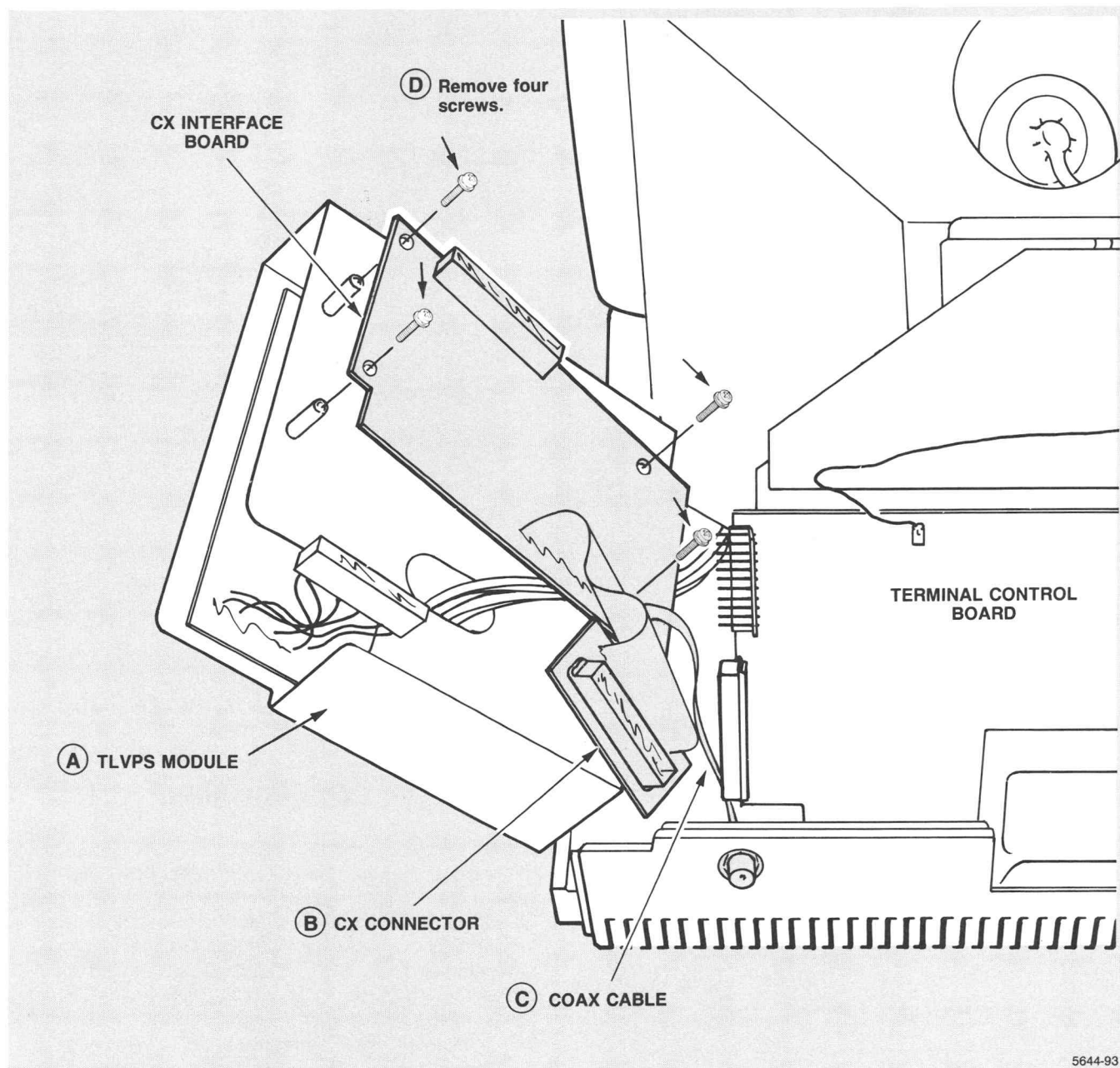


Figure 6-9. Removal of the CX Interface Board.

OPENING THE GMA302 DISPLAY MODULE FOR CALIBRATION

To calibrate the Display Module, first remove the fan assembly; this provides access to the Display Module adjustments.

Fan Assembly Removal

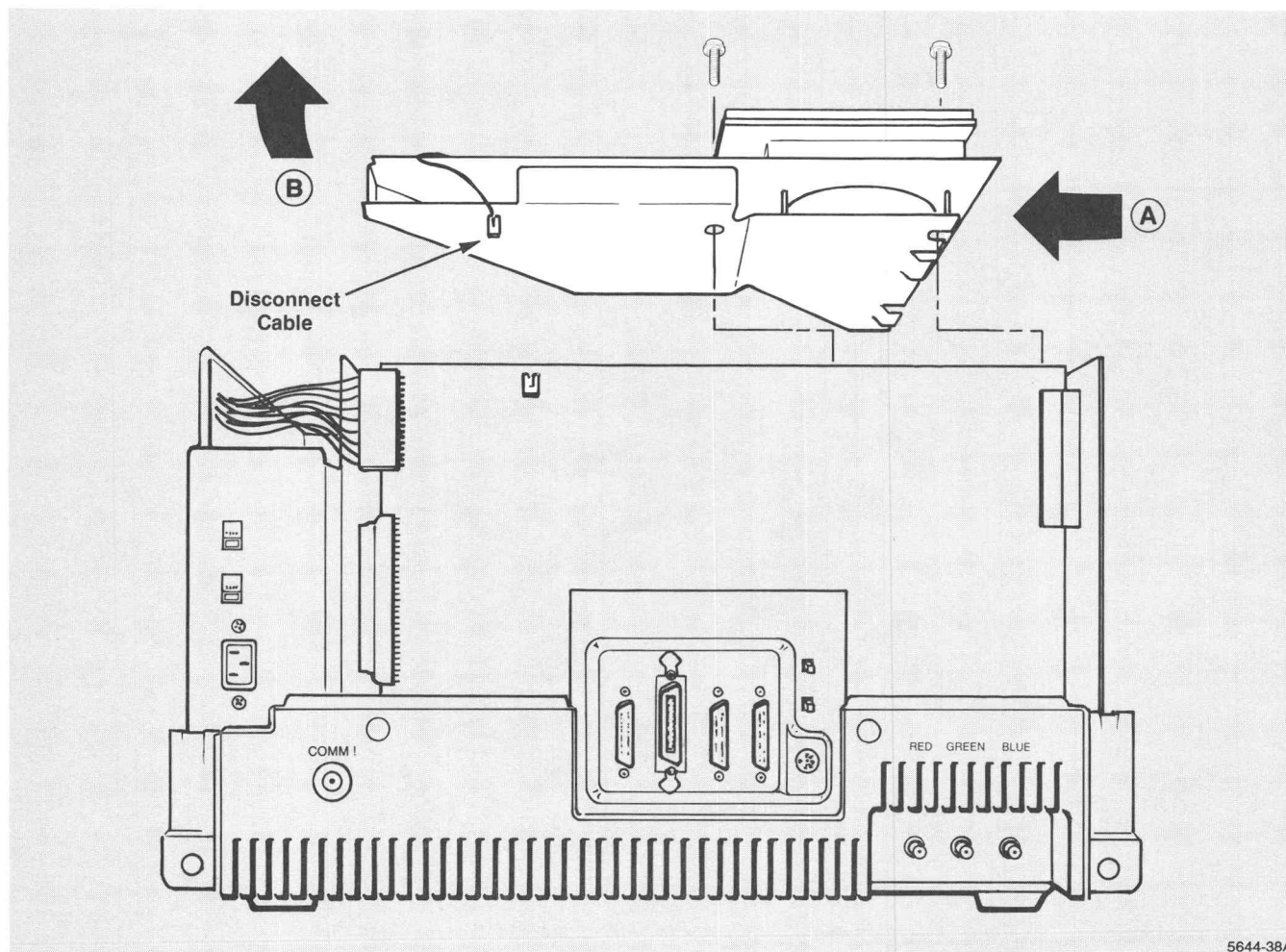
See Figure 6-10 during the following removal steps:

1. Unplug the fan wiring connector (J128) from the Terminal Control board.

2. Remove the retaining screw from the center of the assembly.
3. Slide the fan assembly toward the TLVPS module until the retaining tabs release. Then, lift the assembly away from the terminal.

NOTE

Before reinstalling the fan, be sure the retaining tabs are slid UNDER the chassis to secure the fan assembly.



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Figure 6-10. Removing The Fan Assembly (GMA302).

REPLACEABLE ASSEMBLIES OF THE GMA302 DISPLAY MODULE

As a general strategy, you may remove any Display Module circuit board without removing the crt. To make access easier, first remove the fan assembly, then remove the previously described terminal logic boards (Terminal Control, Display Control, and RAM Option boards).

Removing the Video and Video Connector Boards

Refer to Figure 6-11 to remove the Video board and the Video Connector board.

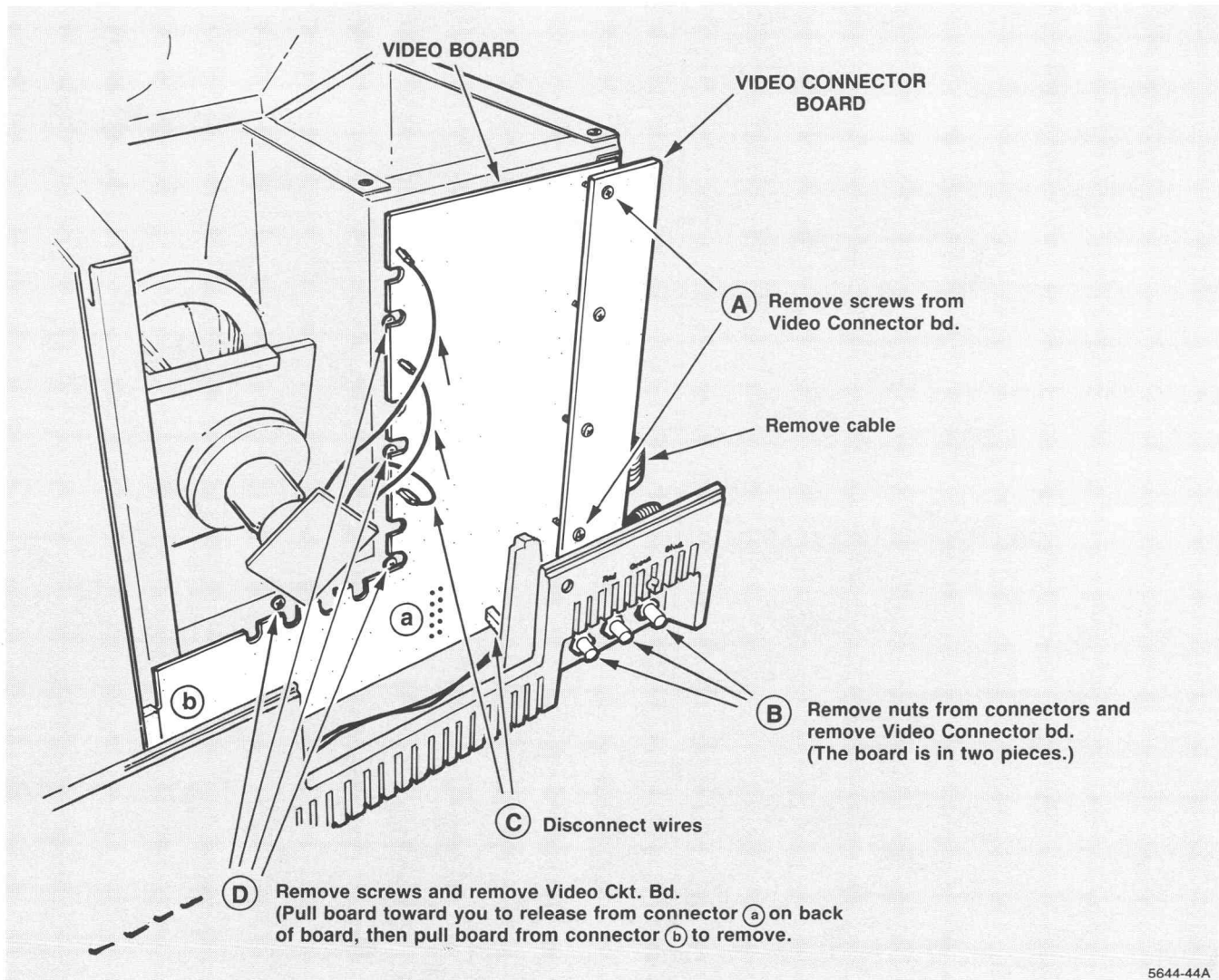


Figure 6-11. Removing the Video and Video Connector Boards (GMA302).

Removing the Remaining GMA302 Circuit Boards

Refer to Figure 6-12 to remove the Convergence and Deflection boards.

WARNING

Lethal voltages are present on the HV anode cable. Discharge this connection before removing the High Voltage Power Supply.

Refer to Figure 6-13 on next page to remove the Low Voltage Power Supply board and High Voltage Power Supply board.

Front Bezel Removal

See Figure 6-14 to remove the front bezel that surrounds the crt and contains the BRIGHTNESS, POWER, and DEGAUSS controls. The bezel attaches with four screws (two in each side).

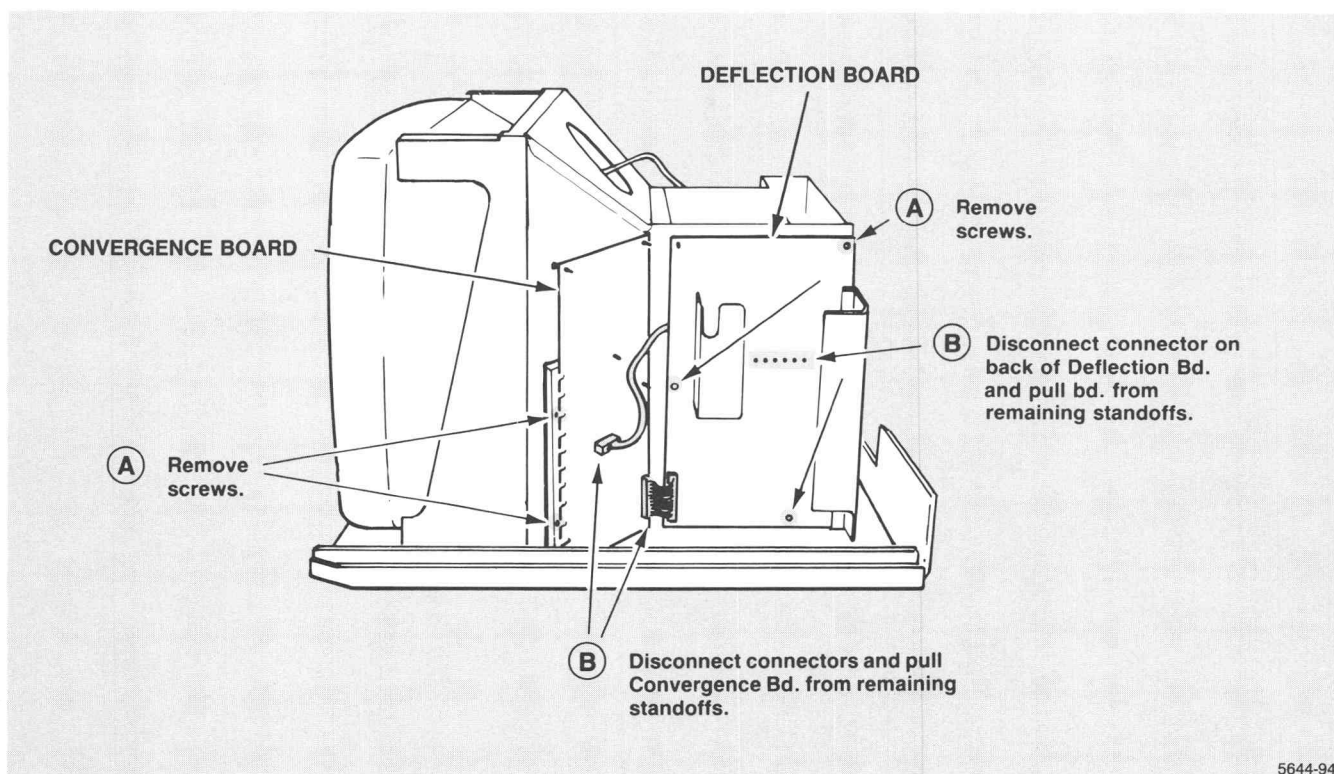


Figure 6-12. Removing the Convergence and Deflection Boards (GMA302).

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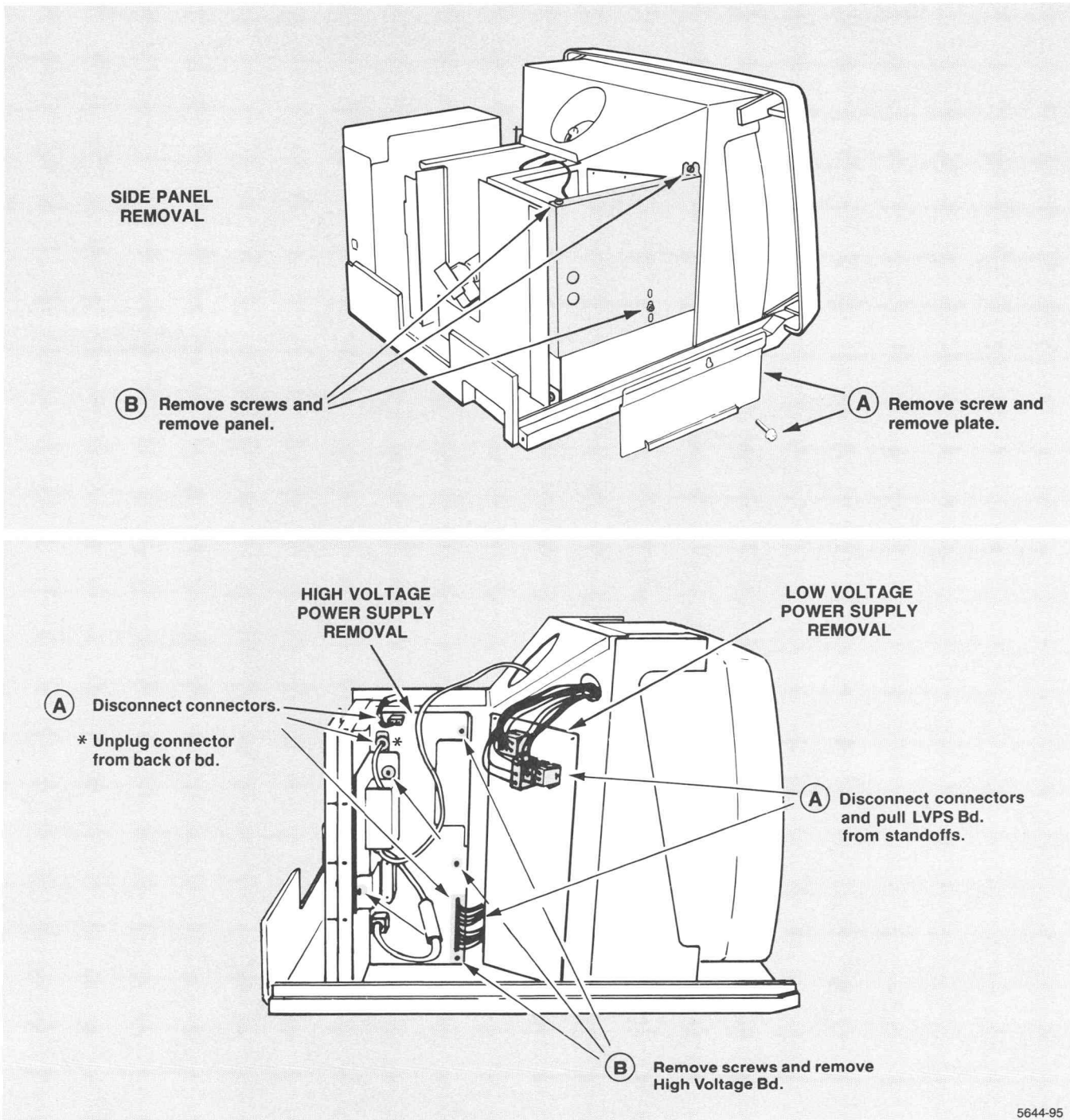
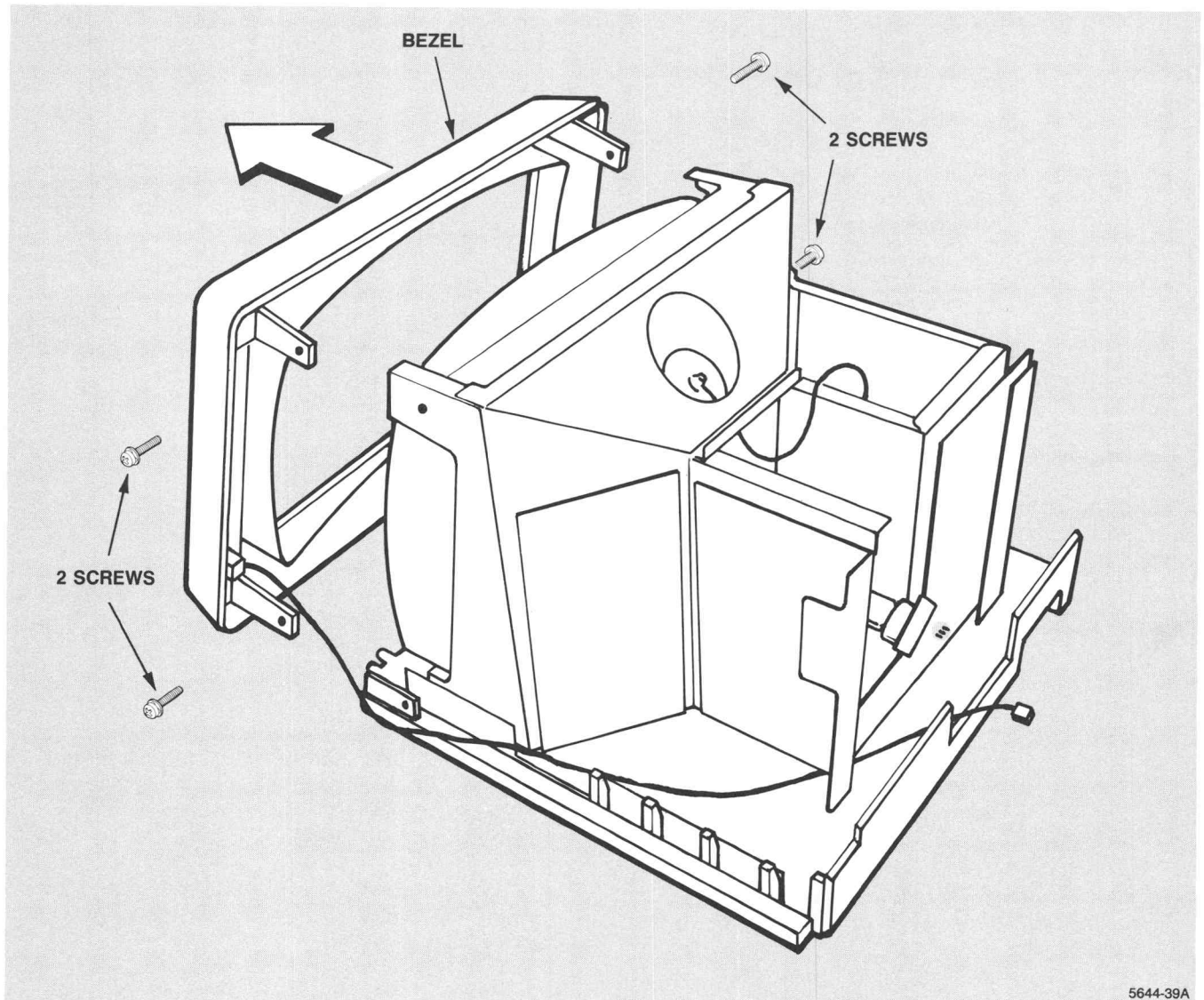


Figure 6-13. Removing the Low Voltage Power Supply and High Voltage Power Supply Boards (GMA302).



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Figure 6-14. Removing the Front Bezel.

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Removing the Socket Board

The Socket board mounts to the rear plug on the crt (see Figure 6-15).

WARNING

The crt socket is quite vulnerable to damage. Use caution when working around it.

1. Remove the screw retaining the ground clip on the Socket board.
2. Unplug all connectors. Pull the wires and connectors through the pass-through hole in the chassis.
3. Gently pry off the Socket board. If silicon adhesive was used to secure the board to the crt, peel it off with a knife.

CRT Removal

Refer also to Figure 6-15 during the following procedure:

WARNING

Lethal voltages are present at the High Voltage anode on the crt. Discharge this HV connection before performing the following procedure. Bodily contact with high voltages may cause shock, injury, or death.

1. (A) Discharge the High Voltage anode button on the crt several times; see preceding WARNING. Then remove the High Voltage anode cable from its connector button at the front of the crt.
2. (B) Unplug the deflection yoke cable from J52 on the Deflection board.
3. (C) Unplug the Socket board from the crt (if not already removed). A silicon adhesive may have been used to secure the Socket board to the crt; if so, careful use a knife to peel the gum away from the Socket board.

4. (D) Unplug the convergence cables from J60 on the Convergence board. Pull the convergence cable wires through the pass-through hole in the chassis.

NOTE

The yoke assembly and the Ring-Magnet assembly are part of the crt, and should not be removed from the crt. Use care not to bump the Ring-Magnet assembly.

5. Place a soft pad on the bench-top and in front of the crt. (When removed, the crt's face will rest on this protective pad.)

WARNING

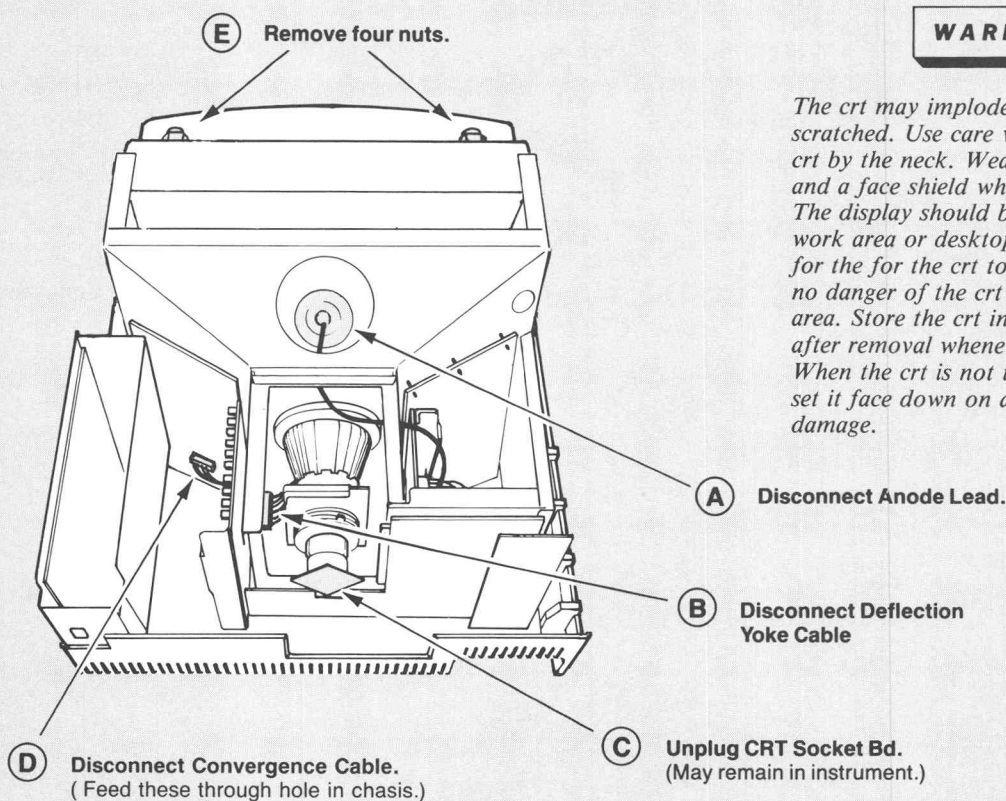
The crt may be damaged by careless handling when removing it from the terminal. Protect it from sharp, solid objects. If the crt cracks and implodes, serious personal injury is likely. It is also wise to discharge the crt anode button to the outside DAG coating just before handling.

6. (E) Remove the four nuts and washers that clamp the front corners of the crt to the Display Module chassis. Place the nuts, washers, and screws in a labeled container (to prevent misplacing them or confusing them with other hardware).
7. (F) Rock the crt forward as shown. Then pull the crt out of the front of the Display Module, and lower it onto the protective pad.

To install the crt, follow the previous steps in reverse order.

WARNING

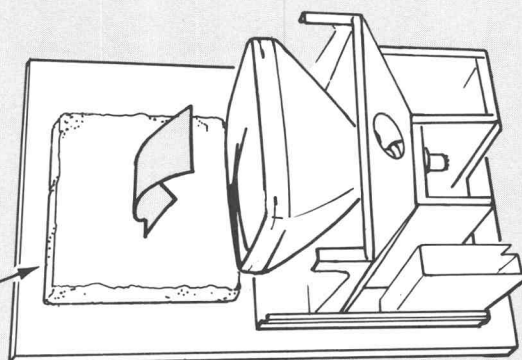
Before handling any crt (new or old), always discharge the crt anode button to the outside DAG coating. A long-term charge effect may leave enough energy at the anode slip-on connection to cause a dangerous shock even though the tube was recently discharged.


WARNING

The crt may implode if it is struck or scratched. Use care when handling the crt by the neck. Wear protective clothing and a face shield when handling the crt. The display should be placed on a stable work area or desktop, with adequate space for the crt to be removed with no danger of the crt falling from the work area. Store the crt in a shipping carton after removal whenever possible. When the crt is not in a shipping carton, set it face down on a soft pad to prevent damage.

F Carefully remove CRT as shown.

Place CRT face down on pad to prevent scratching.



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Figure 6-15. Removing the CRT for the GMA302 Display Module.

Removing the Convergence Coil Set

The convergence coils are mounted on two circuit boards that are fastened together and straddle the neck of the crt. If you need to remove this assembly, follow this procedure while referring to Figure 6-16. This procedure assumes the crt is removed.

1. Swing up the fastener-arm that hooks the two halves of the Coil board together. Then let the halves open out away from the crt (the lower part of the assembly contains a hinge point).
2. Remove the Coil-Set assembly.

When replacing the Coil Set assembly, use care to not break off the fastener hook that joins the top halves of this assembly. Also, plug the Socket board back onto the crt, and reconnect the coil wires.

Removing the Display Module from the Terminal

The Display Module mounts to the terminal with eight screws. One screw is located in each corner of the Display Module's base. Two screws in each side of the chassis (near the front of the crt) fasten the terminal's front bezel to the Display Module. Figure 6-17 shows the locations of the four corner screws on the bottom of the Display Module.

The following procedure assumes the terminal has all components installed except the top cover, back panel, and fan assembly.

WARNING

Lethal voltages are present at the High Voltage anode on the crt. Discharge this HV connection before performing the following procedure. Bodily contact with high voltages may cause shock, injury, or death.

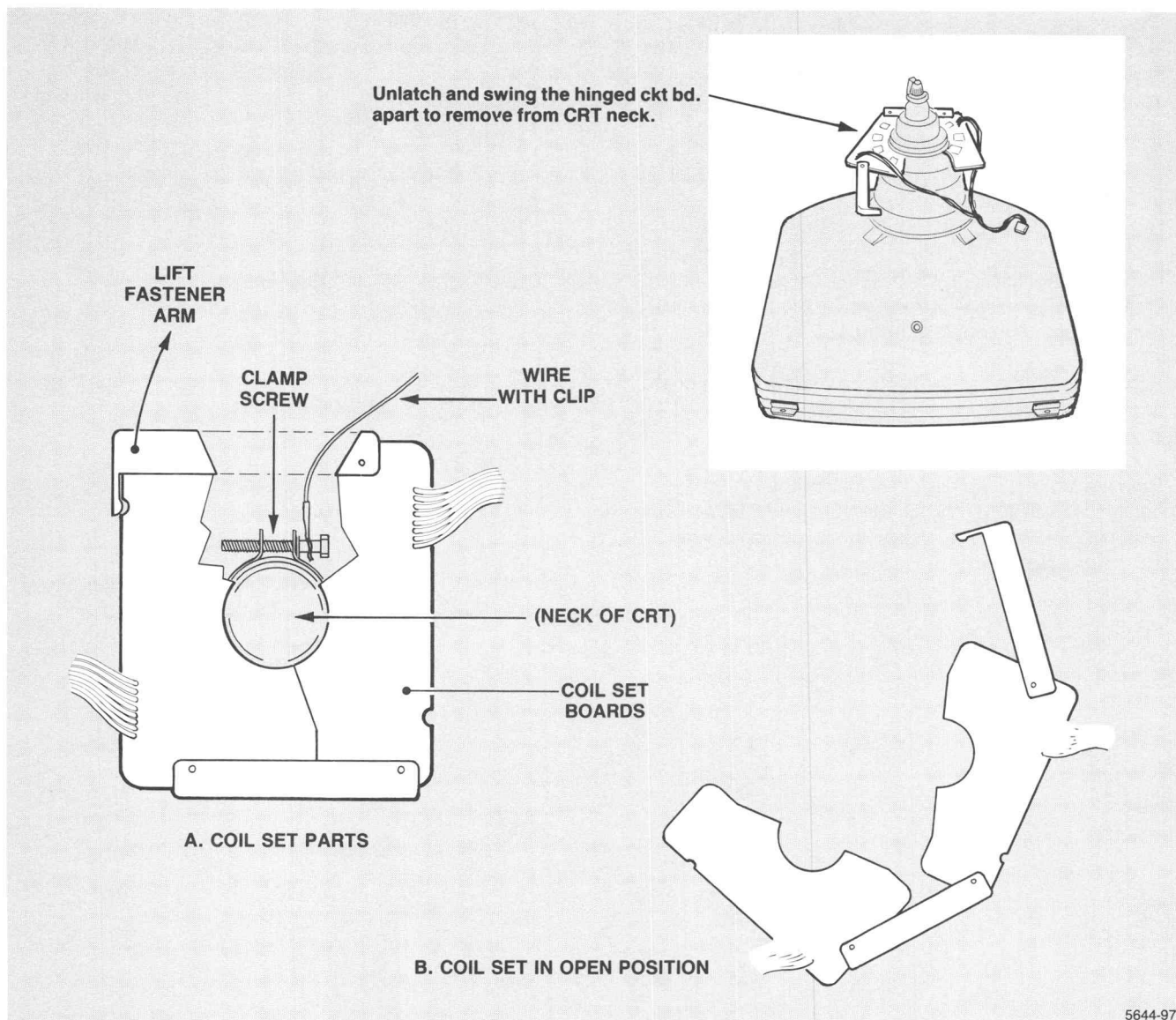


Figure 6-16. Removing the Convergence Coil Assembly (GMA302).

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1. Discharge the high voltage anode button on the crt. Using an insulated screwdriver, slip the blade under the rubber anode-cover; then lay the screwdriver shaft against the grounded metal frame.
2. Disconnect the ground lug from the rear panel connector plate on the Terminal Control board assembly.
3. Unplug the two Display Module connectors to the TLVPS. Unplug the TLVPS connector to the Terminal Control board. Disconnect the two front panel connectors from the Display Module. Disconnect any remaining connectors to or from the Display Module.
4. Remove the Terminal Control board, RAM Option board, and Display Control boards. Also remove the TLVPS module and the CX Interface board (if installed).
5. Remove the front bezel that surrounds the crt and contains the BRIGHTNESS, POWER, and DEGAUSS controls. This bezel attaches with four screws (two in each side). Refer back to Figure 6-14.
6. Remove the BRIGHTNESS control from the back side of the bezel by spreading the retainer forks that slip over the top and bottom of this control. This releases the potentiometer from the back side of the bezel, while the knob remains attached to the front of the bezel.
7. Unscrew the four Display Module base mounting screws; these screws thread into brass inserts in the base of the terminal.
8. Unplug any remaining Display Module connecting cables.



Exercise care when lifting the Display Module to avoid back injury. Two people are best for lifting the Display Module.

9. Now, lift the Display Module out of the terminal.

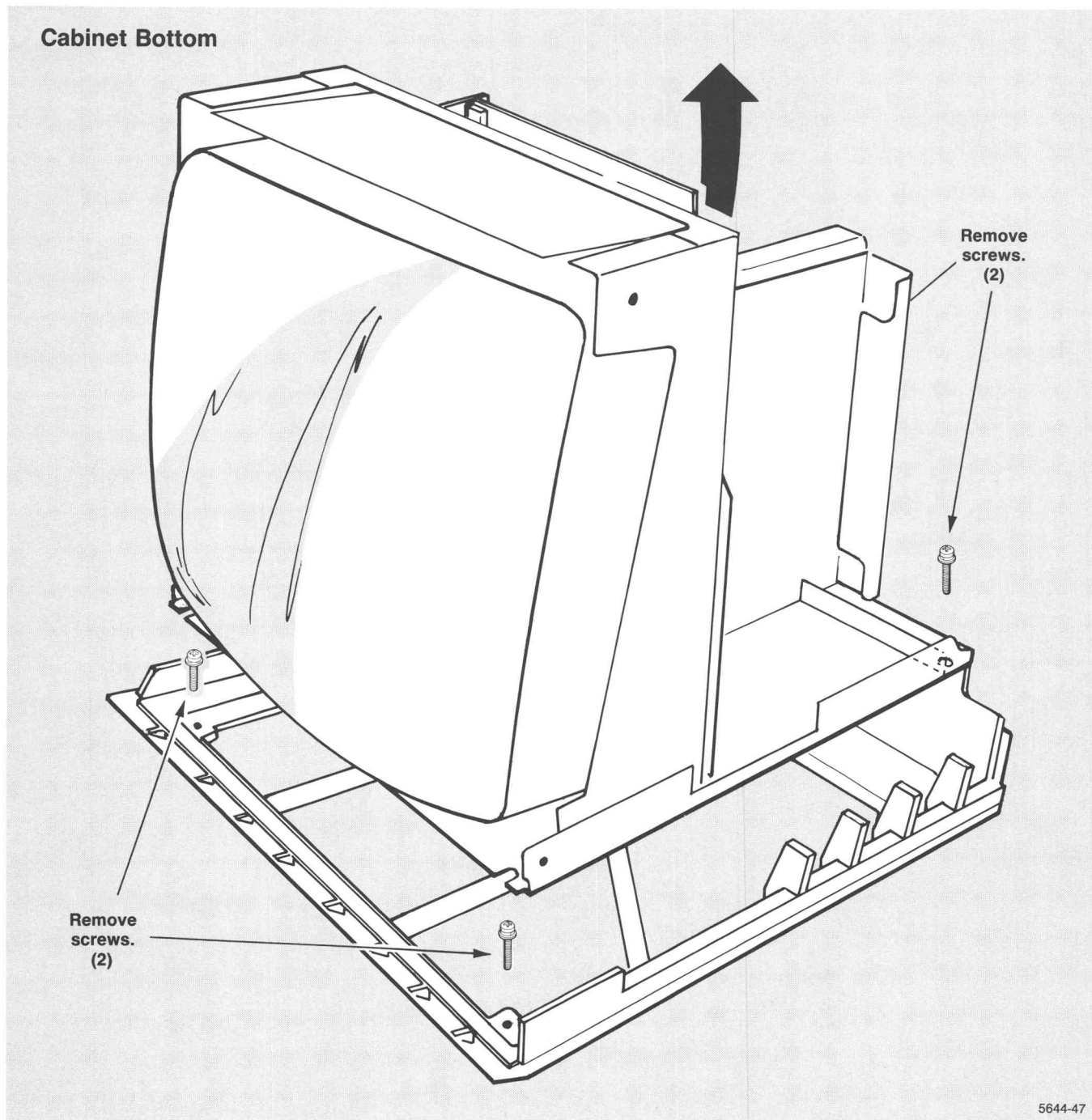


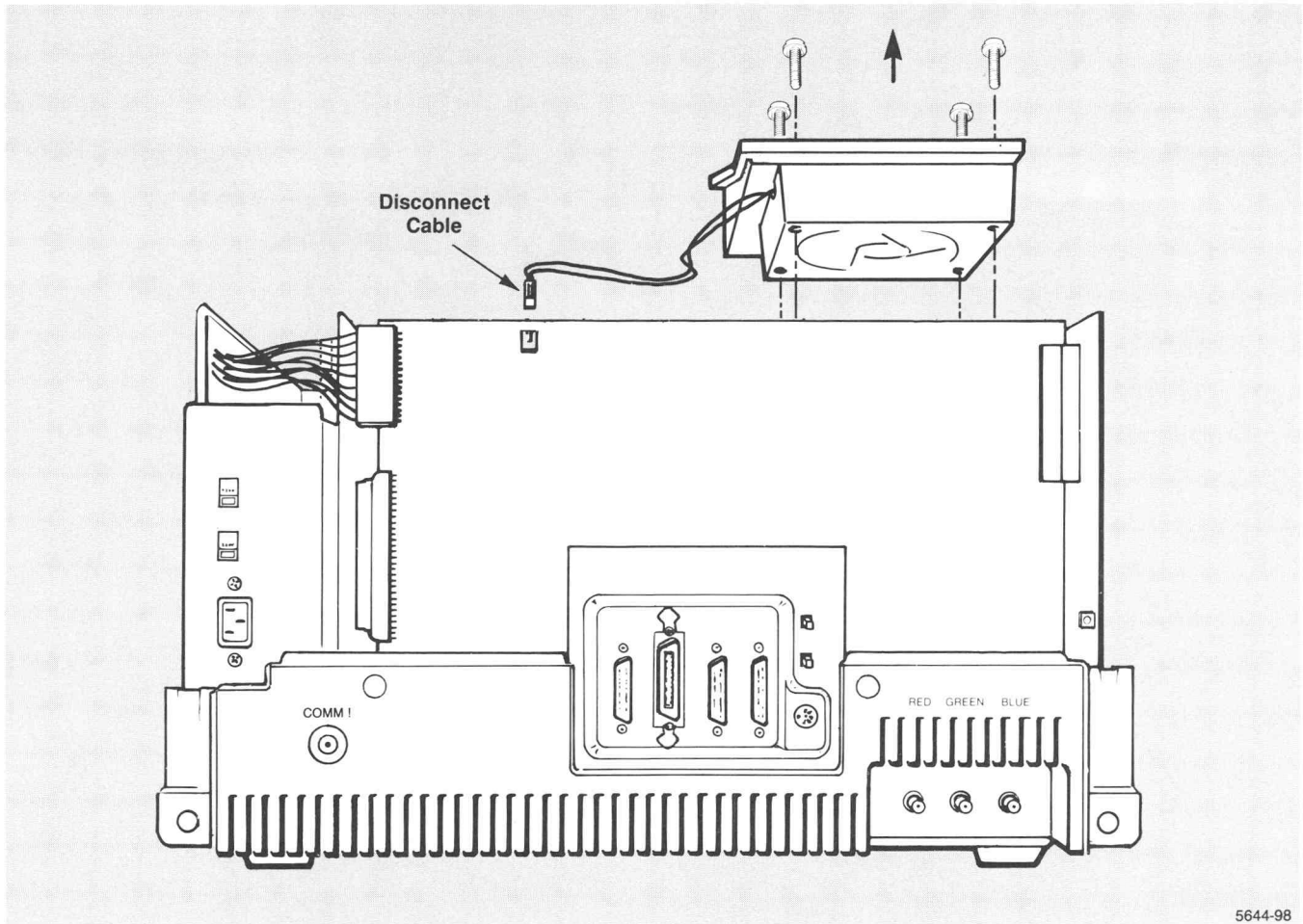
Figure 6-17. Mounting Screws for the Bottom of the Display Module.

OPENING THE 119-2387-00 DISPLAY MODULE FOR CALIBRATION

To provide access to adjustments during Display Module calibration, remove the fan assembly, and the Display Module's top and rear panels.

Fan Assembly

Remove the four screws that secure the fan assembly. Refer to Figure 6-18 for locations.



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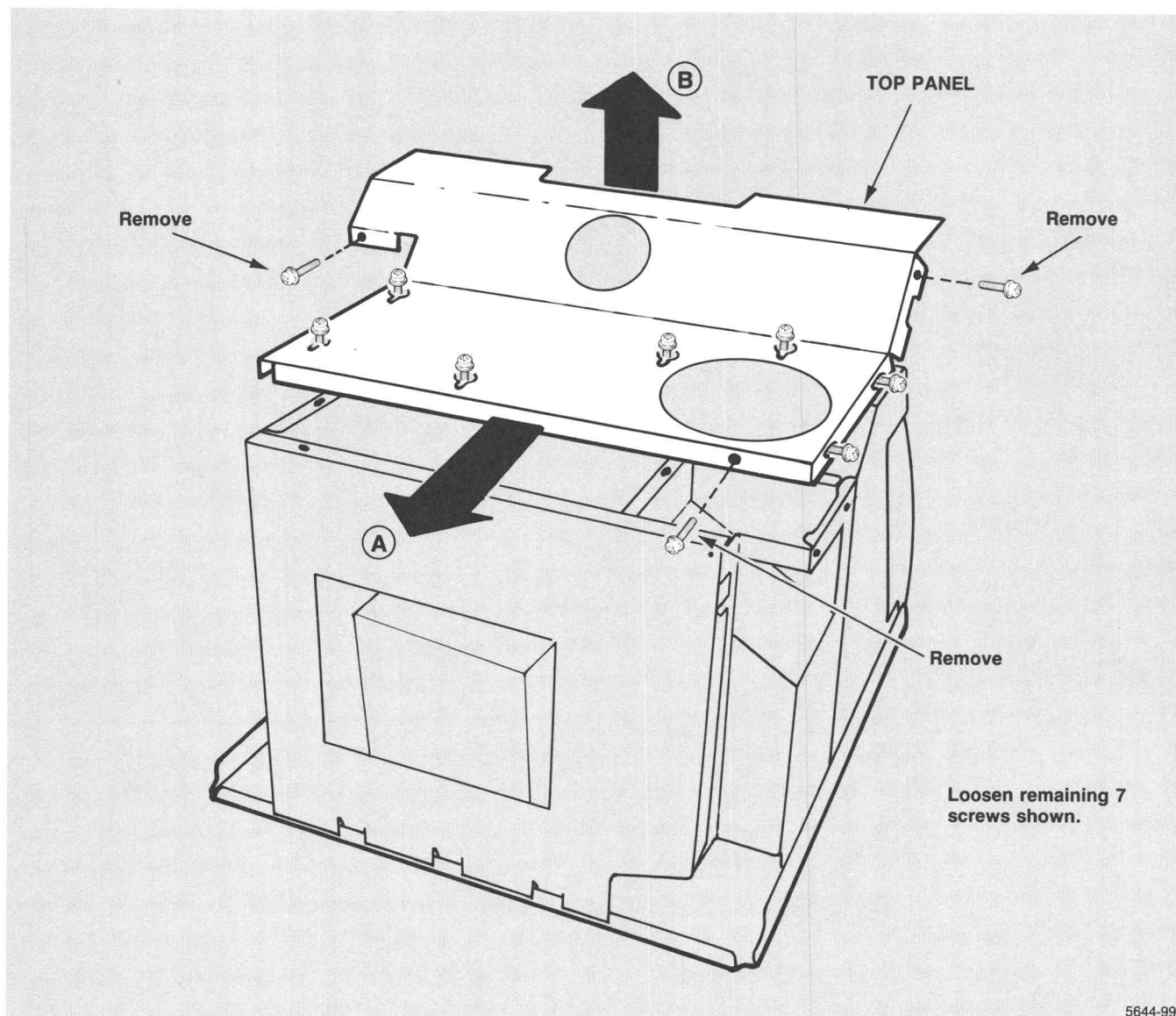
Figure 6-18. Removal of Fan Assembly (119-2387-00).

Display Module Top Panel

Refer to Figure 6-19 during top panel removal.

1. Loosen the seven indicated screws (five on top and two on the side of the fan duct).

2. Remove the three indicated screws on the sides of the top panel.
3. Slide the top panel toward the rear of the Display Module while gently lifting on the panel. Remove the top panel once the loosened screws are centered in the larger holes.



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Figure 6-19. Removal of Display Module Top Panel (119-2387-00).

Display Module Rear Panel

Refer to Figure 6-20 during rear panel removal.

1. Remove the two indicated screws on the rear and side of the panel.
2. To remove the rear panel, tilt the panel back slightly while gently lifting.

CAUTION

During reassembly, take care not to pinch cables at the bottom of the Display Module.

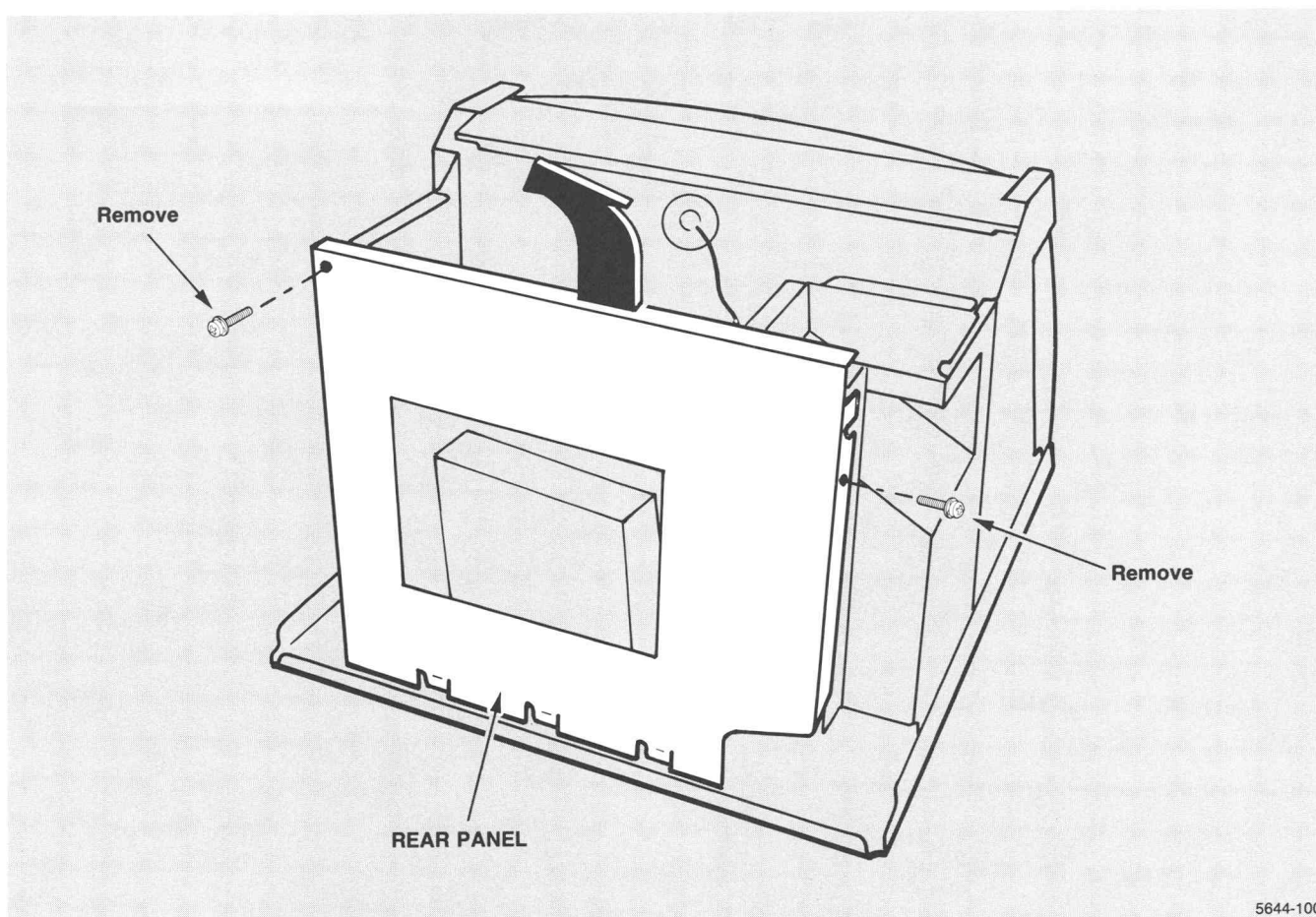


Figure 6-20. Removal of Display Module Rear Panel (119-2387-00).

REPLACEABLE ASSEMBLIES OF THE 119-2387-00 DISPLAY MODULE

For access to the Display Module, first remove the fan assembly. Then remove the previously described terminal logic boards (Terminal Control, Display Control, and RAM Option boards). Finally remove the Display Module's top and rear panels as previously described for the 119-2387-00 Display Module.

Easily accessible boards are the Video board, the Degauss Control board, the Display Low Voltage Power Supply (DLVPS) module, and the AC Distribution board. The Deflection/HV board, on the other hand, is not so easily accessible. In service center environments, remove the crt to most easily access the Deflection/HV board. In office environments (where crt removal could be hazardous to personnel), access the Deflection/HV board by removing both the DLVPS and the sheet metal side it is attached to.

Display Low Voltage Power Supply (DLVPS)

Refer to Figure 6-21 on the next page to remove the DLVPS module. The following procedure requires prior removal of the Terminal Control and Display Control boards.

1. Remove the four screws that secure the fan plenum. Then lift the plenum out of the Display Module.
2. Remove the two indicated screws on the side of the chassis and the screw at the base of the DLVPS module.
3. Remove the five cable connectors to the DLVPS module (CN1, CN2, CN3, CN4, and the unlabeled connector next to CN4).
4. Free the cables attached to the DLVPS module by untwisting the two plastic cable ties.

CAUTION

During DLVPS module removal, take care to not scratch the crt or damage capacitors on the Degauss Control board.

5. During removal, lift the DLVPS module and tilt so the metal lip on the bottom clears the Display Module chassis.

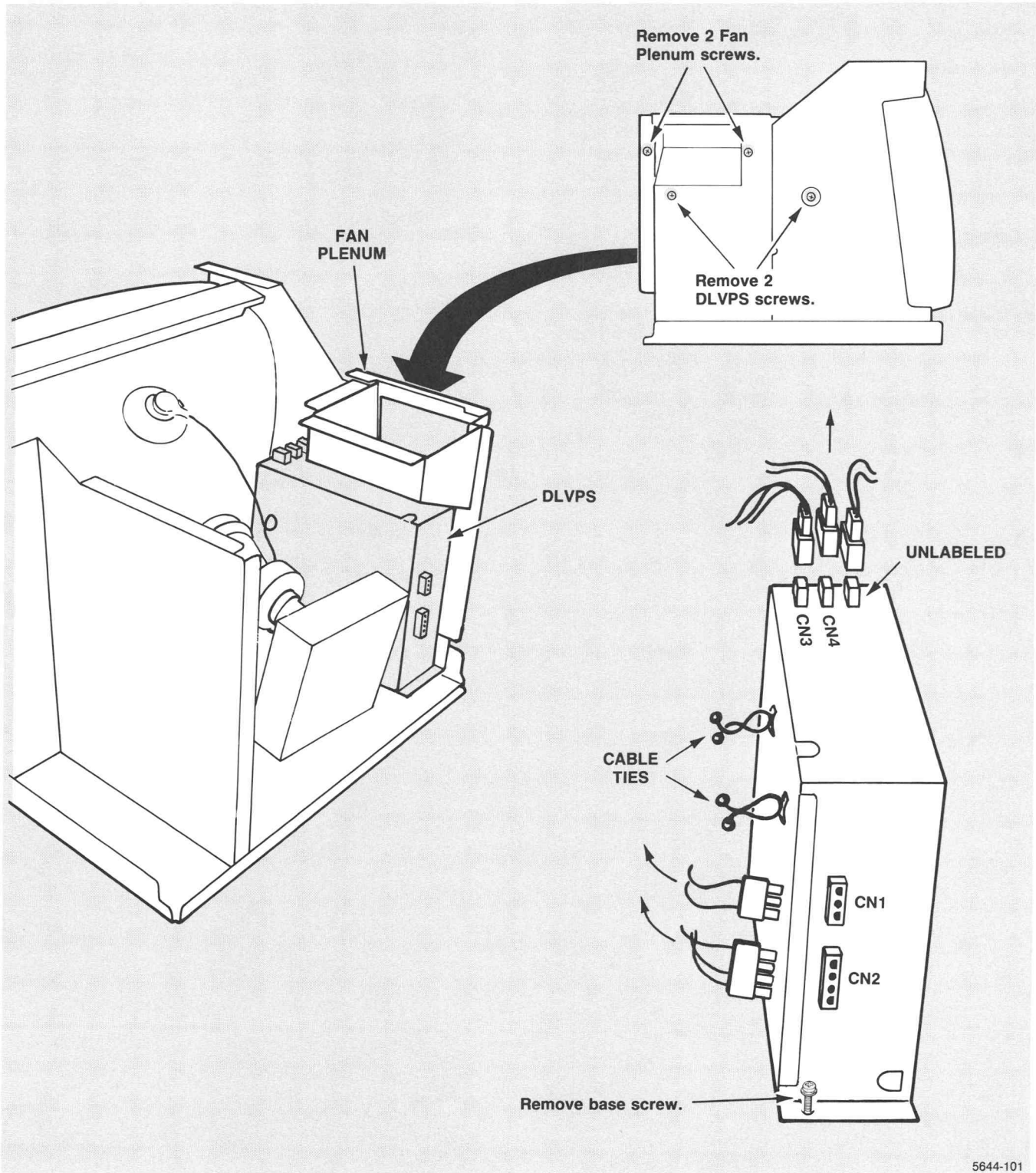


Figure 6-21. Removal of DLVPS Module (119-2387-00).

AC Distribution Board

Perform the following procedure to remove the AC Distribution board:

1. Remove the TLVPS module from the side of the Display Module.
2. Disconnect the three connectors from the AC Distribution board (CN6, CN1, and CN2).
3. With longnose pliers, squeeze the plastic securing tabs to release the AC Distribution board.

Disconnecting the CRT Socket Board

The Socket board mounts to the rear plug on the crt (see Figure 6-22). During the following procedure, the Socket board is only disconnected from the crt; it remains connected to the Deflection/HV board. For Socket board removal, refer to the removal procedure for the Deflection/HV board.

WARNING

The crt socket is quite vulnerable to damage. Use caution when working around it.

1. If silicon adhesive was used to secure the board to the crt, carefully peel it off with a knife.
2. Then gently pry the Socket board off the crt pins. Lay the board down on the Deflection/HV board.

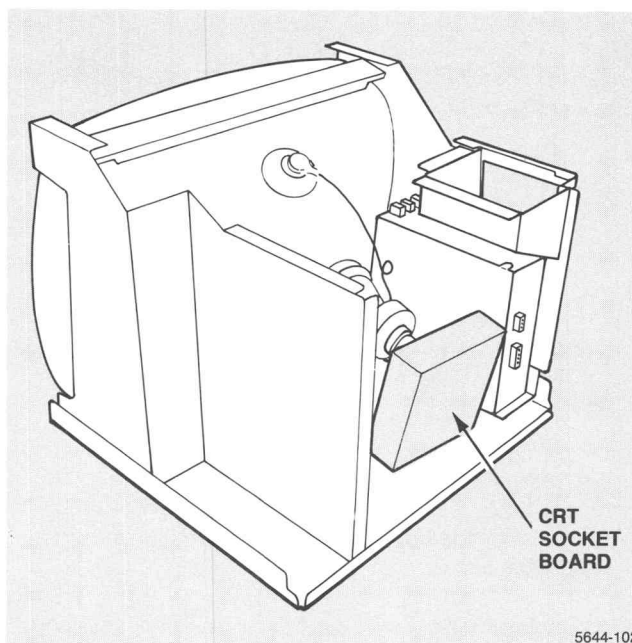


Figure 6-22. CRT Socket Board (119-2387-00).

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Front Bezel

Refer back to Figure 6-14 to remove the front bezel from the Display Module.

CRT Removal

This procedure assumes prior removal of the front bezel. The deflection coil remains on the crt during removal. Refer to Figure 6-23 during the following procedure:

WARNING

Lethal voltages are present at the High Voltage anode on the crt. Discharge this HV connection before performing the following procedure. Bodily contact with high voltages may cause shock, injury, or death.

1. (A) Discharge the High Voltage anode button on the crt several times; see preceding WARNING. Then remove the High Voltage anode cable from its connector button at the front of the crt.
2. (B) Unplug the Socket board from the crt (if not already removed). A silicon adhesive may have been used to secure the Socket board to the crt; if so, carefully use a knife to slice the gum away from the Socket board.
3. (C) Place a soft pad on the bench-top and in front of the crt. (When removed, the crt's face will rest on this protective pad.)

WARNING

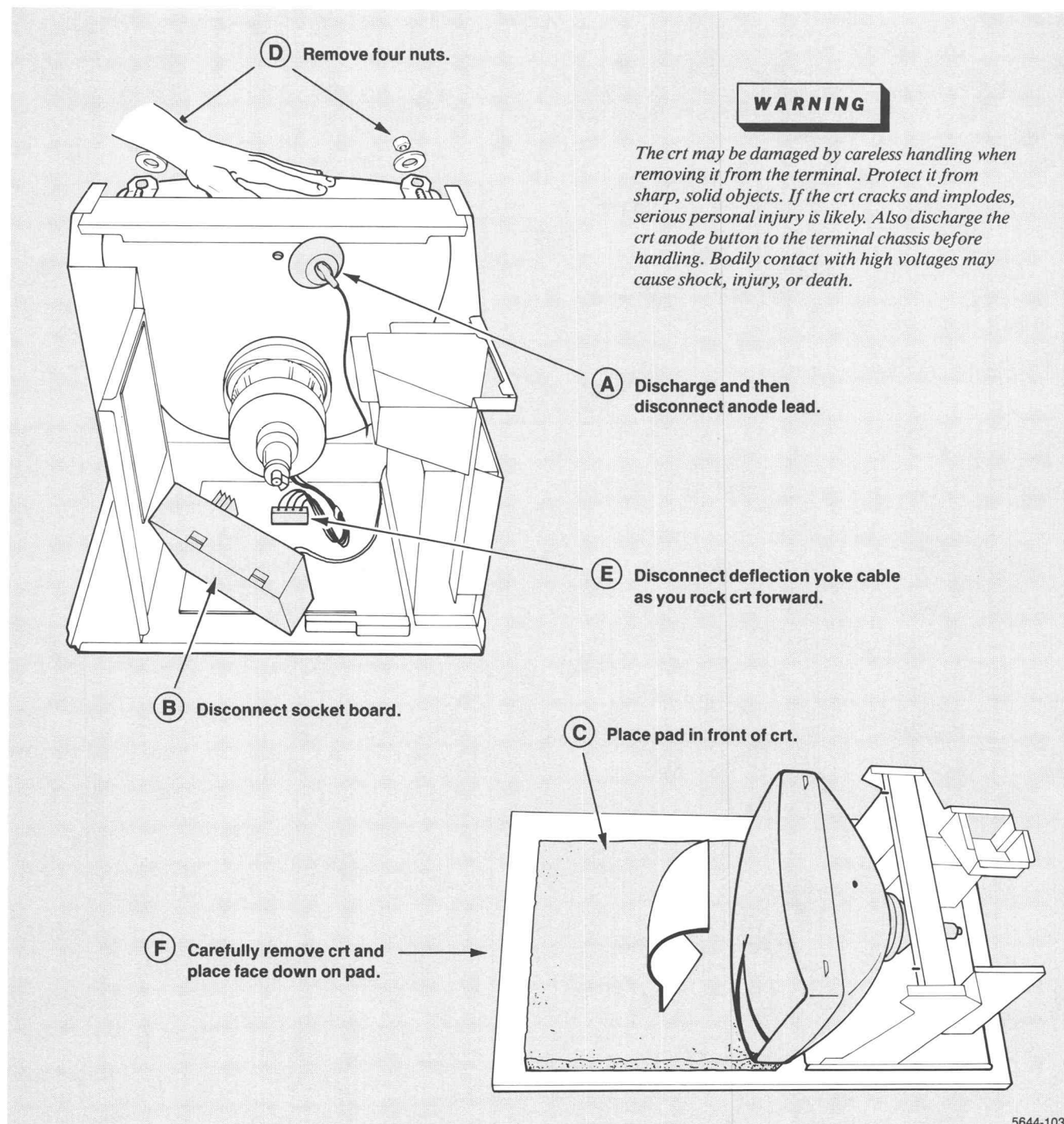
The crt may be damaged by careless handling when removing it from the terminal. Protect it from sharp, solid objects. If the crt cracks and implodes, serious personal injury is likely. It is also wise to discharge the crt anode button to the outside DAG coating just before handling.

4. (D) Using a 5/16 nut driver, remove the four bolts, four large metal washers, twelve small metal washers, and four rubber washers that clamp the front corners of the crt to the Display Module chassis. (For later installation observe the order in which the hardware comes off.) Place the nuts and washers in a labeled container to prevent misplacing them or confusing them with other hardware.
5. (E) Rock the crt forward as shown. Unplug the deflection yoke cable from the Deflection/HV board and disconnect the ground strap.
6. (F) Then pull the crt out of the front of the Display Module, and lower it onto the protective pad.

To reinstall the crt, follow the previous steps in reverse order.

WARNING

Before handling any crt (new or old), always discharge the crt anode button to the outside DAG coating. A long-term charge effect may leave enough energy at the anode slip-on connection to cause a dangerous shock even though the tube was recently discharged.



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Figure 6-23. Removing the CRT for the 119-2387-00 Display Module.

Video Board

Removal of the Video board requires the following prior disassembly; remove the fan assembly, Terminal Control board, Display Control board, and the Display Module's top and rear panels. Refer to Figure 6-24 for the following procedure:

1. Disconnect the three BNC connectors (RGB outputs) from the Display Control board.
2. Disconnect the three phone-jack connectors from their associated BNC connectors (RED, GREEN and BLUE) at the rear of the terminal.
3. Unwrap the five cable restraints to free the video cables.
4. Disconnect the Blue (2), Red (0), Green (1), and Sync (S) phone-jack connectors on the Video board.
5. Disconnect the A3, A7, A8, and C8 cable connectors from the Video board.
6. Remove the CN4 connector at the top of the DLVPS module.
7. Unwrap all required cable restraints near the Deflection/HV board.
8. With longnose pliers, squeeze the plastic securing tabs to release the Video board.
9. Unwrap any beaded cable ties to free the Video board.

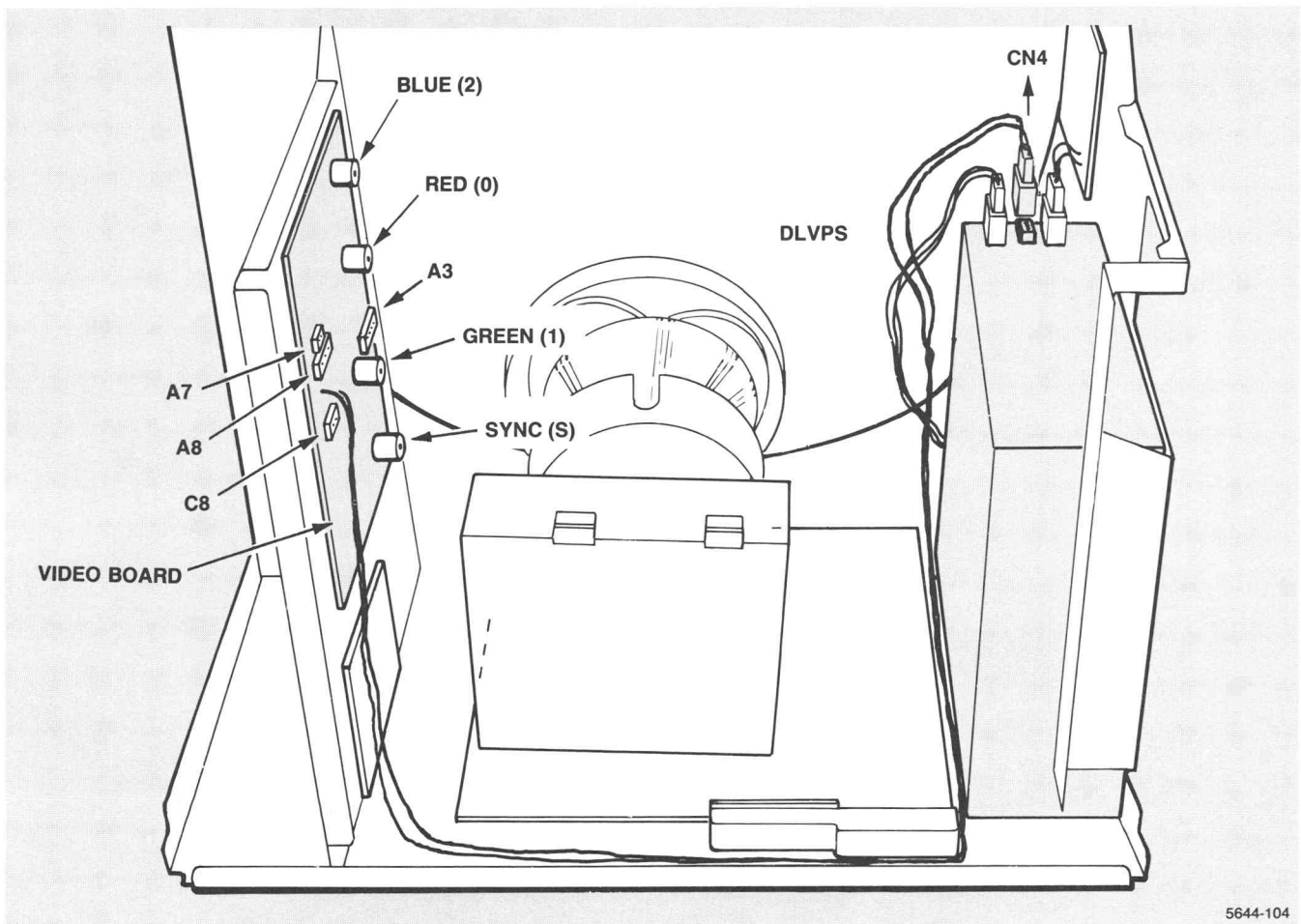


Figure 6-24. Removing the Video Board (119-2387-00).

Deflection/HV Board

Removal of the Deflection/HV board requires the following prior disassembly; remove the fan assembly, Terminal Control board, Display Control board, Display Module's top and rear panels, disconnect the Socket board, and remove the DLVPS with the attached sheet metal side of the Display Module. Refer to Figure 6-25 for the following procedure:

NOTE

The Deflection/HV board and the Socket board are removed as one assembly during this procedure. Both boards are connected together by common wires soldered to each board.

1. Discharge the crt anode to ground. Then disconnect the anode lead from the crt.
2. Disconnect the Blue (2), Red (0), Green (1), and Sync (S) phone-jack connectors from the Video board.
3. Disconnect the A3, A8, and C8 cable connectors from the Video board.
4. Unplug the two ground connectors from the Socket board and the ground connector from the Deflection/HV board.
5. Remove the B connector and the deflection yoke cable from the Deflection/HV board.
6. Unwrap any cable restraints around the edge of the Deflection/HV board.
7. Remove the indicated screws holding the Deflection/HV board to the chassis.
8. Remove the ground straps.
9. Slide the Deflection/HV board to clear the circuit board guides. Then lift the board and attached Socket board out of the Display Module.

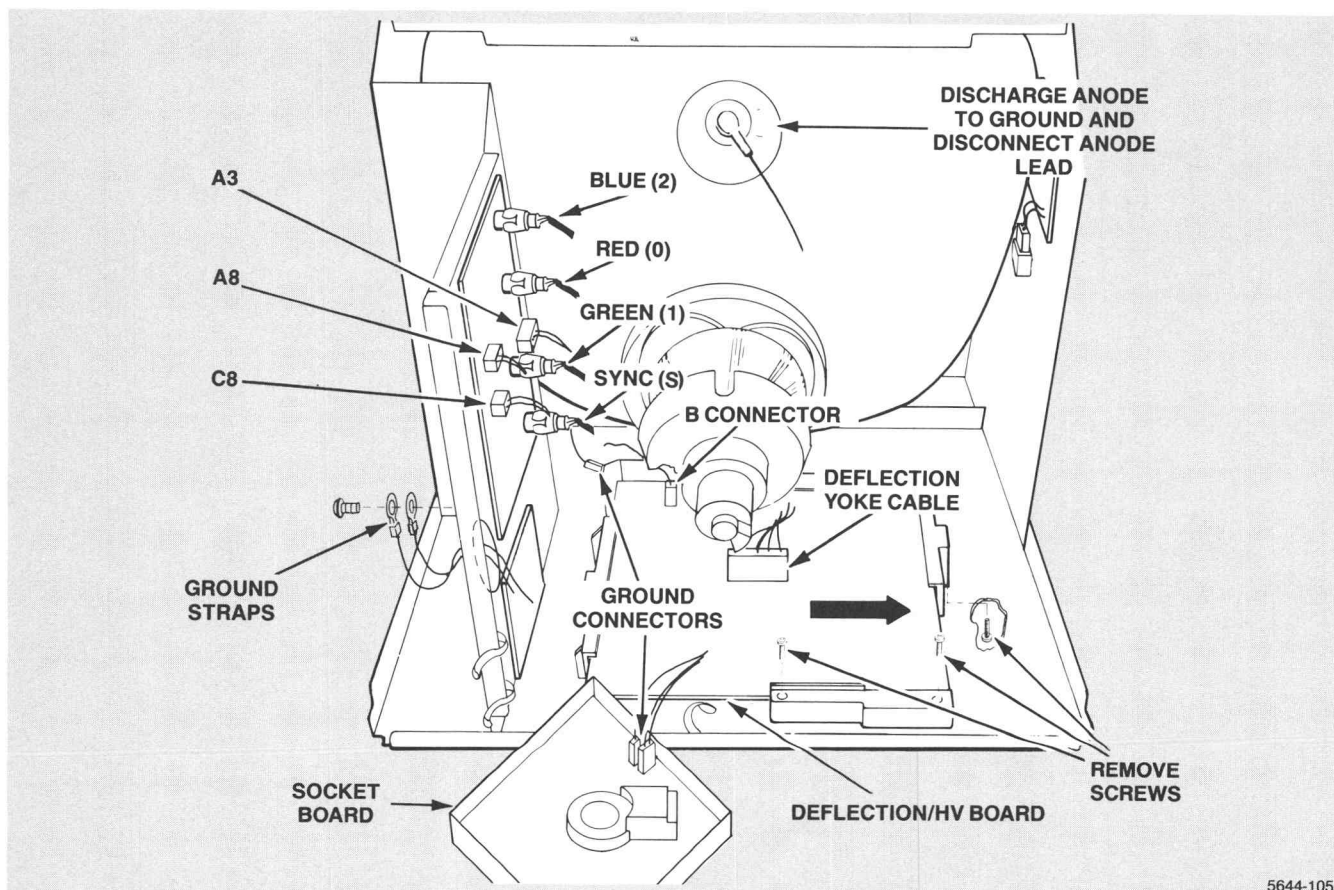


Figure 6-25. Removing the Deflection/HV Board (119-2387-00).

Degauss Control Board

Removal of the Degauss Control board requires the following prior disassembly; remove the fan assembly, Terminal Control board, Display Control board, and Display Module's top and rear panels. Refer to Figure 6-26 for the following procedure:

1. Disconnect CN7 from the TLVPS module.
2. Remove the CN6 connector from the AC Distribution board.
3. Unwrap any cable restraints near the Deflection/HV board to release wires for the previously removed connectors.
4. Disconnect the degauss coil connector from the Degauss Control board (during installation, plug polarity does not matter for this connector).
5. Disconnect the CN5 connector from the top of the DLVPS module.
6. With longnose pliers, squeeze the plastic securing tabs to release the Degauss Control board.

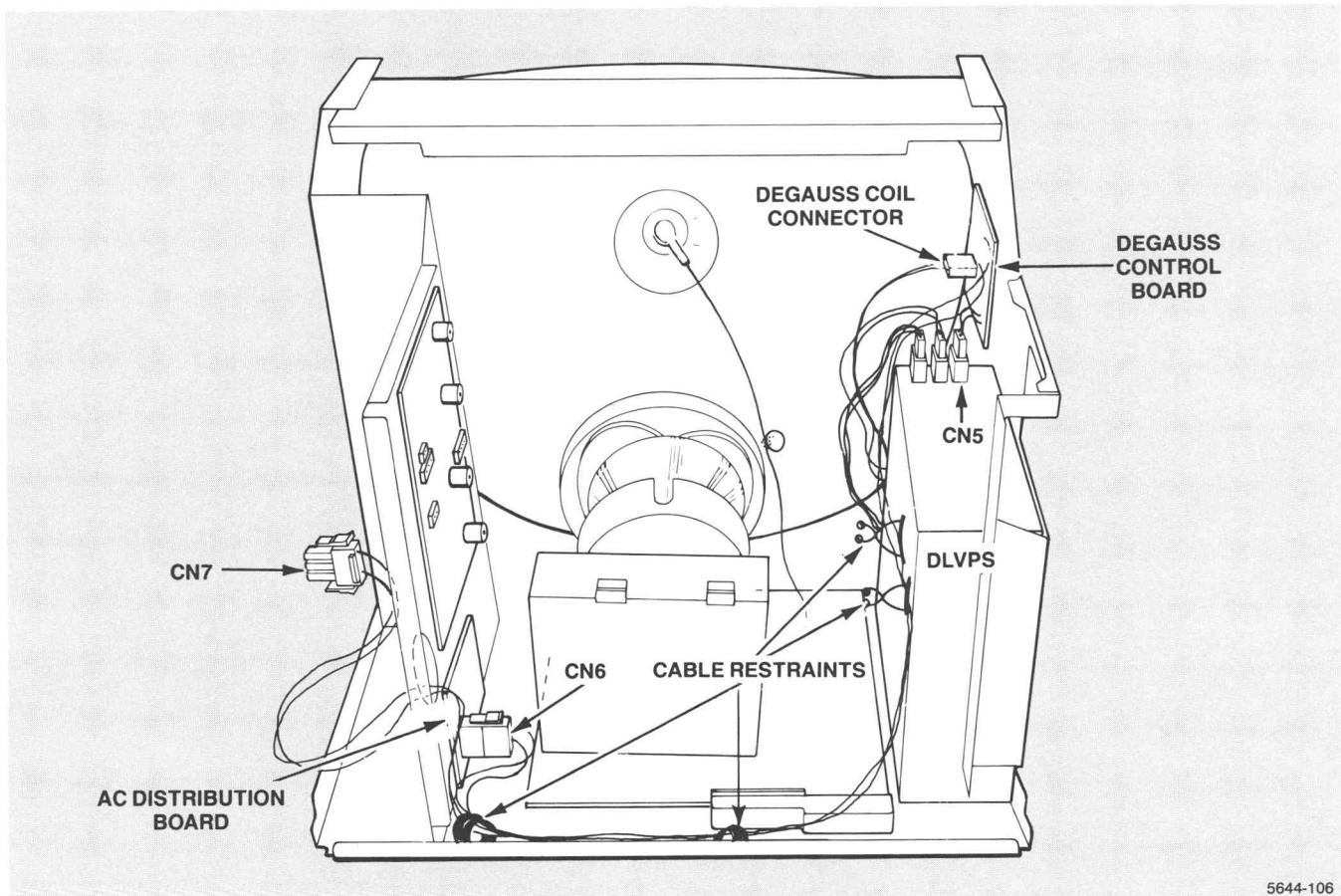


Figure 6-26. Removing the Degauss Control Board (119-2387-00).

KEYBOARDS

The Keyboard Module is physically separate from the main terminal. It is only connected by a five-conductor cord. There are three possible keyboards; the standard keyboard with thumbwheels for the 4111, the optional keyboard with Joydisk for the 4111, and the IBM 3279-style keyboard for the CX4111.

You may separate the keyboard from all other assemblies by unplugging the keyboard connector from the terminal, and by unplugging the mouse connector (if installed) from the keyboard.

Keyboard with Thumbwheels

1. Refer to Figure 6-27. To open, turn the keyboard over on a soft pad and remove the attaching six screws located in the bottom cover panel.
2. Then flip the elevating bails outward, as shown in Figure 6-27.
3. Remove the bottom cover panel, by lifting it off the keyboard assembly.

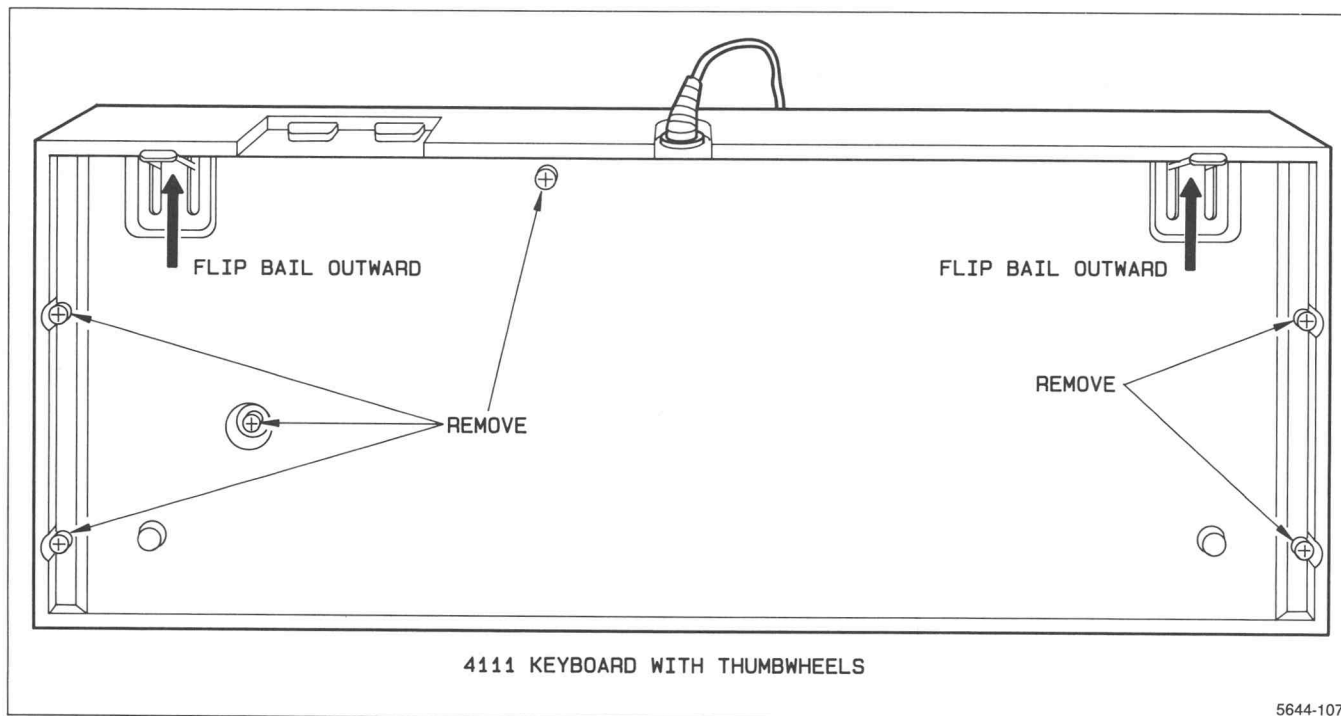


Figure 6-27. Keyboard Cover Screws and Bail Position.

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4. To separate the keyboard cable from the circuit board, unplug the cable's five-pin connector. Then remove the two ground connectors (one to the circuit board, and one to the panel for the Joystick/Mouse connectors). See Figure 6-28.
5. To remove the circuit board, unplug the Mouse (J3) and Joystick (J2) connectors from the circuit board. Also disconnect the vertical and horizontal thumbwheel connectors as shown in Figure 6-28.

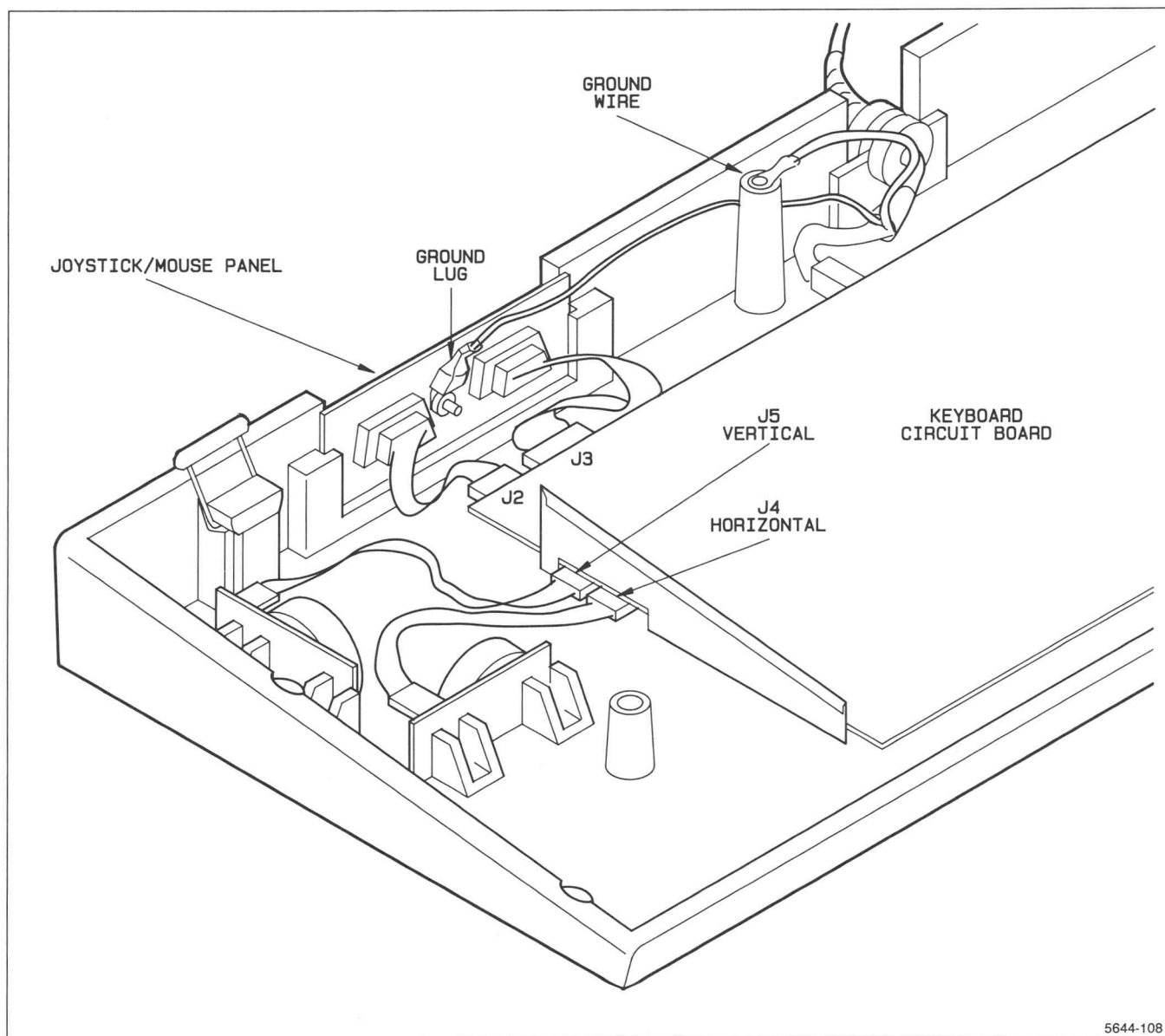
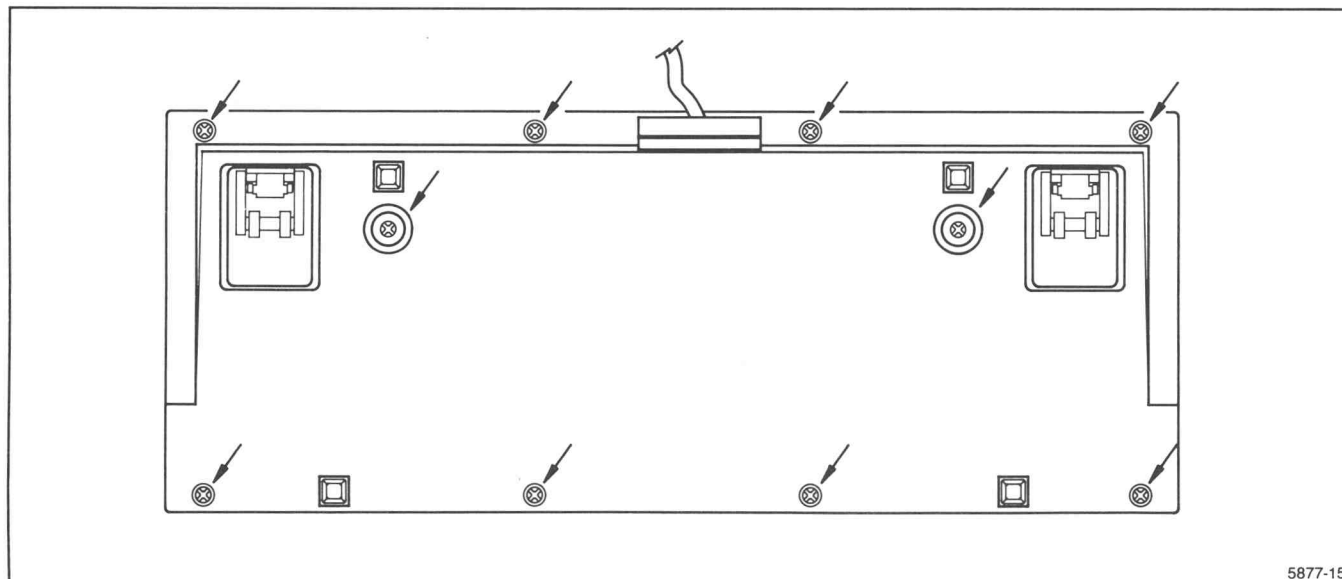


Figure 6-28. Removing the Keyboard Connectors.

4. To reassemble the keyboard, follow the disassembly steps in reverse order. Remember to flip the elevating bails outward and to position the ground lug over the middle post as shown in Figure 6-28. Also check that the "TO JOYSTICK" and "TO MOUSE" labels are visible.

Keyboards with Joydisk

1. To open, turn the keyboard over and remove the attaching screws (ten), located in the bottom cover panel. See Figure 6-29 for screw locations.



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Figure 6-29. Keyboard Cover Screws.

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2. Refer to Figure 6-30. Remove the bottom cover panel, by lifting it off the keyboard assembly. Then lift the circuit board/keypad assembly out of the top cover panel and set the top cover panel aside.
3. To separate the keyboard cable from the circuit board, unplug its six-pin cable connector and remove the cable-tie restraints. Use wire cutters to cut the cable-ties as shown in Figure 6-31.
4. To reassemble the keyboard, follow the disassembly steps in reverse order. Add new cable-tie restraints when reattaching the keyboard cable.

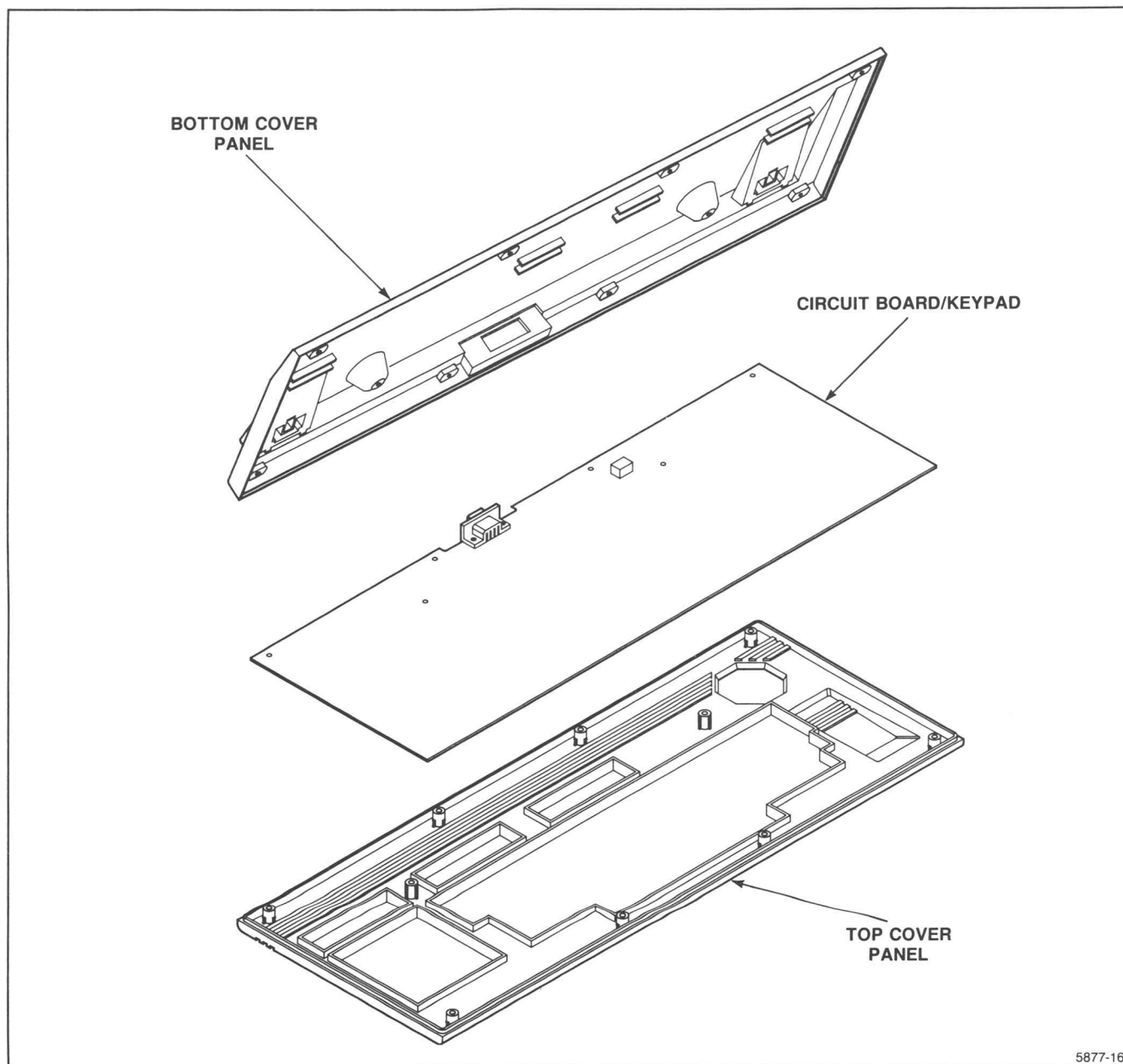


Figure 6-30. Removing the Keyboard Covers.

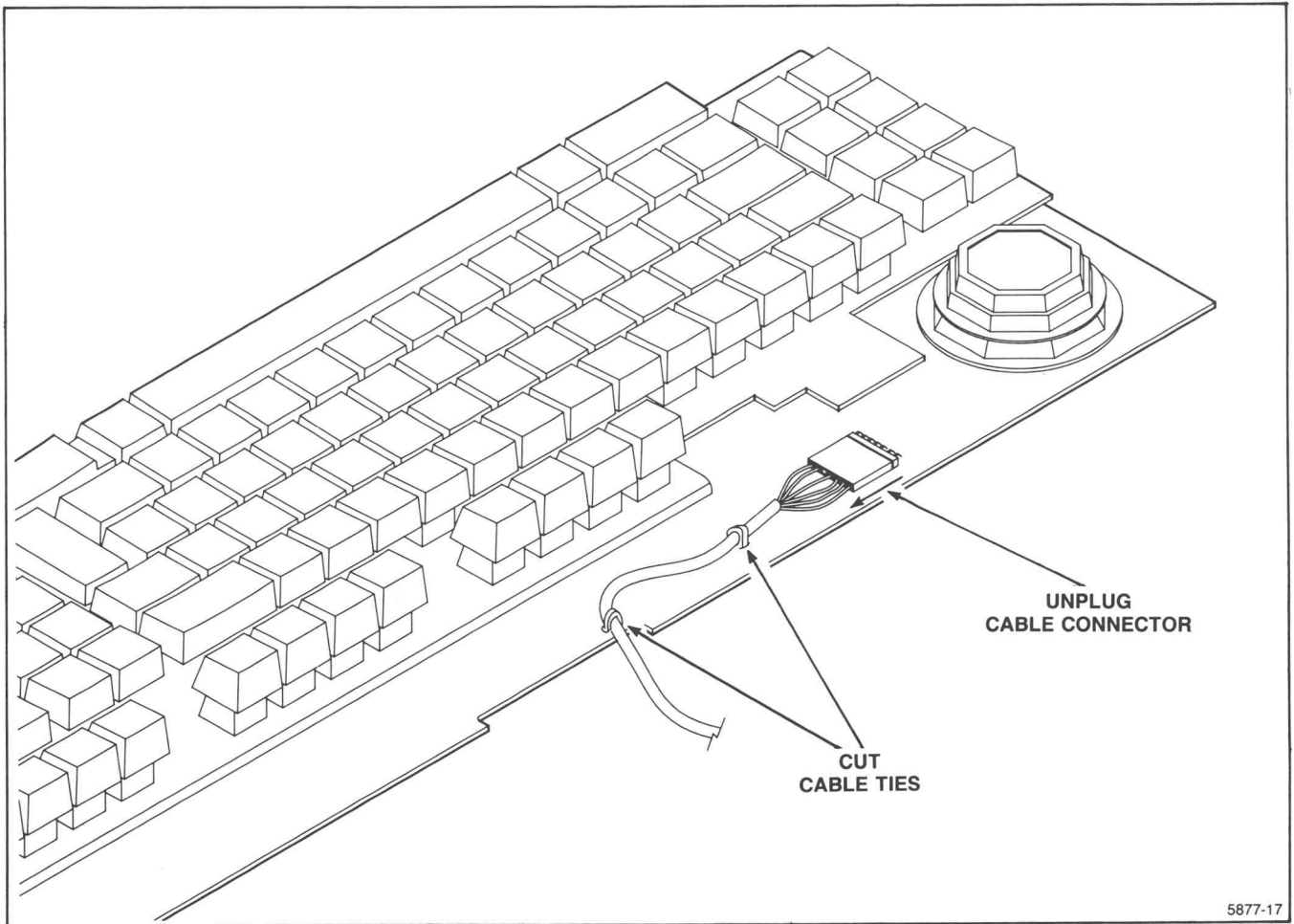


Figure 6-31. Removing the Keyboard Cable.

TROUBLESHOOTING AND CORRECTIVE MAINTENANCE

Fault isolation for the terminal is best handled in the following manner. Carefully observe all symptoms of the problem and list them. Check the main user functions (Section 3) and note any problems. Then run Self-test and record the error message(s) displayed on the screen. (If the Display Module doesn't work, a crude message appears on the LEDs inside the back of the terminal.) After discovering which module is malfunctioning, remove, repair or replace.

SELF-TEST DIAGNOSTIC ROUTINE

Section 3 contains a description of the Self-test diagnostic program. The last part of Section 6 provides a list with explanations of all error messages. This program is designed such that the operator may run Self-test and report the findings to the local service center. This facilitates trouble shooting by narrowing the problem before the technician arrives.

The primary error reporting device is the display screen; all error messages are sent to the screen. If the display is faulty, no messages will appear while Self-test is running, but the bell will ring and LEDs may flash (if you have the standard 4111 Keyboard with thumbwheels).

INITIAL/VISUAL CHECKS

Aside from Self-test, certain simple visual tests may help isolate a problem to the functional block level. The following basic suggestions help when trouble shooting the terminal.

Display Module Problems

The Display Module uses three-color, raster-scan technology, and is much like the display section of most color television receivers. Display problems may be grouped as follows:

- Blank screen — can mean:
 - Burned out filament in crt, or
 - Loss of 25KV high voltage to crt, or
 - Loss of low voltage to accelerating anodes of crt (from LV power supply module). If high voltage is low, check multiplier circuits.
- Low contrast — Check video amplifier stages and condition of crt.
- Dot of light — Check the horizontal and vertical deflection circuits.
- Only a horizontal line — Check the vertical deflection circuitry.
- Vertical line only (no deflection) — Check horizontal deflection circuits.
- Raster on screen but no information — Check the data path through the video amplifier sections.
- No color (only black and white) — Check the programming of the Color Map. (If white is pure, this means all three color guns are operational.)
- Check the voltages to the Video Board (in the GMA302 Display Module, these are: +5V, +9V, +11V, -11V, +15V, -15V, +19V, -19V, +25V, +75V, and +160V).

These are customary checks when troubleshooting a color raster display.

COMPONENT LEVEL REPAIR PROCEDURES

The use of Self-test and visual checks should provide fault isolation to the board/module level. Normally the defective board/module is sent to a regional service center where component level repairs are performed with ease. If on-site component repairs are necessary, follow these helps.

- Check the power inputs to various chips on the board to verify that +5V, +12V, and all other supply voltages are reaching all parts of the board. (First, verify that the power supply works).
- Examine the board for obvious signs of excessive heat (especially on analog or discrete circuitry, such as the Display Module boards and power supply board).
- If the bell fails, examine/replace the small round transducer, located inside the keyboard.
- Replace the crt if one gun fails.

NOTE

Certain components, such as High-Voltage supplies or high-efficiency circuits, may produce excessive and harmful radiation if replaced by non-Tektronix parts. Part numbers for these components are identified in the electrical parts list (Section 8).

SELF-TEST ERROR MESSAGES

INTRODUCTION

The 4111 Self-test system is a sequence of tests in two main modules: the Terminal Control board module and the Display Control board module. If you have a CX4111, tests are also made on the CX Interface board module.

When a Self-test error occurs, the keyboard bell will ring twice if a non-fatal error occurs or three times if a fatal error occurs. An English-language message (with several codes for additional information) will be printed on the terminal screen. The error message has the following format:

“‘Test Name’ Failure [XX.YY.ZZ]”

Where ‘Test Name’ identifies the test, XX is the hexadecimal test code, YY is the subtest number, and ZZ is the submessage code.

In addition to the screen message, LEDs on the circuit boards assist in identification of failures.

TERMINAL CONTROL BOARD TEST MODULE ERROR MESSAGES

“Keyboard Interface Failure [FC.xx.yy]”

Explanation. The keyboard and LED test has failed. The hexadecimal error code is FC, xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the keyboard, the keyboard LEDs, and the interface from the keyboard to the Terminal Control board (the Keyboard Controller — U482). An error in this test is non-fatal, and the test is performed during Extended Self-test and Cycle testing only.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 Keyboard Interface Loopback Test
 - 01 Status bits were incorrect at the transmission of the first character
 - 02 Status bits were incorrect at the transmission of the second character
 - 04 Status bits were incorrect at the transmission of the third or fourth character
 - 08 Status bits were incorrect when receiving a character
 - 10 Failed to receive correct first character (00)
 - 20 Failed to receive correct second character (0FF)
 - 40 Failed to receive correct third character (55)
 - 80 Failed to receive correct fourth character (0AA)
- 02 Keyboard ID Check

“Processor System Failure [EF.xx.yy]”

Explanation. The 80186 timer test has failed. The hexadecimal error code is EF, xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the 80186 timer on the Terminal Control board (U410). An error in this test is non-fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 80186 timer and registers failed static test
- 02 80186 timer failed dynamic test
 - 00 Timer 0, count too short
 - 01 Timer 0, count too long
 - 02 Timer 1, count too short
 - 03 Timer 1, count too long
 - 04 Timer 2, count too short
 - 05 Timer 2, count too long

“ROM Failure [EC.xx.yy]”

Explanation. The system ROM check has failed. The hexadecimal error code is EC, xx is submessage 1, and yy is submessage 2. The board failure LED is on the Terminal Control Board.

Description. This test checks the system EPROMs on the Terminal Control board (U130, U330, U140, U340, U142, U342, U150, U350, U152, U352, U162, U362). An error in this test is fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

Submessage 1

- 0 aaaa Top nibble of failed ROM pair address (example: if ROM pair at E8000 failed, aaaa would be 0E)

Submessage 2

- 11 High ROM not present
- 21 High ROM checksum error
- 31 High ROM position incorrect
- 12 Low ROM not present
- 22 Low ROM checksum error
- 32 Low ROM position incorrect
- 13 Both ROMs not present
- 23 Checksum error in both ROMs
- 33 ROM position incorrect, both ROMs

“Processor System Failure [EB.xx.yy]”

Explanation. The interrupt test has failed. The hexadecimal error code is EB, xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the interrupt logic on the Terminal Control board. An error in this test is non-fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 Interrupt Register test (the registers are internal to the Processor IC — U410)
 - 01 Int3 Control Register failed
 - 02 Int2 Control Register failed
 - 03 Int1 Control Register failed
 - 04 Int0 Control Register failed
 - 05 DMA1 Control Register failed
 - 06 DMA0 Control Register failed
 - 07 Timer Control Register failed
 - 08 Interrupt Status Register failed
 - 09 Interrupt Request Register failed
 - 0A Interrupt Service Register failed
 - 0B Priority Mask Register failed
- 02 Dynamic Interrupt test
 - 01 INT0 failed
 - 02 INT1 failed
 - 03 INT2 failed
 - 04 INT3 failed
 - 05 NMI failed (bus timeout)
 - 06 DMA request 0 failed
 - 07 DMA request 1 failed
- 03 Divide-by-zero Interrupt test

“Processor System Failure [DF or DE.aa.ll.hh]”

Explanation. The Processor Bus test has failed. The hexadecimal error code is DF (low bits) or DE (high bits); aa, ll, and hh are defined in the submessages. The board failure LED is on the Terminal Control Board.

Description. This test checks the Processor bus on the Terminal Control board. An error in this test is fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 Bus test
 - aa Base address of failure
 - ll Bit in error in low data byte
 - hh Bit in error in high data byte

“Host Port Failure [DD, DC, or DB.xx.yy]”

Explanation. The Host RS-232 I/O Port Baud Rate Loopback Character check has failed. The hexadecimal error code is DD (I/O Port check), DC (Baud Rate/Loopback check), or DB (Status Line check); xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the host RS-232 port on the Terminal Control board. An error in this test is non-fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing. (The Control/Status Line Check, subtest 03, is performed in Adjustment Self-test only.)

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 Host Port Xmit/Receive check (U462)
 - 01 Status bits failed on transmission of first character
 - 02 Status bits failed on transmission of second character
 - 04 Status bits failed on transmission of third or fourth character
 - 08 Status bits failed on character reception
 - 10 Failed to receive correct first character (00)
 - 20 Failed to receive correct second character (0FF)
 - 40 Failed to receive correct third character (55)
 - 80 Failed to receive correct fourth character (0AA)
- 02 Baud Rate check
 - 01 19200 baud failed
 - 02 9600 baud failed
 - 04 4800 baud failed
 - 08 2400 baud failed
 - 10 1200 baud failed
 - 20 600 baud failed
 - 40 300 baud failed
 - 80 150 baud failed
- 03 Control/Status Line check
 - 01 CTS not high or delta CTS not set
 - 02 CTS not low or delta CTS not set
 - 04 DSR not high or delta DSR not set
 - 08 DSR not low or delta DSR not set
 - 10 DCD not high or delta DCD not set
 - 20 SDCCD not high or delta SCDC not set
 - 40 DCD not low or delta DCD not set
 - 80 SDCCD not low or delta SDCCD not set

“RS-422 Failure [DA.xx.yy]”

Explanation. The Host RS-422 I/O Port Baud Rate Loopback Character check has failed. The hexadecimal error code is DA, xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the host RS-422 port on the Terminal Control board. An error in this test is non-fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 DMA Transfer check
 - 01 SCC failed to sync
 - 02 Receiver failed to start
 - 04 Transmitter failed to start
 - 08 Receiver started but failed to finish
 - 10 Transmitter started but failed to finish
 - 20 DMA transfer finished but data incorrect

“RAM System Failure [aa.xx.pp.yy.zz]”

Explanation. The System RAM check has failed. Refer to the error code (aa) descriptions for an explanation of the coded portion of the message. The board failure LED is on the Terminal Control Board.

Description. This test checks the system RAM memory. An error in this test is fatal if an error occurs in low RAM, but is non-fatal if the error occurs in high RAM. Refer to the subtest descriptions for information regarding when the test is performed.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

- B4 Optional RAM Register check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
xx gives the Status Register bits in error
- B9 Low Walking Ones test
This test is performed during Extended Self-test and Cycle testing only.
xx is the address of the RAM error (xx000)
pp is the RAM page (when xx > 40)
yy is the low data byte bits in error
zz is the high data byte bits in error
- B3 High Walking Ones test
This test is performed during Extended Self-test and Cycle testing only.
Refer to "Low Walking Ones test" for error codes.
- B8 Low Walking Zeros test
This test is performed during Extended Self-test and Cycle testing only.
Refer to "Low Walking Ones test" for error codes.
- B8 High Walking Zeros test
This test is performed during Extended Self-test and Cycle testing only.
Refer to "Low Walking Ones test" for error codes.
- B7 Low All Ones check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
Refer to "Low Walking Ones test" for error codes.
- B7 High All Ones check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
Refer to "Low Walking Ones test" for error codes.
- B6 Low Init RAM check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
Refer to "Low Walking Ones test" for error codes.
- B6 High Init RAM check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
Refer to "Low Walking Ones test" for error codes.

- BB Refresh check
This test is performed during Extended Self-test and Cycle testing only.
Refer to "Walking Ones test" for error codes.
- BA RAM/ROM Memory Map
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
xx is the address of the RAM/ROM error (xx000)
 - 0 Memory timeout problem
 - 1 Problem in high RAM/ROM of pair
 - 2 Problem in low RAM/ROM of pair
 - 3 Problem in both RAMs/ROMs in pair
- B5 RAM Stack Building
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
No further submessages
- B4 Operating System Vector Table check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
No further submessages

"Defaults Reset - Nonvolatile Parameter Failure [AF.xx]"

Explanation. The EEROM Memory check has failed. The hexadecimal error code is AF and xx is the subtest. The board failure LED is on the Terminal Control Board.

Description. This test checks the EEROM on the Terminal Control board. An error in this test is non-fatal, and the test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest Codes. The following codes identify the circuitry in which the error occurred:

- 01 EEROM byte cannot be correctly written
- 02 EEROM did not go to ready
- 04 EEROM checksum incorrect
- 08 EEROM setup incorrect (different firmware version)

“PPI Port Failure [6E or 6F.xx.yy]”

Explanation. The 2PPI Register and Character check has failed. The hexadecimal error code is 6E (Port 0) or 6F (Port 1), xx is the subtest, and yy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the 2PPI ports on the Terminal Control board. An error in this test is non-fatal. Refer to the subtest descriptions for information regarding when the test is performed.

Subtest and Submessage Codes. The following codes identify the circuitry in which the error occurred:

01 PPI Xmit/Receive check (can have multiple errors)

This test is performed during Power-up and Extended Self-tests, and Cycle testing.

- 01 SCC status bits failed on transmission of first character
- 02 SCC status bits failed on transmission of second character
- 04 SCC status bits failed on transmission of third or fourth character
- 08 SCC status bits failed on reception of character
- 10 Failed to receive correct first character (00)
- 20 Failed to receive correct second character (0FF)
- 40 Failed to receive correct third character (55)
- 80 Failed to receive correct fourth character (0AA)

02 PPI Baud Rate check

This test is performed during Extended and Adjustment Self-tests only.

- 01 19200 baud failed
- 02 9600 baud failed
- 04 4800 baud failed
- 08 2400 baud failed
- 10 1200 baud failed
- 20 600 baud failed
- 40 300 baud failed
- 80 150 baud failed

03 Status Control Line check (can have multiple errors)

This test is performed during Adjustment Self-test only.

- 01 PPI CTS output not seen high
- 02 PPI CTS output not seen low
- 04 PPI DSR output not seen high
- 08 PPI DCD output not seen high
- 10 PPI DTR input not seen high
- 20 PPI DTR input not seen low

04 Baud Rate Control Register test

This test is performed during Power-up and Extended Self-tests, and during Cycle testing. The submessage is the bit in error.

“Hard Copy Port Failure [6C.xx.yyyy]”

Explanation. The hard copy check has failed. The hexadecimal error code is 6C, xx is the subtest, and yyyy is the submessage. The board failure LED is on the Terminal Control Board.

Description. This test checks the hard copy port on the Terminal Control board. An error in this test is non-fatal. Refer to the subtest explanations for information regarding when the test is run.

Subtest and submessage Codes. The following codes identify the circuitry in which the error occurred:

- 01 Register check
This test is performed during Power-up and Extended Self-tests, and Cycle testing.
yy is the bits in error
- 02 External Loopback test
This test is performed only during Adjustment Self-test.
 - 001 Data line 0 in error
 - 002 Data line 1 in error
 - 004 Data line 2 in error
 - 008 Data line 3 in error
 - 010 Data line 4 in error
 - 020 Data line 5 in error
 - 040 Data line 6 in error
 - 080 Data line 7 in error
 - 100 INPRIME-0 in error
 - 200 STROBE-0 in error
- 03 Print Pattern
This test can be performed only during Adjustment Self-test.
No submessage on this test

“Multiplier Failure [5E or 5F.xx.yy]”

Explanation. The multiplier check has failed. The hexadecimal error code is 5E (Multiplier 0) or 5F (Multiplier 1) and xx is the subtest. The board failure LED is on the Terminal Control Board.

Description. This test checks the multipliers on the Terminal Control board. An error in this test is non-fatal. This test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest Codes. The following codes identify the circuitry in which the error occurred (the codes represent the bit position of the set bit in the error message — there can be multiple errors):

- 01 Static register test failure
- 02 Unsigned multiply failure
- 04 2’s complement multiply failure
- 08 Arithmetic shifter failure

495X Tablet Check

The 495X Tablet check tests a 4950 Series Graphics Tablet and its interface when installed. The test results are printed on the screen of the terminal. There is no board failure LED. The test can be run only in Adjustment Self-test.

DISPLAY CONTROLLER SYSTEM TEST MODULE ERROR MESSAGES

“Display System Failure [9E.xx.yyyy]”

Explanation. The timing controller, index map, and color map check has failed. The hexadecimal error code is 9E, xx is the subtest, and yyyy is the submessage. The board failure LED is on the Display Control board.

Description. This test checks the timing controller, index map, and color map circuitry on the Display Control board. An error in this test is non-fatal. This test is performed during Extended Self-test and Cycle testing.

Subtest Codes. The following codes identify the circuitry in which the error occurred:

- 03 Vertical Blanking check
 - 01 VBLANK-0 not seen
 - 02 60 Hz too fast
 - 04 60 Hz too slow or 50 Hz too fast
 - 08 50 Hz too slow
- 08 Index Map check
 - yyyy is the failed index address.
- 09 Index and Color Maps test
 - yyyy is the failed color map address.

“Display System Failure [9A.xx.yy]”

Explanation. The Alpha/Cursor Overlay check has failed. The hexadecimal error code is 9A, xx is the subtest, and yy is the submessage. The board failure LED is on the Display Control board.

Description. This test checks the alpha and cursor overlay circuitry. An error in this test is non-fatal. This test is performed during Extended Self-test and Cycle testing.

Subtest Codes. The following codes identify the circuitry in which the error occurred:

- 02 Alpha Overlay Control Register check
 - yy is the bit in error.
- 03 Alpha Overlay RAM Address test
 - yy is the bit in error.
- 04 Alpha Overlay RAM All Ones test
 - yy is the bit in error.
- 05 Alpha Overlay RAM Unique Bit test
 - yy is the bit in error.
- 06 Alpha Overlay RAM All Zeros test
 - yy is the bit in error.
- 07 Alpha Overlay RAM Refresh test
 - yy is the bit in error.

“Graphics Display System Failure [97.xx.yy]”

Explanation. The Frame Buffer Interface check has failed. The hexadecimal error code is 97, xx is the subtest, and yy is the submessage. The board failure LED is on the Display Control board.

Description. This test checks the frame buffer interface circuitry on the Display Control board. An error in this test is non-fatal. This test is performed during Power-up and Extended Self-tests, and Cycle testing.

Subtest Codes. The following codes identify the circuitry in which the error occurred:

- 0A Pixel ALU Operations check
 - 02 “A OR B” operation failed
 - 03 “A AND B” operation failed
 - 04 “A XOR B” operation failed
 - 05 “A + B” operation failed
 - 06 “A - B” operation failed
 - 07 “No Op” failed (Output = A)
 - 08 “ALU output = 0” operation failed
 - 09 “A NOT” operation failed
 - 0A “B NOT” operation failed
 - 0D Invalid data received at “A” input from frame buffer
- 0B Vector Generator check
 - 01 Register check failed
 - 02 X address check failed
 - 03 Y address check failed
 - 04 Dash mask check failed
 - 05 Major and minor octants and associated logic check failed
 - 06 Index check failed
 - 07 Frame buffer path check failed

“Graphics Display System Failure [96.xx.yyyy]”

Explanation. The Frame Buffer check has failed. The hexadecimal error code is 96, xx is the subtest, and yyyy is the submessage. The board failure LED is on the Display Control board.

Description. This test checks the frame buffer circuitry on the Display Control board. An error in this test is non-fatal. Refer to the subtest descriptions for information regarding when this test is performed.

Subtest Codes. The following codes identify the circuitry in which the error occurred:

- 03 Pixel Walk test

This test is performed during Extended Self-test and Cycle testing.

yyyy is the pixel in error.
- 04 Short Memory test

This test is performed during Power-up and Extended Self-tests, and Cycle testing.

yyyy is the pixel in error.
- 05 Frame Buffer RAM Refresh Memory test

This test is performed during Extended Self-test and Cycle testing.

yyyy is the pixel in error.
- 0C Plane Uniqueness check

This test is performed during Power-up and Extended Self-tests, and Cycle testing.

yy is the Write Mask bit in error.
- 0D Write Mask Logic check

This test is performed during Extended Self-test and Cycle testing.

 - 01 Plane 0 failed
 - 02 Plane 1 failed
 - 04 Plane 2 failed
 - 08 Plane 3 failed
 - 10 Write to Frame Buffer failed

CX INTERFACE BOARD TEST MODULE ERROR MESSAGES (CX4111 ONLY)

“CX Interface Failure [10.xx]”

Explanation. The CX Interface board has failed. The hexadecimal error code is 10, xx is the subtest. Because the CX Interface board does not have a board failure LED, the board failure LED on the Terminal Control board lights to indicate a CX Interface error.

Description. This test checks the operation of the CX Interface board. An error in this test is non-fatal. This test is performed during Power-Up, Extended Self-test, and Cycle testing.

Subtest Codes. The following codes identify the circuitry on the CX Interface board in which the error occurred:

Initialization

- 00 Failed to initialize command flag to 0, apparently never powered up
- 10 Failed to clear command flag, never came out of Phase-1
- 20 Failed to set attention flag, check flag hardware

Register Checks

- 30 Bad data compare on Register 0, I/O address 180H
- 31 Bad data compare on Register 1, I/O address 182H
- 32 Bad data compare on Register 2, I/O address 184H
- 33 Bad data compare on Register 3, I/O address 186H
- 40 Board never came out of Phase-2

CX RAM Test by CX Processor

- 51 55 pattern failed
- 52 AA pattern failed
- 63 Address = Data pattern failed
- 54 00 pattern failed

Transceiver Test

- 81 Transmitter not active
- 91 Receiver not active
- A1 Transmitter not inactive
- B1 Receiver not ready
- C1 Receiver error
- D1 Receiver not inactive
- E1 Receiver D2-D9 error
- F1 Receiver D10-D11 error

CX RAM Test by Terminal Processor, address 80000 — 81FFF

- 55 Initial pattern load failed
- 56 Walking-one's pattern failed

CX RAM Test by Terminal Processor, with CX Processor contention

- 57 Initial pattern load failed
- 58 Walking-one's pattern failed
- 70 0080 CX Interface failed during contention tests

CX RAM Test by CX Processor, with Terminal Processor contention

- 59 0020 11 55 pattern failed
- 5A 0020 12 AA pattern failed
- 5B 0020 13 Address = Data pattern failed
- 5C 0020 14 00 pattern failed

Transceiver Test (again)

- 82 Transmitter not active
- 92 Receiver not active
- A2 Transmitter not inactive
- B2 Receiver not ready
- C2 Receiver error
- D2 Receiver not inactive
- E2 Receiver D2-D9 error
- F2 Receiver D10-D11 error

Section 7

INSTALLATION

INTRODUCTION

Installation of either a 4111 or CX4111 Computer Display Terminal consists of the following:

- Selecting an installation site
- Unpacking
- Checking line voltage settings
- Connecting cables and applying power
- Running Self-test
- Setting communication parameters
- Selecting a terminal operating mode
- Connecting to a host computer
- Testing communication
- Connecting peripheral devices

The terminal is preassembled and requires no assembly for initial installation. The only options to the terminal are external, and do not require disassembly of the terminal. Installation of optional keyboards are described later in this section.

If new internal options become available and are to be installed, disassembly of the terminal may be required. Option installation inside the terminal should be performed only by qualified service technicians.

SELECTING AN INSTALLATION SITE

The installation site you select for the terminal should meet the following requirements.

CAUTION

Because the terminal consumes a maximum of 500 W (1700 BTU/hour), do not block air flow or cover the terminal air vents in any way. This could cause overheating and result in circuit damage.

- **The site should provide enough room for adequate ventilation and cable routing.** The terminal air vents should be at least 2 inches (50 mm) from the nearest wall or surface. Allow at least 3 inches (75 mm) at the rear of the terminal for cable routing. Use Figure 7-1 (next page) as a guide.
- **The site should provide a stable environment.** While the terminal is operating, the ambient temperature should stay within 50 to 104° F (+ 10 to + 40° C).

Relative humidity should stay between 0 and 75%. Do not operate the terminal at an altitude greater than 10,000 ft (3050 m).

If any of these operating limits are exceeded, the terminal may not operate properly.

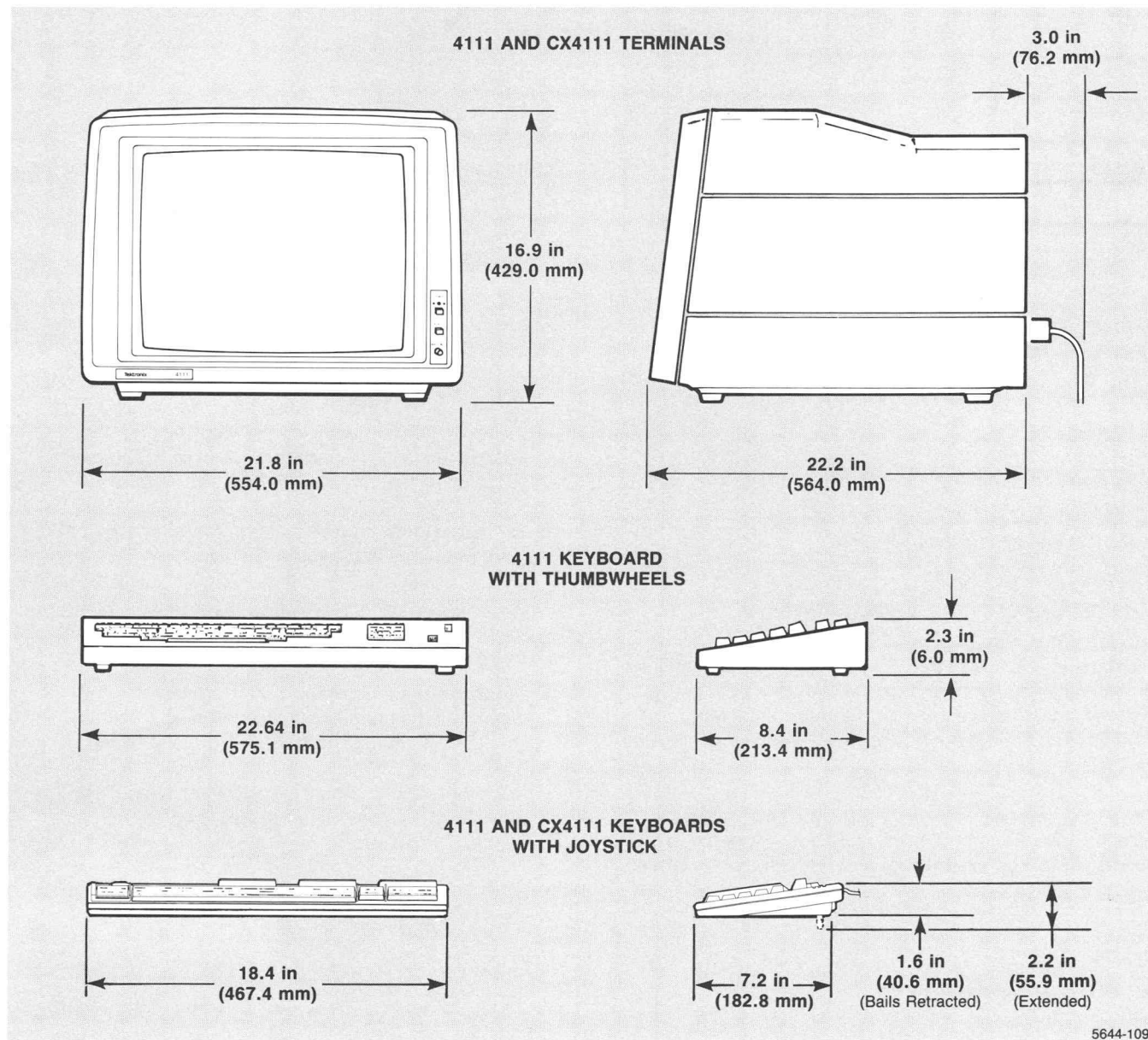


Figure 7-1. Dimensions.

UNPACKING

NOTE

If the terminal has already been unpacked, go to the next heading, "Checking the Operating Voltage."

Before unpacking the terminal, carefully inspect the shipping carton for any signs of damage. Report any damage to the carrier and the local Tektronix sales representative immediately.

Retain all packing material in case you need to move or ship the terminal in the future.

The terminal and all standard accessories are shipped in one carton. Unpack the carton by following these steps; use Figure 7-2 as a guide.

WARNING

Lifting awkward or heavy objects can cause personal injury. When moving the shipping carton or the terminal, be sure to use recommended safe lifting methods (or have an assistant help) to avoid back injury.

1. Use a carton opener to cut the plastic strapping on the shipping carton. Lift the entire shipping carton straight up and off.
2. Remove the keyboard box and put it aside.
3. Remove the side pads.
4. Remove the accessory box and put it aside.
5. Lift the terminal from the bottom tray and pallet and place it in the site previously selected.

6. Remove the keyboard from its carton and place in front of the terminal.
7. Remove the contents from the accessory box and check the equipment you received against the accessories list in Section 1 of this manual. If any items are missing, notify your Tektronix sales representative immediately.
8. Verify that the proper options (if any) are installed. A list of installed options is included on the serial number label located on the rear of the terminal.

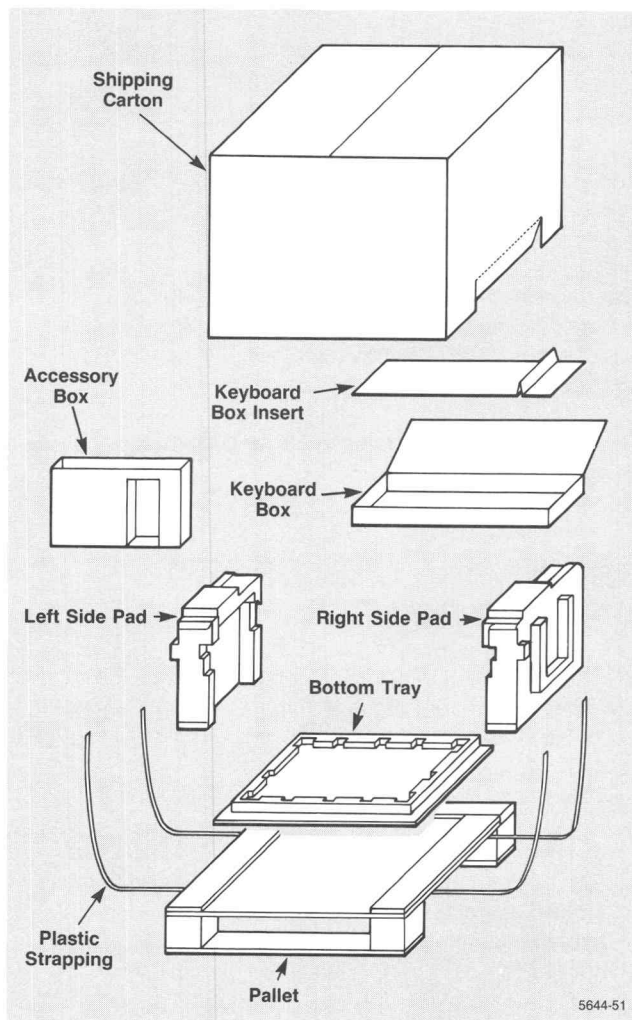


Figure 7-2. Packaging.

CHECKING THE OPERATING VOLTAGE

CAUTION

Both voltage selector switches at the rear of the terminal must be set to the same voltage. Setting the two switches to different voltages, or setting the switches to the wrong voltage, may seriously damage the terminal.

Changing the operating voltage should only be done by qualified service personnel.

Check the indicators on the voltage selector switches (see rear panel of terminal) to ensure that both switches are set to the proper operating voltage, as required by your ac power source. See Figure 7-3.

If the switches are not set to the proper voltage, or if they are not set to the same setting, move the switches to the correct setting. There are only two possible settings (115 Vac or 230 Vac).

Also, check that you have received the correct power cord (voltage and plug type).

CONNECTING CABLES AND APPLYING POWER

Refer to Figures 7-4 through 7-6, which identifies the connectors on the rear of the terminal and at the keyboard, then make these connections:

1. Plug the keyboard cable into the KYBD connector.
2. Connect the RS-232 cable to the COMPUTER port. Secure the cable connector to the terminal with the two small connector screws. Connect the other end of the cable either to a modem or directly to your host computer.

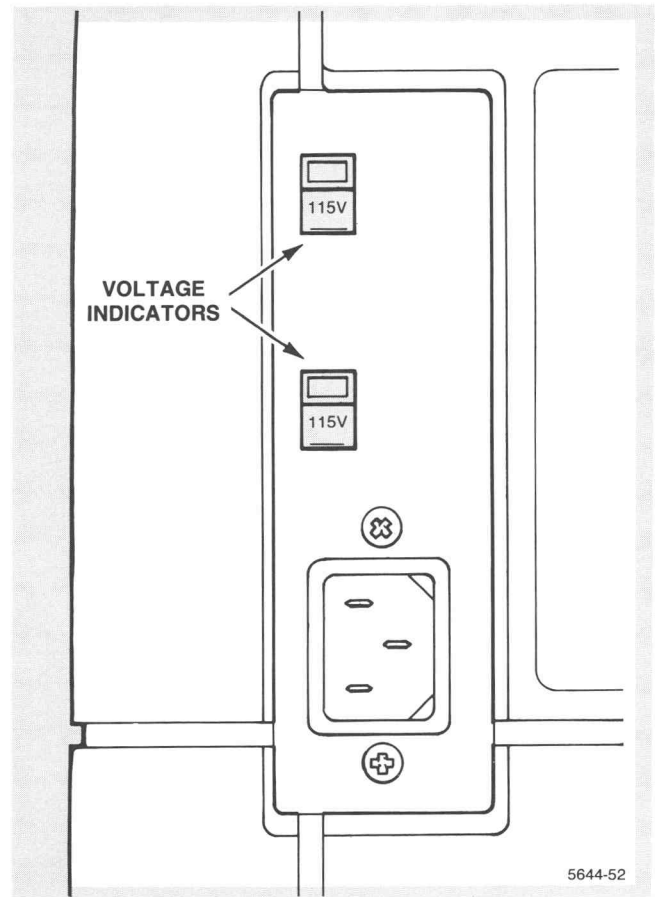


Figure 7-3. Voltage Indicator.

3. If the terminal (CX4111) is to be connected to an IBM host, connect the coaxial cable's BNC connector to the terminal's COMM port. Push and twist the cable's BNC connector into its locked position.
4. Attach the female end of the ac power cord to the rear panel of the terminal, and insert the male end into the ac power source.
5. If you have the 4111 keyboard with thumbwheels, you may connect an optional mouse (Option 4M) and joystick as described below:

NOTE

The joystick is a customer-supplied item. The filter is a customer-ordered item used only to prevent electrical interference. Joydisk-style keyboards do not support a joystick.

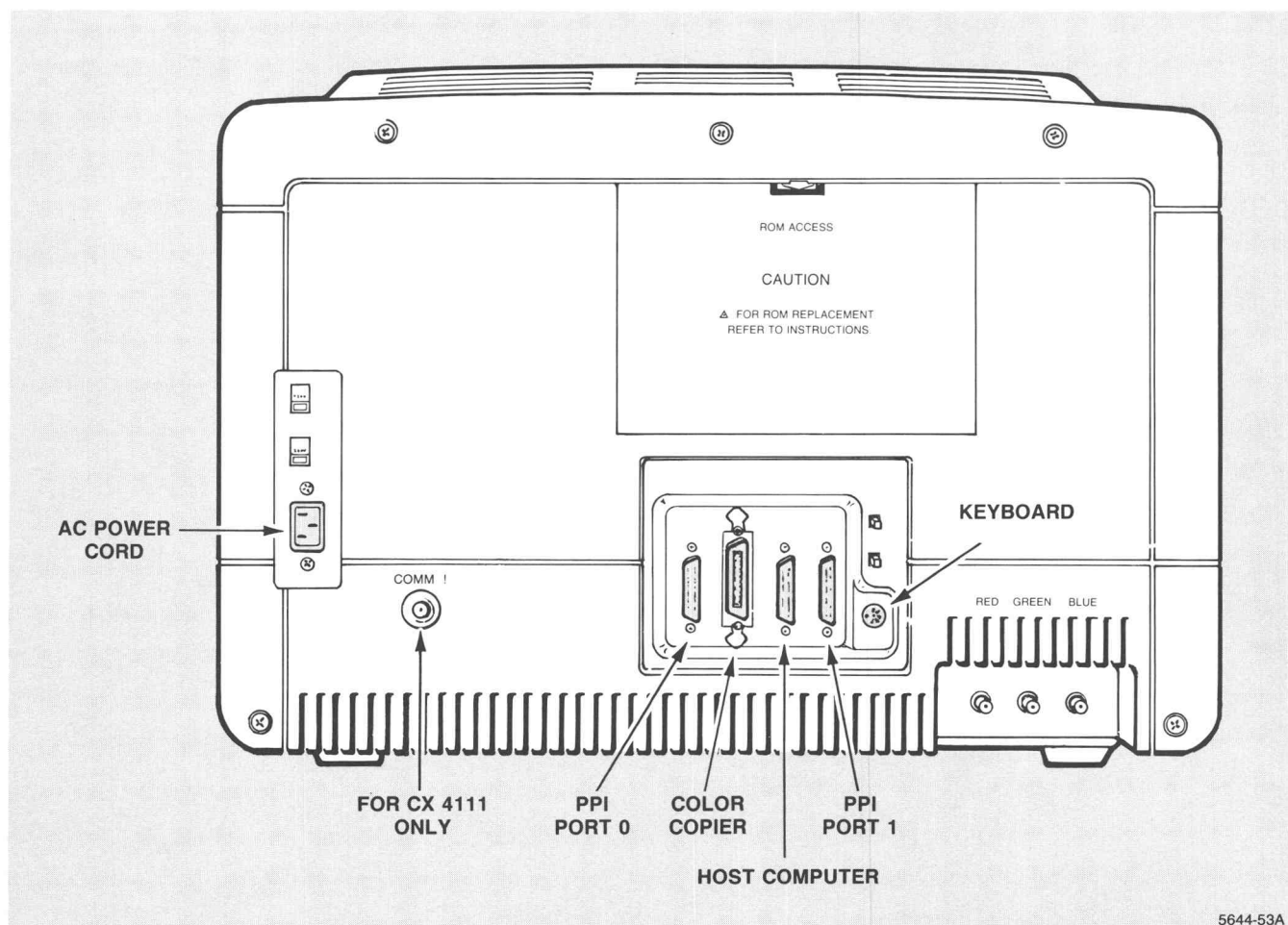


Figure 7-4. Terminal Connector Locations.

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INSTALLATION

- Connect the filter and mouse cable at the TO MOUSE port (right port looking at the back of the keyboard as shown in Figure 7-5). Using the locking screws supplied, connect the filter to the port. Move the slide mechanism on the mouse plug to one side, attach the plug to the filter, and slide the mechanism back to lock the plug to the filter.

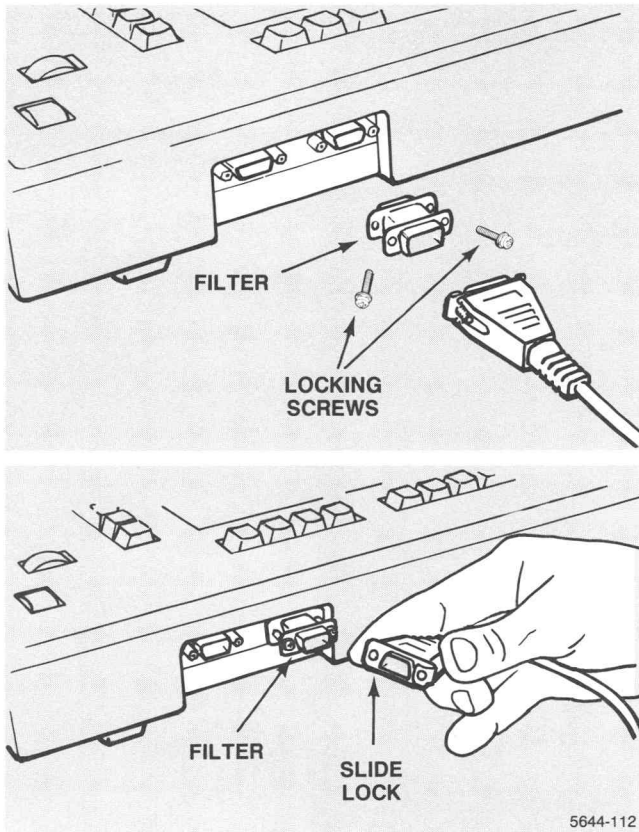


Figure 7-5. Installing a Mouse and Filter.

- Connect a joystick and filter to the male keyboard port (left port looking at the back of the keyboard, as shown in Figure 7-6). The joystick plugs directly into the male port. To install the joystick with a filter, attach the filter to the male port (using the screws supplied with the filter) and plug the joystick into the filter.

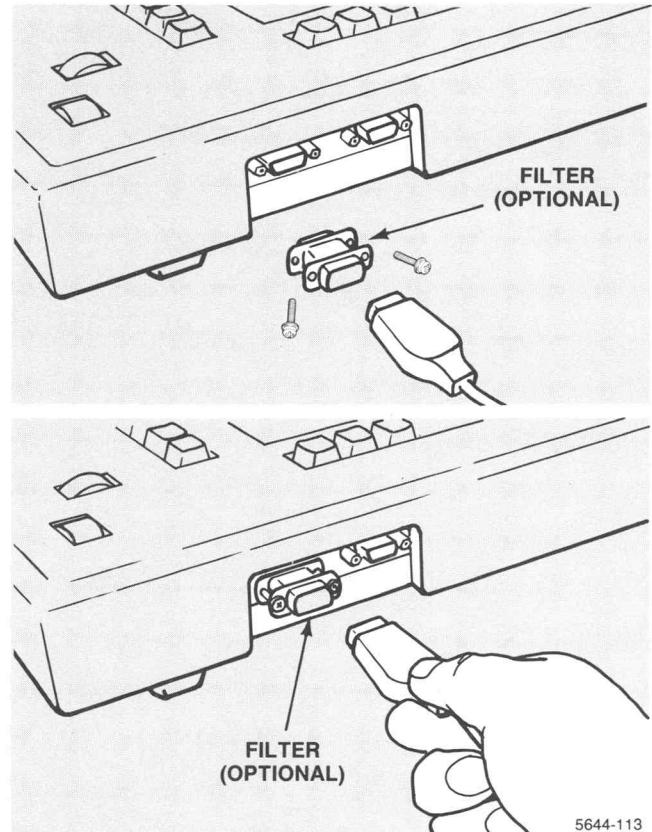


Figure 7-6. Installing a Joystick and Filter.

6. If you have the 4111 keyboard with Joydisk or the CX4111 keyboard, you may connect an optional mouse (Option 4M). Simply plug the mouse cable into the 9-pin port at the rear of the keyboard.
7. Push in the power switch (Figure 7-7). The terminal should power up and the cooling fan should start. Wait a few seconds until the cursor appears in the upper left corner of the screen. If any LEDs stay lit (on the standard keyboard with thumbwheels) and the keyboard bell rings, or if the cursor does not appear, run Self-test (described in Section 3).

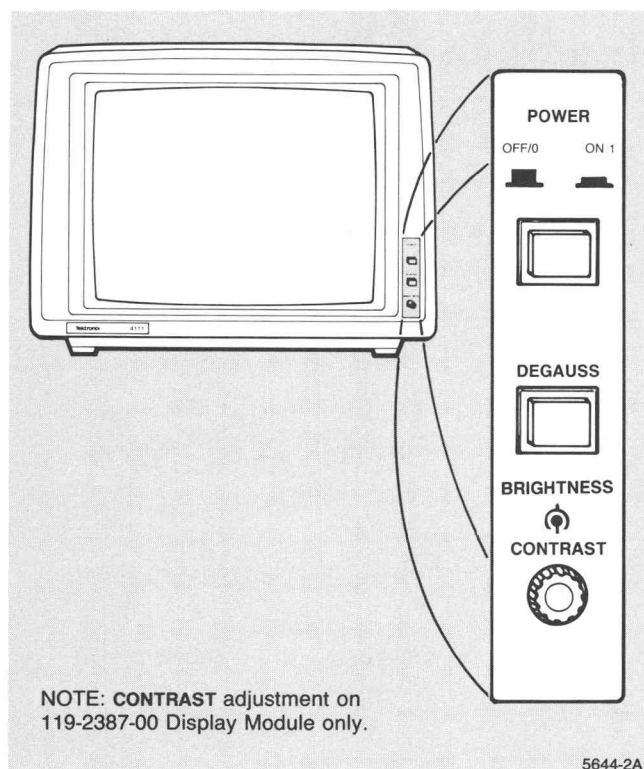


Figure 7-7. Power Switch.

RUNNING SELF-TEST

Run the Extended Self-test program (described here) to verify that the terminal is operating correctly (if necessary, refer to Section 3 for locations of the keys and controls you will use in these steps):

1. Locate the SELF TEST and RESET buttons on the rear of the terminal.
2. Press SELF TEST and hold it in. While holding in SELF TEST, press and release RESET.
3. Hold in SELF TEST for another two seconds, then release it. The keyboard LEDs light sequentially from right to left (cycle) indicating that Extended Self Test is running. (On keyboards with the Joydisk, the Caps Lock light comes on.) After about 30 seconds, the keyboard bell rings. Press any alphanumeric key on the keyboard to continue.

If the terminal detects a failure, it rings the keyboard bell twice, writes a message on the screen, or both. (If no message appears, try turning up the BRIGHTNESS knob.) If a failure is indicated, refer to the last part of Section 6, which tells you what to do. In addition, you may perform the Functional Check in Section 5.

After you have verified that the terminal is functioning properly, you can continue with these installation procedures.

SETTING COMMUNICATION PARAMETERS

If this is the first time you have used a 4111 or CX4111 terminal, or if you need instructions for entering Setup commands, we suggest that you read the *4111 Computer Display Terminal Operators Manual*. Read specifically, "Setting Communication Parameters," in the *Installation and Setup* appendix, to perform setup procedures. Setup commands for the CX4111 Terminal are listed in the *CX4111 Users Information Supplement*.

The terminal is already configured by the factory for typical RS-232 host communications; however, you may need to change some of the terminal settings to match the settings of your host computer.

SELECTING A TERMINAL OPERATING MODE

The terminal has four modes of operation that are compatible with a variety of host applications programs. These modes are:

- **TEK** — For programs that use Tektronix 4100-style graphics and terminal control commands.
- **ANSI** — For programs that use ANSI Standard X3.64 text editing commands.
- **EDIT** — For DEC VT100 applications programs.
- **VT52** — For DEC VT52 applications programs.

Check with your computer center staff or your systems programmer to determine which mode you should use to communicate with your host computer. Then refer to the Operators manual for the following process:

1. Put the terminal into Setup mode (press the Setup key) and select the operating mode with the **CODE** command (for example, use **CODE ANSI** to select ANSI mode).
2. Save the selected mode in nonvolatile memory by using the **NVSAVE** command. Nonvolatile memory is not erased when the terminal is turned off or reset.
3. Remove the terminal from Setup mode (press the Setup key again).

CONNECTING TO A HOST COMPUTER

In general, the host port RS-232 cable can be connected to the host computer in three ways (largely depending on the distance between the terminal and the host computer):

- Directly to the host computer (although usually an asynchronous modem eliminator is needed).
- To a "short haul" modem or line driver device (when the host computer is in the same building or building complex, but not in the same room or immediate area).
- To a modem which conveys information through a telephone line to another modem at the host computer (when the host computer is a long distance from the terminal).

TELEPHONE LINE CONNECTION

A modulator-demodulator (modem) is required to establish a telephone line connection. There are a number of specialized modems available. The type required depends upon the specific needs of the installation.

A host port RS-232 cable is included with the terminal as a standard accessory. Connect one end of the RS-232 cable to the rear of the terminal at the connector designated "Computer" and connect the other end to the modem.

Once the terminal and the modem are connected, the general procedure for establishing communications with the host computer is as follows (this procedure may vary in some details for different computer installations):

1. Power up the equipment.
2. Dial the number of the computer installation.
3. When the computer responds with an audible tone, do one of the following:
 - Place the telephone headset on the cradle provided in the modem.
 - OR
 - Push the button marked **DATA** and hang up the headset.
 - OR
 - Perform such other function as required by the modem in use.
4. Perform the sign-on procedure as required by the particular computer installation.

TESTING COMMUNICATIONS

Once the host computer-to-terminal connection has been made (in any of the three basic ways using the RS-232 cable), perform the sign-on or logging-in procedure that is required by your specific host computer. Once you have "signed-on" to the system, the communication lines between the host computer and the terminal should be open and you should be able to "talk" to the computer. You should try a few of the basic system commands to ensure that no communication problems exist.

Testing the communication provides the final verification of proper operation. The terminal is now ready for use.

CONNECTING PERIPHERAL DEVICES

The following instructions help you connect peripheral devices to the terminal and set their communications parameters. You should also follow any other installation instructions provided with the peripheral device.

The remaining portion of this section contains installation procedures for:

- 4691 and 4692 Color Graphics Copiers
- 4695 Color Graphics Copier
- 4696 Color Ink-Jet Printer
- 4634 Monochrome Copier with Option 11
- 4662 Interactive Digital Plotter
- 4663 Interactive Digital Plotter
- 4957 and 4958 Graphics Tablets
- 4510 and 4510A Rasterizers

You need only refer to those procedures that apply to the device you want to install.

NOTE

Some applications software running on a host computer may require that some peripherals, such as a 4662 Plotter, be connected to a specific port. Check with your systems programmer.

The Operators manual explains the Setup commands to use for making copies and how to use a graphics tablet.

NOTE

You can connect a copier directly to the terminal to make color hard copies, as described in the following paragraphs, or you may use a 4510 or 4510A Rasterizer-color copier combination connected to PORT 0 or PORT 1. If you use the Rasterizer-copier combination, refer to 4510 RASTERIZER later in this section.

4691 AND 4692 COLOR GRAPHICS COPIERS

1. Plug the copier cable into the COPIER port. Secure the cable connector with the two clips attached to the port.

4695 COLOR GRAPHICS COPIER

1. Plug the copier cable into the COPIER port. Secure the cable connector with the two clips attached to the port.
2. You may need to set the C and M ADJUST switches on the rear panel of the 4695.
 - Switch C tells the copier whether to ignore Carriage Returns from the terminal. If the copier double-spaces lines of text or prints a new line of text on top of the previous line, change the switch setting.
 - Switch M ADJUST tells the copier whether to print in one direction or in two directions. Bidirectional printing is faster, but the dot alignment is better with one-directional printing. For highest quality copies, use the slower, one-directional setting.

4696 COLOR INK-JET PRINTER

1. Plug the copier cable into the COPIER port. Secure the cable connector with the two clips attached to the port.
2. You may also need to set Switch 4 on the rear panel, and press the MEDIA button on the front of the printer.
 - Switch 4 tells the copier whether to ignore Carriage Returns from the terminal. If the copier double-spaces lines of text or prints a new line of text on top of the previous line, change the switch setting.
 - The MEDIA button selects the type of media — paper or film (transparency) — to be copied on. When set to PAPER, the printer prints bidirectionally. When set to FILM, the printer prints in one direction only. This allows more time for the ink to dry on the film and provides a slightly better dot alignment.

INSTALLATION

4634 MONOCHROME COPIER

The 4634 Monochrome Copier must have Option 11 (Tektronix 4111 Compatibility) installed. A 4634 Copier with Option 11 will also include an RGB Mixer (016-0596-06) as part of the equipment package.

1. Use three 75 ohm BNC cables to connect a 4111 or CX4111 to the RGB Mixer. (Connect one end of a BNC cable to the RED output connector on the terminal. Connect the cable's free end to the RED input connector of the RGB Mixer. Perform the same procedure to connect the Green and Blue signal lines between the terminal and the RGB Mixer.)
2. Use another 75 ohm BNC cable to connect the RGB Mixer to the 4634 Copier. (Connect one end of the cable to the OUTPUT connector on the RGB Mixer. Connect the cable's other end to the VIDEO connector on the rear panel of the 4634 Copier.)

4662 INTERACTIVE DIGITAL PLOTTER

1. Connect the plotter RS-232 cable from the "modem" connector on the rear of the plotter to the terminal PORT 0 or PORT 1 port. (For this discussion, assume the plotter is connected to PORT 0.)
2. Set the plotter switches. Table 7-1 shows one way to set the 4662 Plotter switches; this configuration is recommended for communicating with the terminal. The settings not shown in the table use the plotter power-up defaults.

Table 7-1

4662 PLOTTER SETTINGS

Switch	Setting	Communications Parameter ^a
A	3	CR generates LF No Flagging
B	3	Number of Stop Bits is 1
C	2	Address is A No Parity
D	3	Baud rate is 1200

^a Each plotter switch controls more than one communications parameter.

3. Power up the terminal.

4. Use Setup commands to configure the peripheral port. Put the terminal in Setup mode (press the Setup key) and enter these commands:

```
PASSIGN P0:,4662
PFLAG P0:,NONE
PBITS P0:,1,8
PPARITY P0:,NONE
PBAUD P0:,1200
NVSAVE
```

If the plotter is connected to PORT 1, use P1: instead of P0: in the above commands.

5. Power up the plotter and prepare the plotter pen and paper for use.

Other plotter settings may be used; check with your systems programmer. Be sure to configure the terminal port to match the plotter settings.

Configuring a 4662 Plotter With Option 31

If you have a 4662 with Option 31 (multiple-pen plotter), follow the steps for the 4662, but use this PASSIGN command instead:

```
PASSIGN P0:,4662/MP
```

If the plotter buffer overflows, you should use DC1/DC3 flagging (available only if you have Option 31). Enter this PFLAG command instead:

```
PFLAG P0:,CHAR
```

If you use other plotter settings, be sure to configure the terminal port to match.

4663 INTERACTIVE DIGITAL PLOTTER

1. Connect the plotter's RS-232 cable from the "modem" connector on the rear of the plotter to the terminal's PORT 0 or PORT 1 port. (For this discussion, assume the plotter is connected to PORT 0.)
2. Set the plotter switches. Table 7-2 shows one sequence of 4663 parameter settings for communicating with the terminal. The settings not shown use the plotter power-up defaults. (The 4663 Operators manual tells you how to enter the parameter settings.)

Table 7-2

4663 PLOTTER SETTINGS

Parameter	Setting
Output Terminator	CR
Attention Character	<ESC>
Interface Functions	CR Generates LF DEL IGNORE
Communications Control Mode	Full Duplex
Receive Parity	Ignore
Transmit Parity	Logic 0
Character Format	8 Data Bits 1 Stop Bit
Transmit Baud Rate	9600
Receive Baud Rate	9600
Serial Device Address	A
Initial Command/ Response Format	3 (emulates a 4662)
Interface Select	1 (RS-232 interface)
Initial Axis Orientation	Y vertical, X horizontal
Initial Aspect Ratio	4X:3Y

3. Power up the terminal.
4. Use Setup commands to configure the peripheral port. Put the terminal in Setup (press the Setup key) and enter the following commands:

```
PASSIGN P0:,4663
PFLAG P0:,NONE
PPARITY P0:,NONE
PBITS P0:,1,8
PBAUD P0:,9600
NVSAVE
```

If the plotter is connected to PORT 1, use P1: instead of P0: in the previous commands.

5. Power up the plotter and prepare the plotter pen and paper for use.

Other plotter settings may be used; for example, you could use DC1/DC3 flagging. If you use other plotter settings, be sure to configure the terminal port to match.

4957 AND 4958 GRAPHICS TABLETS

1. Connect the puck or stylus cable to the tablet.
2. Connect the tablet communications cable to either the PORT 0 or PORT 1 connector on the rear of the terminal. (For this discussion, assume the tablet is connected to PORT 0.)
3. Plug in the tablet power cord to a standard power outlet.
4. Enter Setup and enter the following commands:

```
PASSIGN P0:,4957
PFLAG P0:,NONE
PPARITY P0:,ODD
PBITS P0:,1,7
PBAUD P0:,9600
PEOF P0:,"
PEOL P0:,"
```

INSTALLATION

4510 SERIES COLOR GRAPHICS RASTERIZER

1. Connect the rasterizer's RS-232 communications cable to the terminal's PORT 0 or PORT 1 (For the following discussion, assume that the rasterizer is connected to PORT 0). Secure the cable connector to the port by tightening the two small connector screws.
2. Connect the copier (4691, 4692, 4695, or 4696) to the rasterizer (see the Rasterizer Operator's manual), and turn on both the rasterizer and the copier.

NOTE

The following Setup commands are suggested entries. Entries may differ for your application. For example, Baud Rate, Parity, Flagging, and Bits can be set to any value, as long as the rasterizer is set the same. Refer to command descriptions in Section 4 of the 4111 Operators manual for specific meanings of parameter choices.

3. Place the terminal in Setup mode, and enter:

```
PASSIGN P0:;4510
PBAUD P0:;19200
PPARITY P0:; NONE
PFLAG P0:;CHAR,Ctrl-Q,Ctrl-S
PBITS P0:;1,S
PINVERSION P0:;1
PCOPIES P0:;1
PORIENT P0:;VTOP
PREPAINT P0:;1
PQUEUE P0:;4500
```

NOTE

Ctrl-Q and Ctrl-S mean to hold down the CTRL key while pressing the Q or S key. Do not type the hyphen.

4. Save the settings in nonvolatile memory by entering:

```
NVSAVE
```

5. The rasterizer's communications parameters must match those of the terminal's port. Refer to the Rasterizer Operator's manual, and set the rasterizer's parameters as shown here (to match the settings in Step 3 above):
 - Set transmit and receive baud rate to 19200
 - Set parity to *no parity* (indicator should read 0)
 - Set flagging to D_1/D_3 , bidirectional
 - Set stop bits to 1
6. Refer to the procedures under "4510/A Rasterizer" in Section 3 of the 4111 Operators manual to transmit files from the terminal to the rasterizer (and subsequently to the copier).

REPACKAGING FOR SHIPMENT

If the terminal is to be shipped long distances by commercial transportation, you should repackage the terminal as originally shipped from the factory. The carton and packing material in which the terminal was initially shipped should be saved for this purpose.

If the terminal is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing the following:

- The name of the Owner (with address)
- The name of a person who can be contacted
- Terminal type and serial number
- An explanation of the service required

Refer to the packaging illustration (Figure 7-2) when repackaging the terminal for shipment.

Section 8 REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
00853	SANGAMO MESTON INC	SANGAMO RD	PICKENS SC 29671
	SANGAMO CAPACITOR DIV	P O BOX 128	
01121	ALLEN-BRADLEY CO	1201 SOUTH 2ND ST	MILWAUKEE WI 53204
01295	TEXAS INSTRUMENTS INC	13500 N CENTRAL EXPRESSWAY	DALLAS TX 75265
	SEMICONDUCTOR GROUP	P O BOX 225012 M/S 49	
01537	MOTOROLA COMMUNICATIONS AND ELECTRONICS INC	2553 N EDGINGTON ST	FRANKLIN PARK IL 60131
02660	BUNKER RAMO CORP	2801 S 25TH AVE	BROADVIEW IL 60153
	AMPHENOL NORTH AMERICA DIV		
03508	GENERAL ELECTRIC CO	M GENESEE ST	AUBURN NY 13021
	SEMI-CONDUCTOR PRODUCTS DEPT		
03888	KOI PYROFILM CORP	60 S JEFFERSON RD	WHIPPANY NJ 07981
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC	5005 E MCDOWELL RD	PHOENIX AZ 85008
	SEMICONDUCTOR GROUP		
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
05828	GENERAL INSTRUMENT CORP	600 M JOHN ST	HICKSVILLE NY 11802
	GOVERNMENT SYSTEMS DIV		
07263	FAIRCHILD CAMERA AND INSTRUMENT CORP	464 ELLIS ST	MOUNTAIN VIEW CA 94042
	SEMICONDUCTOR DIV		
07716	TRM INC	2850 MT PLEASANT AVE	BURLINGTON IA 52601
	TRM ELECTRONICS COMPONENTS		
	TRM IRC FIXED RESISTORS/BURLINGTON		
11236	CTS OF BERNE INC	406 PARR ROAD	BERNE IN 46711
13075	SAVOY ELECTRONICS INC	P O BOX 5727	FORT LAUDERDALE FL 33310
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
14193	CAL-R INC	1601 OLYMPIC BLVD	SANTA MONICA CA 90404
14552	MICRO/SEMICONDUCTOR CORP	2830 S FAIRVIEW ST	SANTA ANA CA 92704
14752	ELECTRO CUBE INC	1710 S DEL MAR AVE	SAN GABRIEL CA 91776
18324	SIGNETICS CORP	811 E ARQUES	SUNNYVALE CA 94086
19701	MEPCO/ELECTRA INC	P O BOX 760	MINERAL WELLS TX 76067
	A NORTH AMERICAN PHILIPS CO		
22526	DU PONT E I DE NEMOURS AND CO INC	30 HUNTER LANE	CAMP HILL PA 17011
	DU PONT CONNECTOR SYSTEMS		
22753	UID SWITCHES INC	6615 M IRVING PARK RD	CHICAGO IL 60634
	DIV OF ILLINOIS TOOL WORKS INC		
24355	ANALOG DEVICES INC	RT 1 INDUSTRIAL PK P O BOX 280	NORWOOD MA 02062
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051
27264	MOLEX INC	2222 MELLINGTON COURT	LISLE IL 60532
	CORPORATE HQ		
31433	UNION CARBIDE CORP	PO BOX 5928	GREENVILLE SC 29606
	ELECTRONICS DIV		
31918	ITT SCHAUM INC	8081 MALLACE RD	EDEN PRAIRIE MN 55343
32997	BOURNS INC	1200 COLUMBIA AVE	RIVERSIDE CA 92507
	TRIMPOT DIV		
34335	ADVANCED MICRO DEVICES	901 THOMPSON PL	SUNNYVALE CA 94086
34371	HARRIS SEMICONDUCTOR DIV OF HARRIS CORP	P O BOX 883	MELBOURNE FL 32901
34649	INTEL CORP	3065 BOMERS AVE	SANTA CLARA CA 95051
50364	MONOLITHIC MEMORIES INC	1165 E ARQUES AVE	SUNNYVALE CA 94086
51642	CENTRE ENGINEERING INC	2820 E COLLEGE AVE	STATE COLLEGE PA 16801
53387	MINNESOTA MINING AND MFG CO	3M CENTER	ST PAUL MN 55101
	ELECTRONIC PRODUCTS DIV		
54407	POWER-ONE INC	740 CALLE PLANO DR	CAMARILLO CA 93010
54473	MATSUSHITA ELECTRIC CORP OF AMERICA	ONE PANASONIC WAY	SECAUCUS NJ 07094
54583	TOK ELECTRONICS CORP	755 EASTGATE BLVD	GARDEN CITY NY 11530
55112	WESTLAKE CAPACITORS INC	5334 STERLING CENTER DRIVE	WESTLAKE VILLAGE CA 91361
55680	NICHICON /AMERICA/ CORP	927 E STATE PKY	SCHAUMBURG IL 60195
56289	SPRAGUE ELECTRIC CO	87 MARSHALL ST	NORTH ADAMS MA 01247
56708	ZILOG INC	10460 BUBB RD	CUPERTINO CA 95014
57668	ROHM CORP	16931 WILLIKEN AVE	IRVINE CA 92713

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
58224	XENELL CORP	HMY 77 S P O BOX 726	MYNNEM000 OK 73098
58361	GENERAL INSTRUMENT CORP OPTOELECTRONICS DIV	3400 HILLVIEW AVE	PALO ALTO CA 94304
59660	TUSONIX INC	2155 N FORBES BLVD	TUCSON, ARIZONA 85705
59821	CENTRALAB INC SUB NORTH AMERICAN PHILIPS CORP	7158 MERCHANT AVE	EL PASO TX 79915
61935	SCHURTER INC	1016 CLEGG COURT	PETALUMA CA 94952
71400	MCGRAM-EDISON CO BUSSMANN MFG DIV	502 EARTH CITY PLAZA P O BOX 14460	ST LOUIS MO 63178
71468	ITT CANNON ELECTRIC DIV INTERNATIONAL TELEPHONE AND TELEGRAPH CO	666 E DYER RD	SANTA ANA CA 92702
75042	TRW INC TRW ELECTRONIC COMPONENTS IRC FIXED RESISTORS PHILADELPHIA DIV	401 N BROAD ST	PHILADELPHIA PA 19108
75915	LITTELFUSE INC	800 E NORTHWEST HMY	DES PLAINES IL 60016
80009	TEKTRONIX INC	4900 S M GRIFFITH DR P O BOX 500	BEAVERTON OR 97077
81312	MINCHESTER ELECTRONICS DIVISION LITTON SYSTEMS INC	MAIN STREET AND HILLSIDE AVENUE	OAKVILLE CT 06779
82389	SWITCHCRAFT INC SUB OF RAYTHEON CO	5555 N ELSTRON AVE	CHICAGO IL 60630
91637	DALE ELECTRONICS INC	P O BOX 609	COLUMBUS NE 68601
96214	TEXAS INSTRUMENTS INC EQUIPMENT GROUP	13500 N CENTRAL EXPY P O BOX 226015	DALLAS TX 75266
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO CA 91341
TK0961	NEC ELECTRONICS USA INC	401 ELLIS ST	MOUNTAIN VIEW CA 94043
TK1360	DALE ELECTRONICS INC	BOX 26950	EL PASO TX 79926
TK1483	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
TK1504	IMS EQUIPMENT INC	2804 BARRANCA	IRVINE CA 92714
TK1873	CADIC INC	10150 SM NIMBUS AVE SUITE E-2	TIGARD OR 97223

REPLACEABLE ELECTRICAL PARTS
TERMCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-8523-40	8010100 8010214	CIRCUIT 80 ASSY:TERMINAL CONTROL	80009	670-8523-40
A	670-8523-41	8010215 8010687	CIRCUIT 80 ASSY:TERMINAL CONTROL	80009	670-8523-41
A	670-8523-42	8010688 8021497	CIRCUIT 80 ASSY:TERMINAL CONTROL	80009	670-8523-42
A	670-8523-43	8021498	CIRCUIT 80 ASSY:TERMINAL CONTROL (FOR FIRMWARE SET ORDER 020-1415-01)	80009	670-8523-43
C112	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C115	290-1021-00		CAP,FXD,ELCTLT:47UF,10VDC	56289	1730476X0010X
C124	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C130	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C170	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C172	290-1021-00		CAP,FXD,ELCTLT:47UF,10VDC	56289	1730476X0010X
C174	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C180	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C182	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C184	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C190	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C212	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C220	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C230	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C240	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C242	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C250	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C252	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C290	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C310	290-1021-00		CAP,FXD,ELCTLT:47UF,10VDC	56289	1730476X0010X
C320	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C370	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C372	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C392	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C410	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C414	290-1122-00		CAP,FXD,ELCTLT:22UF,20%,25V	55680	TLB1E220M
C420	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C422	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C424	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C430	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C440	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C442	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C450	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C460	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C472	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C474	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C476	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C478	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C479	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C480	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C482	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C484	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C485	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C486	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C488	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C489	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C490	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C491	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C492	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C494	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C510	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C520	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C522	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA

REPLACEABLE ELECTRICAL PARTS
TERMCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
C524	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C526	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C528	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C529	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C530	290-1120-00		CAP, FXD, ELCTLT:6.8UF, 20%, 25V	55680	TLB1E6R8M
C540	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C542	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C554	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C560	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C564	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C572	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C574	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C580	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C582	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C584	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C590	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C594	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C614	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C620	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C622	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C624	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C630	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C650	281-0861-00		CAP, FXD, CER DI:270PF, 5%, 50V	54583	MA12C0G1H271J
C652	281-0814-00		CAP, FXD, CER DI:100 PF, 10%, 100V	04222	MA101A101KAA
C656	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C660	281-0813-00		CAP, FXD, CER DI:0.047UF, 20%, 50V	05397	C412C473M5V2CA
C661	281-0813-00		CAP, FXD, CER DI:0.047UF, 20%, 50V	05397	C412C473M5V2CA
C662	281-0813-00		CAP, FXD, CER DI:0.047UF, 20%, 50V	05397	C412C473M5V2CA
C664	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C668	281-0770-00		CAP, FXD, CER DI:1000PF, 20%, 100V	04222	MA101C102MAA
C672	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C674	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C680	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C682	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C684	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C690	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C694	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C720	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C724	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C730	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C760	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C762	281-0775-00		CAP, FXD, CER DI:0.1UF, 20%, 50V	04222	MA205E104MAA
C764	281-0775-00		CAP, FXD, CER DI:0.1UF, 20%, 50V	04222	MA205E104MAA
C772	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C774	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C780	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C782	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C784	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C790	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C794	281-0925-00		CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C810	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C820	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C824	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C826	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C828	290-1021-00		CAP, FXD, ELCTLT:47UF, 10VDC	56289	173D476X0010X
C862	281-0770-00		CAP, FXD, CER DI:1000PF, 20%, 100V	04222	MA101C102MAA
C864	281-0770-00		CAP, FXD, CER DI:1000PF, 20%, 100V	04222	MA101C102MAA
C890	290-1021-00		CAP, FXD, ELCTLT:47UF, 10VDC	56289	173D476X0010X
CR474	152-0141-02		SEMICOND DVC, DI:5W, SI, 30V, 150MA, 30V	03508	0A2527 (1N4152)

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
CR476	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR570	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR572	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR574	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR576	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR630	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR670	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR672	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR760	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR824	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR826	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
DS242	150-1036-00		LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
DS244	150-1036-00		LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
F212	159-0246-00		FUSE,WIRE LEAD:3.5A,125V,FAS I	75915	251 03.5
F310	159-0250-00		FUSE,WIRE LEAD:16A,5 X 20 MM	61935	034.3629
F410	159-0153-00		FUSE,WIRE LEAD:1.5A,125V,FAST BLOW	71400	A1 1/2
J11	131-3436-00		CONN,RCPT,ELEC:1 X 15,RT ANGLE,0.156 SPACIN G,POLARIZED,GOLD PINS	27264	09-47-1152
J13	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	TK1483	073-96914-390
J20	131-0971-00		CONN,RCPT,ELEC:CKT BD MT,25 CONTACT,FEMALE	71468	0825-SH
J21	131-2898-00		CONN,RCPT,ELEC:PCB MOUNT,36 CONTACT	02660	57-40360-22-398
J22	131-0813-00		CONN,RCPT,ELEC:CKT BD MT,25 CONT,MALE	13511	177-08-25P-T
J23	131-0971-00		CONN,RCPT,ELEC:CKT BD MT,25 CONTACT,FEMALE	71468	0825-SH
J25	131-1741-00		CONN,RCPT,ELEC:PCB MOUNT,5 CONTACT	82389	57NC5F
J28	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	TK1483	073-96914-390
J120	131-3437-00		CONN,RCPT,ELEC:HEADER,MALE,RT ANGLE,2 PIN	27264	703-91-0071
L864	108-0474-00		COIL,RF:FIXED,2UH	80009	108-0474-00
L866	108-0474-00		COIL,RF:FIXED,2UH	80009	108-0474-00
LS535	119-1427-01		XDCR,AUDIO:1-4.2KHZ,30MA,6V	TK1066	QMB-06
Q530	151-0188-00		TRANSISTOR:PMP,SI,T0-92	80009	151-0188-00
Q634	151-0190-00		TRANSISTOR:PMP,SI,T0-92	80009	151-0190-00
R112	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R120	315-0330-00		RES,FXD,FILM:33 OHM,5Z,0.25M	19701	5043CX33R00J
R210	315-0330-00		RES,FXD,FILM:33 OHM,5Z,0.25M	19701	5043CX33R00J
R220	315-0101-00		RES,FXD,FILM:100 OHM,5Z,0.25M	57668	NTR25J-E 100E
R290	307-0383-00		RES NTWK,FXD,FI:13,4.7K OHM,ZZ,0.25M	03888	PD14L 4.7K GB
R314	315-0101-00		RES,FXD,FILM:100 OHM,5Z,0.25M	57668	NTR25J-E 100E
R370	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R372	307-0649-00		RES NTWK,FXD,FI:8,33 OHM,ZZ,0.125M	01121	3168330
R410	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R432	315-0821-00		RES,FXD,FILM:820 OHM,5Z,0.25M	19701	5043CX820R0J
R434	315-0821-00		RES,FXD,FILM:820 OHM,5Z,0.25M	19701	5043CX820R0J
R440	307-1223-00		RES NTWK,FXD,FI:8,10 OHM,ZZ,0.3M,16 DIP	TK1360	MDP1603-100G
R472	307-0649-00		RES NTWK,FXD,FI:8,33 OHM,ZZ,0.125M	01121	3168330
R477	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R478	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R479	315-0102-00		RES,FXD,FILM:1K OHM,5Z,0.25M	57668	NTR25JE01K0
R494	315-0102-00		RES,FXD,FILM:1K OHM,5Z,0.25M	57668	NTR25JE01K0
R496	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R520	315-0102-00		RES,FXD,FILM:1K OHM,5Z,0.25M	57668	NTR25JE01K0
R526	315-0101-00		RES,FXD,FILM:100 OHM,5Z,0.25M	57668	NTR25J-E 100E
R530	307-0383-00		RES NTWK,FXD,FI:13,4.7K OHM,ZZ,0.25M	03888	PD14L 4.7K GB
R532	315-0330-00		RES,FXD,FILM:33 OHM,5Z,0.25M	19701	5043CX33R00J
R534	315-0330-00		RES,FXD,FILM:33 OHM,5Z,0.25M	19701	5043CX33R00J
R540	307-0383-00		RES NTWK,FXD,FI:13,4.7K OHM,ZZ,0.25M	03888	PD14L 4.7K GB
R541	315-0132-00		RES,FXD,FILM:1.3K OHM,5Z,0.25M	57668	NTR25J-E01K3
R542	307-1223-00		RES NTWK,FXD,FI:8,10 OHM,ZZ,0.3M,16 DIP	TK1360	MDP1603-100G
R560	315-0472-00		RES,FXD,FILM:4.7K OHM,5Z,0.25M	57668	NTR25J-E04K7
R562	315-0330-00		RES,FXD,FILM:33 OHM,5Z,0.25M	19701	5043CX33R00J

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Component No.	Tektronix Part No.	Serial/Assembly No.		Name & Description	Mfr. Code	Mfr. Part No.
R564	315-0330-00			RES,FXD,FILM:33 OHM,5%,0.25M	19701	5043CX33R00J
R566	315-0821-00			RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
R610	315-0101-00			RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R612	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R614	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R616	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R618	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R630	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25M	57668	NTR25J-E150E
R632	315-0274-00			RES,FXD,FILM:270K OHM,5%,0.25M	57668	NTR25J-E270K
R634	315-0273-00			RES,FXD,FILM:27K OHM,5%,0.25M	57668	NTR25J-E27K0
R636	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R637	315-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.25M	57668	NTR25J-E02K2
R638	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R650	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25M	19701	5043CX15K00J
R652	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R654	315-0153-00			RES,FXD,FILM:15K OHM,5%,0.25M	19701	5043CX15K00J
R656	315-0102-00			RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R660	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R662	315-0471-00			RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R666	315-0151-00			RES,FXD,FILM:150 OHM,5%,0.25M	57668	NTR25J-E150E
R668	307-0383-00			RES NTNK,FXD,FI:13,4.7K OHM,2%,0.25M	03888	P014L 4.7K GB
R732	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25M	19701	5043CX120R0J
R734	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25M	19701	5043CX120R0J
R736	315-0121-00			RES,FXD,FILM:120 OHM,5%,0.25M	19701	5043CX120R0J
R760	315-0331-00			RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R866	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R888	315-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
S666	260-2111-00			SWITCH,PUSH:SPDT,MOMENTARY	59821	ORDER BY DESCR
S760	260-2111-00			SWITCH,PUSH:SPDT,MOMENTARY	59821	ORDER BY DESCR
U115	160-3412-00	B010100	B021601	MICROCKT,DGTL:CMOS,GATE ARRAY,3U MICRON,PRG M	TK1873	CKT137
U115	160-3909-00	B021602		MICROCKT,DGTL:CMOS,GATE ARRAY,1.5 MICRON,PR GM	80009	160-3909-00
U120	160-3412-00	B010100	B021601	MICROCKT,DGTL:CMOS,GATE ARRAY,3U MICRON,PRG M	TK1873	CKT137
U120	160-3909-00	B021602		MICROCKT,DGTL:CMOS,GATE ARRAY,1.5 MICRON,PR GM	80009	160-3909-00
U124	156-2093-00			MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U126	156-1756-00			MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U130	160-3389-01	B010100	B010866	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3389-01
U130	160-3389-02	B010867		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3389-02
U140	160-3387-01	B010100	B010866	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3387-01
U140	160-3387-02	B010867		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3387-02
U142	160-3385-01	B010100	B010866	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3385-01
U142	160-3385-02	B010867		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3385-02
U150	160-3383-01	B010100	B010866	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3383-01
U150	160-3383-02	B010867		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3383-02
U152	160-3381-01	B010100	B010866	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3381-01
U152	160-3381-02	B010867		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3381-02
U182	156-2094-00			MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04B3/J4
U190	156-0789-02			MICROCKT,DGTL:8 BIT SR,PRL LOAD,SCREENED	04713	SN74LS165J05
U220	156-0651-02			MICROCKT,DGTL:8-BIT PRL-OUT SER SHF RGTR	01295	SN74LS164NP3
U274	156-2319-00			MICROCKT,DGTL:QUADRUPE 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U280	156-1756-00	670-8523-43	MICROCKT,DGTL:DUAL 0-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/J4
U281	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U282	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U292	160-3373-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3373-00
U320	156-2091-00		MICROCKT,DGTL:QUAD 2-INP POS NAND GATES	01295	SN74ALS00N/J
U322	160-3374-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3374-00
U324	156-2111-00	8010100	MICROCKT,DGTL:OCTAL 0-TYPE LATCHES,SCRN	01295	SN74ALS373N3/J4
U330	160-3390-01		MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3390-01
U330	160-3390-02		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3390-02
U340	160-3388-01	8010100	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3388-01
U340	160-3388-02		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3388-02
U342	160-3386-01	8010100	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3386-01
U342	160-3386-02		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3386-02
U350	160-3384-01	8010100	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3384-01
U350	160-3384-02		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3384-02
U352	160-3382-01	8010100	MICROCKT,DGTL:32768 X 8 EPROM,NMOS,PRGM	80009	160-3382-01
U352	160-3382-02		MICROCKT,DGTL:NMOS,32768 X 8 EPROM,PRGM (PART OF 020-1415-XX)	80009	160-3382-02
U380	156-2296-00		MICROCKT,DGTL:NMOS,DYNAMIC RAM CONTROLLER	34649	8208
U382	156-2140-00		MICROCKT,DGTL:NMOS,2048 X 8 EPROM	34649	2817A-4
U390	156-1998-00	670-8523-40	MICROCKT,DGTL:TTL,OCTAL 0-TYPE FLIP-FLOP	01295	SN74ALS273
U392	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U410	156-1841-01		MICROCKT,DGTL:16 BIT MICROPROCESSOR,SCRN	34649	C80186
U410	156-1841-02		MICROCKT,DGTL:NMOS,MICROPROCESSOR,8MHZ	34649	A80186
U420	156-2178-00		MICROCKT,DGTL:TTL,QUAD 2 IN POS NAND BUFFER M/OPEN COLLECTOR OUTPUTS,SCRN	01295	SN74ALS38AN3/J4
U422	156-2093-00	670-8523-42	MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U424	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U430	156-2111-00		MICROCKT,DGTL:OCTAL 0-TYPE LATCHES,SCRN	01295	SN74ALS373N3/J4
U432	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS048N3/J4
U440	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U442	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U450	156-1570-01		MICROCKT,DGTL:PRGM PRPHL INTFC	34335	AM8255A-5 P/D CB
U460	156-0878-01	670-8523-41	MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
U462	156-1737-00		MICROCKT,DGTL:DUAL ASYNCHRONOUS RECEIVER/XMTR	18324	SCN2681AC1N40
U464	156-0879-01		MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
U490	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U492	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U510	156-2618-00		MICROCKT,DGTL:DUAL 4 LINE TO 1-LINE DATA	01295	SN74ALS352N3
U516	156-2092-00		MICROCKT,DGTL:QUADRUPL 2-INP POS NOR GATES	01295	SN74ALS02N3/J4
U522	156-2098-00		MICROCKT,DGTL:SYNCHRONOUS 4-BIT COUNTERS,SCR EENED	01295	SN74ALS161B3/J4
U526	156-1754-01	670-8523-41	MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U526	156-1740-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVER M ITH THREE-STATE OUTPUT,SCREENED	34335	AM29660CB
U528	156-1748-02	670-8523-41	MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U530	156-2111-00		MICROCKT,DGTL:OCTAL 0-TYPE LATCHES,SCRN	01295	SN74ALS373N3/J4
U540	156-0645-02		MICROCKT,DGTL:HEX INV ST NAND GATES	04713	SN74LS14NDS
U550	156-1756-00		MICROCKT,DGTL:DUAL 0-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/J4
U560	156-0878-01		MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
U564	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U570	156-2178-00		MICROCKT,DGTL:TTL,QUAD 2 IN POS NAND BUFFER M/OPEN COLLECTOR OUTPUTS,SCRN	01295	SN74ALS38AN3/J4
U572	156-1876-00	670-8523-41	MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
U574	156-1876-00		MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15
U580	156-1876-00		MICROCKT,DGTL:NMOS,65536 X 1 BIT DRAM	04713	MCM6665-AP-15

REPLACEABLE ELECTRICAL PARTS
TERMCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U582	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U584	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U590	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U592	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U594	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U610	156-2319-00		MICROCKT,DGTL:QUADRUPE 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3
U620	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS048N3/J4
U622	156-2076-00		MICROCKT,DGTL:SERIAL COMMUNICATION CONTROLL ER,SCRN	56708	Z8530A-00
U624	156-0878-01		MICROCKT,DGTL:QUAD LINE RCVR	04713	MC1489LDS
U630	156-2101-00		MICROCKT,DGTL:DUAL 4-INPUT POSITIVE NAND GA TES,SCREENED	01295	SN74ALS20AN3/J4
U654	156-0733-02		MICROCKT,DGTL:DUAL MONOSTABLE MV M/ST INP	01295	SN74LS22N3
U666	156-1080-01		MICROCKT,DGTL:HEX BUFFERS M/DC HV OUT,SCRN	01295	SN7407NP3
U670	156-0462-02		MICROCKT,DGTL:HEX INVERTER,SCREENED	01295	SN7414NP3
U672	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U674	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U680	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U682	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U684	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U690	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U692	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U694	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U720	156-2113-00		MICROCKT,DGTL:QUAD 2-INP PSOITIVE-AND GATE	01295	SN74ALS08N3/J4
U724	156-1315-00		MICROCKT,INTFC:LSTTL,QUAD DIFF RCVR	27014	DS26LS32NA+
U772	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U774	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U780	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U782	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U784	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U790	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U792	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U794	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U810	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS048N3/J4
U820	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U824	156-0879-01		MICROCKT,DGTL:QUAD LINE DRIVER	04713	MC1488LD
U830	156-1681-00		MICROCKT,DGTL:QUAD DIFFERENTIAL LINE DRIVER	34335	AM26LS310CB
U872	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U874	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U880	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U882	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U884	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U890	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U892	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
U894	156-1876-00		MICROCKT,DGTL:N MOS,65536 X 1 BIT DRAM	04713	MCN6665-AP-15
VR664	152-0279-00		SEMICOND DVC,DI:ZEN,SI,5.1V,5%,0.4M,DO-7	14552	TD3810989
M120	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M124	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M126	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M182	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M190	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M192	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M314	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M524	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
M668	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OWA 07
Y114	119-2196-00		OSC,XTAL CLOCK:5.0MHZ,0.01%	08111	M1290-5M
Y210	119-2061-00		OSCILLATOR,RF:CRYSTAL CLOCK,16MHZ,0.01%	01537	RASCO 1E 16MHZ

REPLACEABLE ELECTRICAL PARTS
TERMCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
Y450	119-1850-00		OSC,XTAL CLOCK:7.3728MHZ,0.01%	08111	M1200/A1824

REPLACEABLE ELECTRICAL PARTS
RAMOPT

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-8526-00		CIRCUIT BD ASSY:RAM OPTION	80009	670-8526-00
A	670-8526-01		CIRCUIT BD ASSY:RAM OPTION	80009	670-8526-01
C110	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C112	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C120	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C122	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C130	290-1021-00		CAP,FXD,ELCTLT:47UF,10VDC	56289	1730476X0010X
C132	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C210	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C212	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C220	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C222	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C240	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C310	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C312	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C320	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C322	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C330	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C332	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C340	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C342	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C410	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C412	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C420	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C422	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C430	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C432	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C440	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C442	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C510	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C512	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C520	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C522	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C530	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C532	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C540	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C542	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C610	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C612	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C614	290-1021-00		CAP,FXD,ELCTLT:47UF,10VDC	56289	1730476X0010X
C620	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C622	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C630	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C632	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C640	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
C642	281-0925-00		CAP,FXD,CER DI:0.22UF,20%,50V,AXIAL	96733	M5138Z224M
DS110	150-1036-00		LT EMITTING DIO:RED,650NM,40MA MAX	58361	Q6878/MV5074C
J49	131-2964-00		CONN,RCPT,ELEC:FEMALE,3 X 32,RTANG,0.1 CTR	TK1493	073-96914-390
R112	315-0821-00		RES,FXD,FILM:820 OHM,5%,0.25W	19701	5043CX820R0J
R130	307-0475-00		RES NTMK,FXD,FI:10K OHM,(15)RES,DIP	03888	P016L 10K68
R132	307-0475-00		RES NTMK,FXD,FI:10K OHM,(15)RES,DIP	03888	P016L 10K68
R142	307-0649-00		RES NTMK,FXD,FI:8.33 OHM,2%,0.125W	01121	3168330
R240	307-0649-00		RES NTMK,FXD,FI:8.33 OHM,2%,0.125W	01121	3168330
U110	160-3476-00		MICROCKT,DGTL:STTL ARRAY LOGIC,PRGM,SCRN	80009	160-3476-00
U112	156-0789-02		MICROCKT,DGTL:8 BIT SR,PRL LOAD,SCREENED	04713	SN74LS165JDS
U120	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4

REPLACEABLE ELECTRICAL PARTS
RAMOPT

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U122	156-2178-00		MICROCKT,DGTL:TTL,QUAD 2 IN POS NAND BUFFER M/OPEN COLLECTOR OUTPUTS,SCRN	01295	SN74ALS38AN3/J4
U132	156-2296-00		MICROCKT,DGTL:NMOS,DYNAMIC RAM CONTROLLER	34649	8208
U140	156-2091-00		MICROCKT,DGTL:QUAD 2-INP POS NAND GATES	01295	SN74ALS00N/J
U210	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U212	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U220	156-1998-00		MICROCKT,DGTL:TTL,OCTAL D-TYPE FLIP-FLOP	01295	SN74ALS273
U222	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04BN3/J4
U232	156-2093-00	670-8526-01	MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U310	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U312	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U320	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U322	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U330	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U332	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U340	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U342	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U410	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U412	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U420	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U422	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U430	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U432	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U440	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U442	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U510	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U512	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U520	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U522	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U530	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U532	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U540	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U542	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U610	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U612	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U620	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U622	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U630	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U632	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U640	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL
U642	156-2139-00		MICROCKT,DGTL:NMOS,262144 X 1 DRAM	01295	TMS4256-15NL

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-8524-40	8010100	8010152	CIRCUIT BD ASSY:DISPLAY CONTROLLER	80009	670-8524-40
A	670-8524-41	8010153	8010214	CIRCUIT BD ASSY:DISPLAY CONTROL	80009	670-8524-41
A	670-8524-42	8010215	8010329	CIRCUIT BD ASSY:DISPLAY CONTROL	80009	670-8524-42
A	670-8524-43	8010330	8010525	CIRCUIT BD ASSY:DISPLAY CONTROLLER	80009	670-8524-43
A	670-8524-45	8010526	8021104	CIRCUIT BD ASSY:DISPLAY CONTROLLER	80009	670-8524-45
A	670-8524-46	8021105	8021335	CIRCUIT BD ASSY:DISPLAY CONTROLLER	80009	670-8524-46
A	670-8524-47	8021336	8021500	CIRCUIT BD ASSY:DISPLAY CONTROLLER	80009	670-8524-47
A	670-8524-48	8021501		CIRCUIT BD ASSY:DISPLAY CONTROLLER (CONTAINS 670-8524-XX & 670-9181-XX)	80009	670-8524-48
C114	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C120	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C140	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C142	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C144	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C218	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C226	281-0913-00	670-8524-46		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C227	281-0913-00	670-8524-46		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C230	281-0913-00	670-8524-46		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C234	281-0913-00	670-8524-46		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C253	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C254	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C260	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C284	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C286	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C291	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C292	290-0745-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
C293	290-0745-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
C294	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C314	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C318	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C321	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C330	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C338	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C340	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C342	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C344	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C348	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C386	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C393	290-0745-00			CAP,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
C394	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C413	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C422	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C430	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C432	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C448	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C454	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C458	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C460	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C468	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C470	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C472	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C474	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C480	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C482	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C484	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C488	281-0913-00			CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C512	290-1121-00			CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C548	290-1121-00			CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
C554	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C558	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C560	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C562	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C564	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C568	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C570	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C572	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C574	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C578	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C580	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C592	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C596	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C614	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C618	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C620	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C622	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C624	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C628	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C630	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C632	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C634	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C638	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C640	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C642	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C644	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C654	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C658	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C660	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C662	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C668	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C670	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C672	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C674	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C678	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C680	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C682	281-0819-00	670-8524-40 670-8524-40	CAP, FXD, CER DI:33 PF, 5%, 50V	04222	GC105A330J
C682	281-0759-00	670-8524-41 670-8524-47	CAP, FXD, CER DI:22PF, 10%, 100V	04222	MA101A220KAA
C693	290-0745-00		CAP, FXD, ELCTLT:22UF, +50-10%, 25V	54473	ECE-A25V22L
C767	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C773	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C782	290-0745-00		CAP, FXD, ELCTLT:22UF, +50-10%, 25V	54473	ECE-A25V22L
C782	281-0819-00	670-8524-41	CAP, FXD, CER DI:33 PF, 5%, 50V	04222	GC105A330J
C783	281-0925-00	670-8524-41 670-8524-47	CAP, FXD, CER DI:0.22UF, 20%, 50V, AXIAL	96733	M5138Z224M
C784	281-0913-00	670-8524-41 670-8524-47	CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C787	281-0913-00	670-8524-48	CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C794	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C795	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C796	290-0524-00		CAP, FXD, ELCTLT:4.7UF, 20%, 10V	05397	T368A475M010A7
C813	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C815	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C819	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C821	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C823	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C827	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C829	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C831	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C833	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA
C837	281-0913-00		CAP, FXD, CER DI:0.1UF, 50V, AXIAL	04222	MA105E104ZAA

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
C839	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C841	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C843	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C854	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C858	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C860	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C861	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C864	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C866	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C870	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C871	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C872	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C873	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C876	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C880	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C882	281-0759-00	670-8524-40 670-8524-40	CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
CR682	152-0141-02	670-8524-48	SEMICONO DVC,DI:SM,SI,30V,150MA,30V	03508	DA2527 (1N4152)
CR781	152-0141-02	670-8524-41 670-8524-47	SEMICONO DVC,DI:SM,SI,30V,150MA,30V	03508	DA2527 (1N4152)
CR887	152-0141-02		SEMICONO DVC,DI:SM,SI,30V,150MA,30V	03508	DA2527 (1N4152)
J648	131-3506-00		CONN,RCPT,ELEC:HEADER,2 X 20,MALE,0.1 CTR	55322	TSN-120-15-G-D
J889	131-3360-00		CONN,RCPT,ELEC:HEADER,RTANG,20 PIN	53387	3592-6002
L681	108-0181-01	670-8524-40 670-8524-40	COIL,RF:FIXED,165MH	80009	108-0181-01
L681	108-0182-00	670-8524-41 670-8524-47	COIL,RF:FIXED,285MH	80009	108-0182-00
P35	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	96P-6043-0723-3
P39	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	96P-6043-0723-3
Q686	151-0482-00		TRANSISTOR:PMP,SI,T0-220	04713	SJE1977
Q783	151-0188-00	670-8524-41 670-8524-47	TRANSISTOR:PMP,SI,T0-92	80009	151-0188-00
Q786	151-0188-00	670-8524-48	TRANSISTOR:PMP,SI,T0-92	80009	151-0188-00
R112	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R132	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R136	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R165	307-0493-00		RES NTMK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R176	315-0330-00		RES,FXD,FILM:33 OHM,5%,0.25M	19701	5043CX33R00J
R178	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R222	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R230	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R259	307-0541-00		RES NTMK,FXD,FI:(7) 1K OHM,10%,1M	01121	108A102
R279	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R284	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R285	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R312	315-0102-00	670-8524-48	RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R331	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R332	307-0640-00		RES NTMK,FXD,FI:9.50 OHM,5%,0.125M	11236	750-101-R50
R362	307-0675-00		RES NTMK,FXD,FI:9.1K OHM,2%,1.25M	11236	750-101-R1K OHM
R379	307-0493-00		RES NTMK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R386	315-0470-00	670-8524-42 670-8524-47	RES,FXD,FILM:47 OHM,5%,0.25M	57668	NTR25J-E47E0
R387	315-0470-00	670-8524-45	RES,FXD,FILM:47 OHM,5%,0.25M	57668	NTR25J-E47E0
R395	315-0470-00	670-8524-48	RES,FXD,FILM:47 OHM,5%,0.25M	57668	NTR25J-E47E0
R414	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R418	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R421	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R423	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R443	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R444	307-0605-00		RES NTMK,FXD,FI:7.470 OHM,2%,0.15M,TC=250	11236	750-81-R470 OHMS
R452	307-0541-00		RES NTMK,FXD,FI:(7) 1K OHM,10%,1M	01121	108A102
R516	307-0828-00		RES NTMK,FXD,FI:4.33 OHM,2%,0.30M	32997	4308R-102-330
R561	307-0541-00		RES NTMK,FXD,FI:(7) 1K OHM,10%,1M	01121	108A102
R564	307-0493-00		RES NTMK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R576	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
R588	315-0390-00	670-8524-45	RES,FXD,FILM:39 OHM,5%,0.25M	57668	NTR25J-E39E0
R592	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R599	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R613	307-0640-00		RES NTWK,FXD,FI:9.50 OHM,5%,0.125M	11236	750-101-R50
R652	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R663	307-0828-00		RES NTWK,FXD,FI:4.33 OHM,Z%,0.30M	32997	4308R-102-330
R664	307-0828-00		RES NTWK,FXD,FI:4.33 OHM,Z%,0.30M	32997	4308R-102-330
R676	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R681	315-0512-00	670-8524-41 670-8524-47	RES,FXD,FILM:5.1K OHM,5%,0.25M	57668	NTR25J-E05K1
R681	315-0510-00	670-8524-48	RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R682	315-0472-00	670-8524-48	RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R698	311-1920-00		RES,VAR,NONWM:TRMR,500 OHM,10%,0.5 M	32997	3386C-T07-501
R716	307-0828-00		RES NTWK,FXD,FI:4.33 OHM,Z%,0.30M	32997	4308R-102-330
R752	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R762	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R765	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R769	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R771	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R775	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R778	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R779	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R781	315-0472-00	670-8524-40 670-8524-47	RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R782	315-0510-00	670-8524-40 670-8524-47	RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R788	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R789	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R793	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R796	321-0193-00		RES,FXD,FILM:1K OHM,1%,0.125M,TC=TO	19701	5033ED1K00F
R811	307-0828-00		RES NTWK,FXD,FI:4.33 OHM,Z%,0.30M	32997	4308R-102-330
R854	315-0111-00	670-8524-43	RES,FXD,FILM:110 OHM,5%,0.25M	57668	NTR25J-E110E
R855	315-0181-00	670-8524-43	RES,FXD,FILM:180 OHM,5%,0.25M	57668	NTR25J-E180E
R863	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R871	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R875	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R878	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R879	307-0493-00		RES NTWK,FXD,FI:(7) 50 OHM,5%,0.125M	11236	750-81-R50 OHM
R881	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R883	315-0510-00	670-8524-41 670-8524-47	RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R885	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R894	308-0441-00		RES,FXD,WM:3 OHM,5%,3M	14193	SA31-3R00J
R895	308-0441-00		RES,FXD,WM:3 OHM,5%,3M	14193	SA31-3R00J
U110	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U113	156-2169-00		MICROCKT,DGTL:SYNC 4 BIT UP/DOWN DECADE & BINARY COUNTER,SCRN	01295	SN74ALS169BN3
U122	156-2169-00		MICROCKT,DGTL:SYNC 4 BIT UP/DOWN DECADE & BINARY COUNTER,SCRN	01295	SN74ALS169BN3
U124	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U128	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U130	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U134	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS04BN3/J4
U138	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U140	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COUNTER,SCRN	01295	SN74AS869NT3
U142	160-3575-00		MICROCKT,DGTL:STTL,2048 X 8 PROM,PRGM (STANDARD KEYBOARD ONLY)	80009	160-3575-00
U142	160-3402-00		MICROCKT,DGTL:2048 X 8,STTL,PRGM (OPTION 4K ONLY) (NOT PART OF CIRCUIT BOARD)	80009	160-3402-00
U144	160-3367-00		MICROCKT,DGTL:STTL,2048 X 8 PROM PRGM	80009	160-3367-00
U148	156-2321-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT POSITIVE	01295	SN74AS08N3

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U152	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U154	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U160	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U164	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U168	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U170	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U172	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U174	156-2293-00		MICROCKT,DGTL:DUAL 2-LINE TO 4-LINE DECODER /MULTIPLEXER	01295	SN74ALS139N3/J4
U179	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U180	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U182	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U186	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U210	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U212	160-3378-00	670-8524-40 670-8524-43	MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3378-00
U212	160-3378-01	670-8524-44	MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3378-01
U214	160-3371-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3371-00
U218	156-2294-00		MICROCKT,DGTL:DUAL 4-BIT D-TYPE EDGE TRIGGE RED FLIP FLOP,SCRN	01295	SN74ALS874ANT3
U220	160-3375-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3375-00
U226	160-3411-00		MICROCKT,DGTL:CMOS,GATE ARRAY,3U MICRON,PRG M	TK1873	CKT125
U230	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U234	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U248	156-2166-00		MICROCKT,DGTL:HEX 2 INPUT NOR DRIVER,SCRN	01295	SN74AS8058N3
U254	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U258	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U260	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U264	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U268	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U270	156-2319-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3
U272	156-2319-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3
U274	156-1172-01		MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393NP3
U278	156-2321-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT POSITIVE	01295	SN74AS08N3
U280	156-2101-00		MICROCKT,DGTL:DUAL 4-INPUT POSITIVE NAND GA TES,SCREENED	01295	SN74ALS20AN3/J4
U282	156-2320-00		MICROCKT,DGTL:HEX INVERTING BUFFER M/OPEN C OLLECTOR OUTPUT,SCRN	01295	SN74ALS1005N3/J4
U286	160-3376-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3376-00
U310	156-2322-00		MICROCKT,DGTL:ARITHMETIC LOGIC UNIT/FUNCTIO N GENERATOR,SCRN	01295	SN74AS181ANT3
U314	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U318	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U320	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U322	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U324	156-2164-00		MICROCKT,DGTL:LSTTL,DUAL ONE OF FOUR DECODE R M/3 STATE OUT,SCRN	34335	AM25LS2539P3
U328	156-1858-00		MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U330	156-1858-00		MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)
U334	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U338	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U340	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U342	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U344	156-2318-00		MICROCKT,DGTL:DUAL 4-BIT D-TYPE EDGE TR,F/F	01295	SN74AS876NT3
U348	160-3372-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3372-00
U354	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U358	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U360	156-2063-00		MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374
U364	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U368	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	156-2292-00
U370	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	156-2292-00
U372	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	156-2292-00
U374	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	156-2292-00
U378	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U380	156-2294-00		MICROCKT,DGTL:DUAL 4-BIT D-TYPE EDGE TRIGGE RED FLIP FLOP,SCRN	01295	SN74ALS874ANT3
U382	156-2285-00		MICROCKT,DGTL:DUAL 4 BIT D-TYPE EDGE TRIGGE RED FLIP-FLOP,SCRN	01295	SN74ALS876NT
U386	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74AS832BN3/J4
U410	156-2096-00		MICROCKT,DGTL:OCTAL D-TYPE FLIP-FLOPS,SCRN	01295	SN74ALS175N3/J4
U413	156-2295-00		MICROCKT,DGTL:QUADRUPLE 1 OF 2 DATA SELECTO R/MULTIPLEXER,SCRN	01295	SN74AS158N3/J4
U416	156-2295-00		MICROCKT,DGTL:QUADRUPLE 1 OF 2 DATA SELECTO R/MULTIPLEXER,SCRN	01295	SN74AS158N3/J4
U420	156-2295-00		MICROCKT,DGTL:QUADRUPLE 1 OF 2 DATA SELECTO R/MULTIPLEXER,SCRN	01295	SN74AS158N3/J4
U422	156-2295-00		MICROCKT,DGTL:QUADRUPLE 1 OF 2 DATA SELECTO R/MULTIPLEXER,SCRN	01295	SN74AS158N3/J4
U424	156-2161-00		MICROCKT,DGTL:QUAD 2-1LINE SATA SEL/MLTPLXR	01295	SN74ALS158N3
U430	156-2161-00		MICROCKT,DGTL:QUAD 2-1LINE SATA SEL/MLTPLXR	01295	SN74ALS158N3
U432	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U434	156-1869-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS M/3-STATE OUT,SCRN	34335	AM29650CB
U438	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U440	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U442	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U448	156-2095-00	670-8524-41 670-8524-46	MICROCKT,DGTL:QUADRUPLE 2-INPUT EXCLUSIVE	01295	SN74ALS86N3/J4
U448	156-1800-00	670-8524-47	MICROCKT,DGTL:ASTTL,QUAD 2 INPUT EXCLUSIVE	18324	N74F86(NB OR JB)
U454	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U458	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U460	156-2063-00		MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374
U462	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U464	160-3369-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3369-00
U467	160-3368-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3368-00
U468	156-2063-00	670-8524-41 670-8524-43	MICROCKT,DGTL:8D-TYPE FLIP-FLOP	01295	SN74ALS374

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U468	156-1704-01	670-8524-45	MICROCKT,DGTL:OCTAL D-TYPE FF M/3-STATE OUT	80009	156-1704-01
U470	160-3377-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3377-00
U472	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U473	156-2285-00		MICROCKT,DGTL:DUAL 4 BIT D-TYPE EDGE TRIGGE RED FLIP-FLOP,SCRN	01295	SN74ALS876NT
U474	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U478	160-3370-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3370-00
U480	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U481	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U482	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U484	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U488	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U492	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U494	156-1754-01	670-8524-41 670-8524-45	MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U494	156-1740-00	670-8524-46	MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVER M ITH THREE-STATE OUTPUT,SCREENED	34335	AM29660CB
U512	156-1756-00	670-8524-48	MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U514	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74AS832BN3/J4
U518	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U520	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U522	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U524	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U528	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U530	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U532	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U534	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U538	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U540	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U542	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U544	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U554	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U558	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U560	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U562	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U568	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U570	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U572	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U574	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U578	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U580	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U584	156-2482-00		MICROCKT,DGTL:OCTAL BUFFER/LINE DRIVER M/3 STATE OUT,SCRN	96214	SN74AS240(N/J)
U588	156-2481-00		MICROCKT,DGTL:HEX 2-INPUT,NAND DRIVER,SCRN	01295	SN74ALS804N/J
U590	156-1617-00		MICROCKT,DGTL:HEX 2-INP NOR DRVR,SCRN	01295	SN74AS804AN
U592	156-2339-00		MICROCKT,DGTL:QUADRUPLE 2-INP POS-OR GATE	01295	SN74AS32N3
U596	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U612	156-2164-00		MICROCKT,DGTL:LSSTTL,DUAL ONE OF FOUR DECODE R M/3 STATE OUT,SCRN	34335	AM25LS2539P3
U614	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U618	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U620	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U624	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U628	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U630	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U632	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U634	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U638	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U640	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U642	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U644	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U654	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U658	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U660	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U662	156-2290-00		MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR,S CRN	04713	MC10H125PD
U668	156-2290-00		MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR,S CRN	04713	MC10H125PD
U670	156-0860-02		MICROCKT,DGTL:TRIPLE LINE RECEIVER	04713	MC10116PD/LD
U672	156-1642-01		MICROCKT,DGTL:SCREENED	04713	MC10H105LD
U674	156-1889-00		MICROCKT,DGTL:MECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PD
U678	156-0638-01		MICROCKT,DGTL:FOUR-BIT UNIV SHIFT RGTR	04713	MC10141(PDORLD)
U680	156-0205-02		MICROCKT,DGTL:QUAD 2 INP NOR GATE	04713	MC10102PD/LD
U712	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74ASB32BN3/J4
U714	156-1869-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS M/3-STATE OUT,SCRN	34335	AM29650CB
U718	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U720	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U722	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U724	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U728	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U730	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U732	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U734	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U738	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U740	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U742	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U744	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U754	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U758	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U760	156-2289-00		MICROCKT,DGTL:QUAD TTL-TO MECL TRANSLATOR	04713	MC10H124PD
U764	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U770	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U772	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U776	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U780	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U786	156-0205-02	670-8524-40 670-8524-47	MICROCKT,DGTL:QUAD 2 INP NOR GATE	04713	MC10102PD/LD
U792	156-2329-00		MICROCKT,LINEAR:ECL,4 BIT D/A CONVERTER,100 MHZ,VIDEO	24355	AD9702
U813	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U815	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U819	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U821	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U827	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U829	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U831	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U833	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U837	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U839	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U841	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U843	156-2330-00		MICROCKT,DGTL:NMOS,65536 X 1,DUSL PORT DRAM	01295	TMS4161-20NL
U854	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U858	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U860	156-2289-00		MICROCKT,DGTL:QUAD TTL-TO MECL TRANSLATOR	04713	MC10H124PD
U864	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U870	156-0543-01		MICROCKT,DGTL:HEX BUFFER	04713	MC10188PD/LD

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U872	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U876	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U880	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
VR886	152-0278-00		SEMICONO DVC,DI:ZEN,SI,3V,5%,0.4M,00-7	04713	SZG35009K20
M576	131-0566-00		BUS,COND:DUMMY RES,0.094 00 X 0.225L	24546	OMA 07
Y680	158-0284-00	670-8524-41 670-8524-47	XTAL UNIT,QTZ:67.659MHZ,SERIES	13075	158-0284-00
Y781	158-0284-00	670-8524-40 670-8524-40	XTAL UNIT,QTZ:67.659MHZ,SERIES	13075	158-0284-00
Y783	119-2362-00	670-8524-48	XTAL UNIT,QTZ:67.659MHZ	80009	119-2362-00

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-9725-00		CIRCUIT BD ASSY:DISPLAY CONTROL	80009	670-9725-00
C41	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C42	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C51	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C52	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C53	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C54	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C55	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C56	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C57	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C58	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C61	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C62	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C63	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C64	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C66	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C71	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C72	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C73	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C74	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C75	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C76	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C77	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C78	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C81	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C82	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C83	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C85	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C115	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C121	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C122	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C125	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C131	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C132	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C135	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C182	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C251	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C252	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C255	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C256	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C261	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C262	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C265	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C266	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C271	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C272	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C275	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C276	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C281	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C282	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C291	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C295	290-0745-00		CAP,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
C301	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C302	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C304	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C305	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C310	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
C311	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C312	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C315	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C321	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C325	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C326	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C331	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C332	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C335	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C341	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C342	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C444	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C465	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C491	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C511	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C515	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C522	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C541	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C551	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C552	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C553	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C555	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C556	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C557	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C561	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C562	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C563	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C564	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C571	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C572	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C575	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C576	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C581	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C582	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C583	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C585	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C601	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C611	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C616	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C621	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C625	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C626	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C635	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C641	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C642	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C655	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C656	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C661	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C662	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C665	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C666	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C671	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C672	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C675	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C676	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C681	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C683	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C685	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C705	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
C711	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C712	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C714	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C715	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C716	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C721	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C722	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C723	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C725	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C731	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C732	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C733	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C735	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C736	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C741	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C742	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C751	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C752	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C753	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C755	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C761	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C762	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C765	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C766	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C771	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C772	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C776	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C781	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C782	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C783	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C784	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
C785	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	WA105E104ZAA
CR165	152-0141-02		SEMICOND DVC,DI:5M,SI,30V,150MA,30V	03508	DA2527 (1N4152)
CR195	152-0141-02		SEMICOND DVC,DI:5M,SI,30V,150MA,30V	03508	DA2527 (1N4152)
CR295	152-0278-00		SEMICOND DVC,DI:2EN,SI,3V,5%,0.4M,DO-7	04713	SZG35009K20
J1	131-3739-00		CONN,RCPT,ELEC:CIRCUIT BOARD,BNC	80009	131-3739-00
J2	131-3739-00		CONN,RCPT,ELEC:CIRCUIT BOARD,BNC	80009	131-3739-00
J3	131-3739-00		CONN,RCPT,ELEC:CIRCUIT BOARD,BNC	80009	131-3739-00
J91	131-3784-00		CONN,RCPT,ELEC:MALE,2 X 3,0.025 SQ,M/3 TERM INATORS	80009	131-3784-00
J889	131-3360-00		CONN,RCPT,ELEC:HEADER,RTANG,20 PIN	53387	3592-6002
P35	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	96P-6043-0723-3
P39	131-2963-00		CONN,RCPT,ELEC:MALE,3 X 32,0.1 CTR	81312	96P-6043-0723-3
Q295	151-0188-00		TRANSISTOR:PNP,SI,T0-92	80009	151-0188-00
Q395	151-0482-00		TRANSISTOR:PNP,SI,T0-220	04713	SJE1977
R35	315-0111-00		RES,FXD,FILM:110 OHM,5%,0.25M	57668	NTR25J-E110E
R36	315-0111-00		RES,FXD,FILM:110 OHM,5%,0.25M	57668	NTR25J-E110E
R37	315-0111-00		RES,FXD,FILM:110 OHM,5%,0.25M	57668	NTR25J-E110E
R39	315-0151-00		RES,FXD,FILM:150 OHM,5%,0.25M	57668	NTR25J-E150E
R45	315-0151-00		RES,FXD,FILM:150 OHM,5%,0.25M	57668	NTR25J-E150E
R55	307-1321-00		RES NTKM,FXD,FI:82 OHM,2%,2.25M	80009	307-1321-00
R64	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R66	307-1321-00		RES NTKM,FXD,FI:82 OHM,2%,2.25M	80009	307-1321-00
R76	307-1321-00		RES NTKM,FXD,FI:82 OHM,2%,2.25M	80009	307-1321-00
R155	307-1321-00		RES NTKM,FXD,FI:82 OHM,2%,2.25M	80009	307-1321-00
R161	307-1321-00		RES NTKM,FXD,FI:82 OHM,2%,2.25M	80009	307-1321-00
R165	315-0472-00		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R166	315-0560-00		RES,FXD,FILM:56 OHM,5%,0.25M	57668	NTR25J-E56E0
R172	307-0393-00		RES NTKM,FXD,FI:13,100 OHM,2%,0.175M	01121	314A101

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
R181	307-1321-00		RES NTMK,FXD,FI:82 OHM,Z%,2.25M	80009	307-1321-00
R182	307-1321-00		RES NTMK,FXD,FI:82 OHM,Z%,2.25M	80009	307-1321-00
R192	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R195	311-1920-00		RES,VAR,NONMH:TRMR,500 OHM,10%,0.5 M	80009	311-1920-00
R251	307-1321-00		RES NTMK,FXD,FI:82 OHM,Z%,2.25M	80009	307-1321-00
R272	307-1321-00		RES NTMK,FXD,FI:82 OHM,Z%,2.25M	80009	307-1321-00
R282	307-0393-00		RES NTMK,FXD,FI:13,100 OHM,Z%,0.175M	01121	314A101
R292	321-0193-00		RES,FXD,FILM:1K OHM,1%,0.125M,TC=TO	19701	5033ED1K00F
R295	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R341	307-0649-00		RES NTMK,FXD,FI:8,33 OHM,Z%,0.125M	01121	3168330
R431	307-1321-00		RES NTMK,FXD,FI:82 OHM,Z%,2.25M	80009	307-1321-00
R441	307-0349-00		RES NTMK,FXD,FI:13,1K OHM,Z%,0.25M	03888	P014L-1K-G8
R485	315-0330-00		RES,FXD,FILM:33 OHM,5%,0.25M	19701	5043CX33R00J
R491	308-0441-00		RES,FXD,MM:3 OHM,5%,3M	14193	SA31-3R00J
R495	308-0441-00		RES,FXD,MM:3 OHM,5%,3M	14193	SA31-3R00J
R531	315-0471-00		RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R532	315-0390-00		RES,FXD,FILM:39 OHM,5%,0.25M	57668	NTR25J-E39ED
R541	315-0471-00		RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R542	315-0471-00		RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R543	315-0471-00		RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R544	315-0471-00		RES,FXD,FILM:470 OHM,5%,0.25M	57668	NTR25J-E470E
R576	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R601	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R602	315-0300-00		RES,FXD,FILM:30 OHM,5%,0.25M	19701	5043CX30R00J
R605	315-0470-00		RES,FXD,FILM:47 OHM,5%,0.25M	57668	NTR25J-E47ED
R641	307-0393-00		RES NTMK,FXD,FI:13,100 OHM,Z%,0.175M	01121	314A101
R642	307-0649-00		RES NTMK,FXD,FI:8,33 OHM,Z%,0.125M	01121	3168330
R682	307-0349-00		RES NTMK,FXD,FI:13,1K OHM,Z%,0.25M	03888	P014L-1K-G8
R741	307-0393-00		RES NTMK,FXD,FI:13,100 OHM,Z%,0.175M	01121	314A101
R775	307-0349-00		RES NTMK,FXD,FI:13,1K OHM,Z%,0.25M	03888	P014L-1K-G8
U21	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U22	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U25	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U31	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U32	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U35	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U41	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U42	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U51	156-2289-00		MICROCKT,DGTL:QUAD TTL-TO MECL TRANSLATOR	04713	MC10H124PD
U52	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U55	156-0543-01		MICROCKT,DGTL:HEX BUFFER	04713	MC10188PD/LD
U61	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U71	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U72	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U75	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U81	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U82	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U121	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U122	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U125	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U131	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U132	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U135	156-2602-00		MICROCKT,DGTL:N MOS,65536 X 4 DUAL PORT DRAM	TK0961	P041264-15
U141	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U142	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U151	156-2289-00		MICROCKT,DGTL:QUAD TTL-TO MECL TRANSLATOR	04713	MC10H124PD
U152	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U155	156-1700-01		MICROCKT,DGTL:ECL,16 X 4 SRAM	04713	MC10H145L
U162	156-1642-01		MICROCKT,DGTL:SCREENED	04713	MC10H105LD

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U166	156-1712-00		MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
U171	156-1642-01		MICROCKT,DGTL:SCREENED	04713	MC10H105LD
U175	156-2480-00		MICROCKT,DGTL:ECL,COMPARATOR,SCRN	04713	10H166LD
U176	156-2480-00		MICROCKT,DGTL:ECL,COMPARATOR,SCRN	04713	10H166LD
U185	156-2329-00		MICROCKT,LINEAR:ECL,4 BIT D/A CONVERTER,100 MHZ,VIDEO	24355	AD9702
U205	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U206	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U211	156-2322-00		MICROCKT,DGTL:ARITHMETIC LOGIC UNIT/FUNCTIO N GENERATOR,SCRN	01295	SN74AS181ANT3
U241	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U242	156-1961-00		MICROCKT,DGTL:BIDIRECT UNIVERSAL SHIFT REG	07263	74F194P
U251	156-2290-00		MICROCKT,DGTL:QUAD WECL TO TTL TRANSLATOR,S CRN	04713	MC10H125PD
U255	156-2290-00		MICROCKT,DGTL:QUAD WECL TO TTL TRANSLATOR,S CRN	04713	MC10H125PD
U256	156-1889-00		MICROCKT,DGTL:WECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PD
U261	156-0860-02		MICROCKT,DGTL:TRIPLE LINE RECEIVER	04713	MC10116PD/LD
U262	156-0205-02		MICROCKT,DGTL:QUAD 2 INP NOR GATE	04713	MC10102PD/LD
U271	156-0638-01		MICROCKT,DGTL:FOUR-BIT UNIV SHIFT RGTR	04713	MC10141(PDORLD)
U275	156-1889-00		MICROCKT,DGTL:WECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PD
U276	156-1889-00		MICROCKT,DGTL:WECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PD
U281	156-1889-00		MICROCKT,DGTL:WECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PD
U301	156-2494-00		MICROCKT,DGTL:QUADRUPL 1 OF 2 DATA SELECTO R/MULTIPLEXER M/3 STATE,INVERTED OUTPUTS,SC RN	96214	SN74AS258N
U305	156-2494-00		MICROCKT,DGTL:QUADRUPL 1 OF 2 DATA SELECTO R/MULTIPLEXER M/3 STATE,INVERTED OUTPUTS,SC RN	96214	SN74AS258N
U306	156-2494-00		MICROCKT,DGTL:QUADRUPL 1 OF 2 DATA SELECTO R/MULTIPLEXER M/3 STATE,INVERTED OUTPUTS,SC RN	96214	SN74AS258N
U311	156-2494-00		MICROCKT,DGTL:QUADRUPL 1 OF 2 DATA SELECTO R/MULTIPLEXER M/3 STATE,INVERTED OUTPUTS,SC RN	96214	SN74AS258N
U312	156-2113-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE-AND GATE	01295	SN74ALS08N3/J4
U315	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U316	156-2164-00		MICROCKT,DGTL:LSTTL,DUAL ONE OF FOUR DECODE R M/3 STATE OUT,SCRN	34335	AM25LS2539P3
U321	156-1869-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS M/3-STATE OUT,SCRN	34335	AM29650CB
U322	156-2161-00		MICROCKT,DGTL:QUAD 2-1LINE SATA SEL/MLTPLXR	01295	SN74ALS158N3
U325	156-2161-00		MICROCKT,DGTL:QUAD 2-1LINE SATA SEL/MLTPLXR	01295	SN74ALS158N3
U326	156-2096-00		MICROCKT,DGTL:OCTAL D-TYPE FLIP-FLOPS,SCRN	01295	SN74ALS175N3/J4
U331	156-2164-00		MICROCKT,DGTL:LSTTL,DUAL ONE OF FOUR DECODE R M/3 STATE OUT,SCRN	34335	AM25LS2539P3
U332	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74AS8328N3/J4
U335	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74AS8328N3/J4
U341	156-1869-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVERS M/3-STATE OUT,SCRN	34335	AM29650CB
U351	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U352	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U355	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U356	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U361	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U362	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U365	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U366	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U371	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD

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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U372	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U375	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U376	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U381	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U382	156-0316-04		MICROCKT,DGTL:QUAD ECL TO TTL TRANSLATOR	04713	MC10125PD/LD
U401	156-1664-00		MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
U405	156-1664-00		MICROCKT,DGTL:SCREENED	01295	SN74ALS574(NP3)
U406	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U411	156-1858-00		MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)
U412	156-1858-00		MICROCKT,DGTL:TRANSPARENT D-TYPE LATCHES	01295	SN74LS573(NP3)
U415	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U416	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U421	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U422	160-4198-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM	80009	160-4198-00
U425	160-4197-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM	80009	160-4197-00
U426	156-2285-00		MICROCKT,DGTL:DUAL 4 BIT D-TYPE EDGE TRIGGE RED FLIP-FLOP,SCRN	01295	SN74ALS876NT
U431	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U435	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U441	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U451	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U452	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U455	156-1753-00		MICROCKT,DGTL:OCTAL BUFFER & LINE DRIVER	01295	74ALS240NP3
U456	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U461	160-3370-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3370-00
U462	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U465	160-3377-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3377-00
U466	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U471	156-1273-01		MICROCKT,DGTL:8-BIT EQUAL TO COMPT	34335	25LS2521 PCB2
U472	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U475	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U476	156-2481-00		MICROCKT,DGTL:HEX 2-INPUT,NAND DRIVER,SCRN	01295	SN74ALS804N/J
U481	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U482	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U505	160-3411-00		MICROCKT,DGTL:CMOS,GATE ARRAY,3U MICRON,PRG M	TK1873	CKT125
U512	156-2294-00		MICROCKT,DGTL:DUAL 4-BIT D-TYPE EDGE TRIGGE RED FLIP FLOP,SCRN	01295	SN74ALS874ANT3
U516	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U521	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U522	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U525	156-2158-00		MICROCKT,DGTL:HEX 2 INPUT OR DRIVERS,SCRN	01295	SN74AS832BN3/J4
U526	156-2166-00		MICROCKT,DGTL:HEX 2 INPUT NOR DRIVER,SCRN	01295	SN74AS805BN3
U531	156-2338-00		MICROCKT,DGTL:DUAL D-TYPE POSITIVE	01295	SN74AS74NS/J4
U532	156-1800-00		MICROCKT,DGTL:ASTTL,QUAD 2 INPUT EXCLUSIVE	18324	N74F86(NB OR JB)
U535	160-3372-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3372-00
U551	156-2285-00		MICROCKT,DGTL:DUAL 4 BIT D-TYPE EDGE TRIGGE RED FLIP-FLOP,SCRN	01295	SN74ALS876NT
U552	156-2341-00		MICROCKT,DGTL:8-BIT LATCHES/REGISTER M/READ BACK,SCRN	50364	SN74LS794N SHRP
U555	160-3376-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3376-00
U556	156-2293-00		MICROCKT,DGTL:DUAL 2-LINE TO 4-LINE DECODER /MULTIPLEXER	01295	SN74ALS139N3/J4
U561	156-2319-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U562	156-2095-00		MICROCKT,DGTL:QUADRUPL 2-INPUT EXCLUSIVE	01295	SN74ALS86N3/J4
U565	156-2321-00		MICROCKT,DGTL:QUADRUPL 2-INPUT POSITIVE	01295	SN74AS08N3
U566	156-2320-00		MICROCKT,DGTL:HEX INVERTING BUFFER M/OPEN C OLLECTOR OUTPUT,SCRN	01295	SN74ALS1005N3/J4
U571	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U572	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U575	156-2100-00		MICROCKT,DGTL:3 TO 8 LINE DECODERS/DEMUX	01295	SN74ALS138N3/J4
U576	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U581	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U582	156-2101-00		MICROCKT,DGTL:DUAL 4-INPUT POSITIVE NAND GA TES,SCREENED	01295	SN74ALS20AN3/J4
U586	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U611	160-3378-01		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3378-01
U612	160-3371-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3371-00
U616	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U621	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U622	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U625	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U626	156-2291-00		MICROCKT,DGTL:SYNCHRONOUS,8 BIT UP/DOWN COU NTER,SCRN	01295	SN74AS869NT3
U631	156-1617-00		MICROCKT,DGTL:HEX 2-INP NOR DRVR,SCRN	01295	SN74AS804AN
U632	156-2294-00		MICROCKT,DGTL:DUAL 4-BIT D-TYPE EDGE TRIGGE RED FLIP FLOP,SCRN	01295	SN74ALS874ANT3
U635	156-2285-00		MICROCKT,DGTL:DUAL 4 BIT D-TYPE EDGE TRIGGE RED FLIP-FLOP,SCRN	01295	SN74ALS876NT
U651	160-3375-00		MICROCKT,DGTL:STTL,ARRAY LOGIC,PRGM,SCRN	80009	160-3375-00
U652	160-3367-00		MICROCKT,DGTL:STTL,2048 X 8 PROM PRGM	80009	160-3367-00
U655	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U656	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U661	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U662	156-2063-00		MICROCKT,DGTL:80-TYPE FLIP-FLOP	01295	SN74ALS374
U665	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	SN74ALS652
U666	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	SN74ALS652
U671	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	SN74ALS652
U672	156-2292-00		MICROCKT,DGTL:OCTAL BUS TRANSCEIVER AND REG ISTER,SCRN	01295	SN74ALS652
U675	156-1740-00		MICROCKT,DGTL:OCTAL DYNAMIC MEMORY DRIVER M ITH THREE-STATE OUTPUT,SCREENED	34335	AM29660CB
U676	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U681	156-1748-02		MICROCKT,DGTL:OCTAL BUS XCVR M/3-STATE OUT	01295	SN74ALS245AN3/J4
U682	156-2319-00		MICROCKT,DGTL:QUADRUPL 2-INPUT POSITIVE NA ND GATES,SCRN	01295	SN74AS00N3
U685	156-1172-01		MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393NP3
U711	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U712	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U715	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U716	156-1754-01		MICROCKT,DGTL:OCTAL BUFFER M/3-STATE OUT	01295	74ALS244A(N3/J4)
U721	156-1756-00		MICROCKT,DGTL:DUAL D-TYPE POS-EDGE-TRIG FF	01295	SN74ALS74NP3/JP4
U722	156-2169-00		MICROCKT,DGTL:SYNC 4 BIT UP/DOWN DECADE & B INARY COUNTER,SCRN	01295	SN74ALS169BN3
U725	156-2169-00		MICROCKT,DGTL:SYNC 4 BIT UP/DOWN DECADE & B INARY COUNTER,SCRN	01295	SN74ALS169BN3
U726	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U731	156-2339-00		MICROCKT,DGTL:QUADRUPL 2-INP POS-OR GATE	01295	SN74AS32N3

REPLACEABLE ELECTRICAL PARTS
DSPLCTL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
U732	156-2094-00		MICROCKT,DGTL:HEX INVERTERS	01295	SN74ALS048N3/J4
U735	156-2321-00		MICROCKT,DGTL:QUADRUPE 2-INPUT POSITIVE	01295	SN74AS08N3
U751	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U752	156-2179-00		MICROCKT,DGTL:TTL,HEX/QUAD D-TYPE FF M/CLR	01295	SN74ALS174N3/J4
U755	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U756	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U761	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U762	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U765	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U766	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U771	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U772	156-1694-00		MICROCKT,DGTL:4096 X 4 SRAM,DUAL IN LINE SC REENED	04713	MCM6168P-55
U776	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U781	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U782	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
U785	156-2182-00		MICROCKT,DGTL:TTL,QUAD 2 TO 1 LINE DATA SEL ECTOR/MUX,SCRN	01295	SN74ALS157N3/J4
Y265	119-2362-00		XTAL UNIT,QTZ:67.659MHZ	80009	119-2362-00

REPLACEABLE ELECTRICAL PARTS
CURSOR

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-9181-00		CIRCUIT BD ASSY:CROSS HAIR CURSOR	80009	670-9181-00
C10	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C11	290-1119-00		CAP,FXD,ELCTLT:47UF,20%,50V	55680	TLB1H470M
C14	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C16	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C20	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C21	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C22	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C24	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C26	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C110	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C112	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C113	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C114	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C115	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C116	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C117	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C120	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C122	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C124	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C125	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C126	290-1119-00		CAP,FXD,ELCTLT:47UF,20%,50V	55680	TLB1H470M
P30	131-3505-00		CONN,RCPT,ELEC:ECB,BOTTOM ENTRY,2 X 20,FEMA LE	55322	BSM-120-04-S-D
R14	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R22	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R24	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
R26	315-0241-00		RES,FXD,FILM:240 OHM,5%,0.25M	19701	5043CX240R0J
R110	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R111	315-0221-00		RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
R120	307-0393-00		RES NTWK,FXD,FI:13,100 OHM,2%,0.175M	01121	314A101
R126	307-0393-00		RES NTWK,FXD,FI:13,100 OHM,2%,0.175M	01121	314A101
R127	315-0510-00		RES,FXD,FILM:51 OHM,5%,0.25M	19701	5043CX51R00J
U10	156-2093-00		MICROCKT,DGTL:QUAD 2-INP POSITIVE OR GATE	01295	SN74ALS32N3/J4
U12	156-1273-01		MICROCKT,DGTL:8-BIT EQUAL TO COMPT	34335	25LS2521 PC82
U14	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U16	156-1855-00		MICROCKT,DGTL:STTL,BUS INTERFACE LATCHES	34335	AM298410C
U20	156-1889-00		MICROCKT,DGTL:MECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PO
U22	156-1889-00		MICROCKT,DGTL:MECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PO
U24	156-1889-00		MICROCKT,DGTL:MECL,UNIVERSAL HEXADECIMAL	04713	MC10H136 LD/PO
U26	156-1642-01		MICROCKT,DGTL:SCREENED	04713	MC10H105LD
U110	156-2095-00		MICROCKT,DGTL:QUADRUPLE 2-INPUT EXCLUSIVE	01295	SN74ALS86N3/J4
U112	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U114	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U116	156-0368-03		MICROCKT,DGTL:TTL TO ECL QUAD TRANSLATOR	04713	MC10124PD/LD
U122	156-2480-00		MICROCKT,DGTL:ECL,COMPARATOR,SCRN	04713	10H166LD
U124	156-2480-00		MICROCKT,DGTL:ECL,COMPARATOR,SCRN	04713	10H166LD

REPLACEABLE ELECTRICAL PARTS
VIDCONV

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A	670-9003-00		CIRCUIT BD ASSY:VIDEO CONVERTER	80009	670-9003-00
C101	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C121	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C122	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C123	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C131	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C141	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C151	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C152	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C161	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C171	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C172	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C173	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C181	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C201	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C221	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C231	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C241	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C261	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C271	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C341	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
C342	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C381	290-1121-00		CAP,FXD,ELCTLT:100UF,20%,35V	55680	ULB1V101M
C382	281-0913-00		CAP,FXD,CER DI:0.1UF,50V,AXIAL	04222	MA105E104ZAA
CR101	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR131	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
CR161	152-0141-02		SEMICON DVC,DI:SM,SI,30V,150MA,30V	03508	0A2527 (1N4152)
J51	131-3192-00		CONN,RCPT,ELEC:BNC,FEM,PC MOUNT	00779	227673-1
J52	131-3192-00		CONN,RCPT,ELEC:BNC,FEM,PC MOUNT	00779	227673-1
J53	131-3192-00		CONN,RCPT,ELEC:BNC,FEM,PC MOUNT	00779	227673-1
J61	131-3359-00		CONN,RCPT,ELEC:HEADER,RTANG,20 PIN	53387	3592-5002
P33	131-2601-00		CONN,RCPT,ELEC:CIRCUIT BD,1X10 CONTACT	22526	65780-010
P34	131-2631-00		CONN,RCPT,ELEC:CKT BD,1X4,0.1 CENTER	22526	65780-004
P36	131-2631-00		CONN,RCPT,ELEC:CKT BD,1X4,0.1 CENTER	22526	65780-004
P38	131-2631-00		CONN,RCPT,ELEC:CKT BD,1X4,0.1 CENTER	22526	65780-004
Q110	151-0220-00		TRANSISTOR:PMP,SI,TO-92	80009	151-0220-00
Q111	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
Q131	151-0220-00		TRANSISTOR:PMP,SI,TO-92	80009	151-0220-00
Q141	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
Q161	151-0220-00		TRANSISTOR:PMP,SI,TO-92	80009	151-0220-00
Q171	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
Q211	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
Q241	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
Q271	151-0720-00		TRANSISTOR:NPN,SI,TO-92	04713	SPS8232 (MPSH10)
R101	311-1237-00		RES,VAR,NONMM:1K OHM,10%,0.50M	32997	3386X-DY6-102
R102	321-0138-00		RES,FXD,FILM:267 OHM,1%,0.125M,TC=TO	07716	CEA0267R0F
R103	321-0104-00		RES,FXD,FILM:118 OHM,1%,0.125M,TC=TO	24546	NA55D1180F
R104	315-0221-00		RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
R111	321-0141-00		RES,FXD,FILM:287 OHM,1%,0.125M,TC=TO	19701	5033ED287R0F
R121	321-0082-00		RES,FXD,FILM:69.8 OHM,1%,0.125M,TC=TO	91637	CMF55116G69R80F
R122	321-0097-00		RES,FXD,FILM:100 OHM,1%,0.125M,TC=TO	91637	CMF55116G100R0F
R123	321-0185-00		RES,FXD,FILM:825 OHM,1%,0.125M,TC=TO	07716	CEA0825R0F
R131	321-0138-00		RES,FXD,FILM:267 OHM,1%,0.125M,TC=TO	07716	CEA0267R0F
R132	321-0104-00		RES,FXD,FILM:118 OHM,1%,0.125M,TC=TO	24546	NA55D1180F
R133	315-0221-00		RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-E220E
R134	321-0141-00		RES,FXD,FILM:287 OHM,1%,0.125M,TC=TO	19701	5033ED287R0F
R141	321-0082-00		RES,FXD,FILM:69.8 OHM,1%,0.125M,TC=TO	91637	CMF55116G69R80F

REPLACEABLE ELECTRICAL PARTS
VIDCONV

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
R142	321-0097-00		RES,FXD,FILM:100 OHM,1%,0.125M,TC=TO	91637	CMF55116G100R0F
R143	321-0185-00		RES,FXD,FILM:825 OHM,1%,0.125M,TC=TO	07716	CEA0825R0F
R161	321-0138-00		RES,FXD,FILM:267 OHM,1%,0.125M,TC=TO	07716	CEA0267R0F
R162	321-0104-00		RES,FXD,FILM:118 OHM,1%,0.125M,TC=TO	24546	NA5501180F
R163	315-0221-00		RES,FXD,FILM:220 OHM,5%,0.25M	57668	NTR25J-EZ20E
R164	321-0141-00		RES,FXD,FILM:287 OHM,1%,0.125M,TC=TO	19701	5033ED287R0F
R171	321-0082-00		RES,FXD,FILM:69.8 OHM,1%,0.125M,TC=TO	91637	CMF55116G69R80F
R172	321-0097-00		RES,FXD,FILM:100 OHM,1%,0.125M,TC=TO	91637	CMF55116G100R0F
R173	321-0185-00		RES,FXD,FILM:825 OHM,1%,0.125M,TC=TO	07716	CEA0825R0F
R181	315-0330-00		RES,FXD,FILM:33 OHM,5%,0.25M	19701	5043CX33R00J
R182	315-0330-00		RES,FXD,FILM:33 OHM,5%,0.25M	19701	5043CX33R00J
R201	311-1237-00		RES,VAR,NONMM:1K OHM,10%,0.50M	32997	3386X-DY6-102
R202	311-1237-00		RES,VAR,NONMM:1K OHM,10%,0.50M	32997	3386X-DY6-102
R203	315-0821-00		RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
R204	321-0056-00		RES,FXD,FILM:37.4 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G37R40F
R221	321-0131-00		RES,FXD,FILM:226 OHM,1%,0.125M,TC=TO	19701	5043ED226R0F
R222	321-0107-00		RES,FXD,FILM:127 OHM,1%,0.125M,TC=TO	07716	CEA0127R0F
R231	315-0821-00		RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
R232	321-0056-00		RES,FXD,FILM:37.4 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G37R40F
R242	321-0131-00		RES,FXD,FILM:226 OHM,1%,0.125M,TC=TO	19701	5043ED226R0F
R243	321-0107-00		RES,FXD,FILM:127 OHM,1%,0.125M,TC=TO	07716	CEA0127R0F
R261	315-0821-00		RES,FXD,FILM:820 OHM,5%,0.25M	19701	5043CX820R0J
R262	321-0056-00		RES,FXD,FILM:37.4 OHM,0.5%,0.125M,TC=TO	91637	CMF55116G37R40F
R271	321-0131-00		RES,FXD,FILM:226 OHM,1%,0.125M,TC=TO	19701	5043ED226R0F
R272	321-0107-00		RES,FXD,FILM:127 OHM,1%,0.125M,TC=TO	07716	CEA0127R0F
U121	156-1984-00		MICROCKT,LINEAR:VIDEO BUFFER	34371	HA-5033
U151	156-1984-00		MICROCKT,LINEAR:VIDEO BUFFER	34371	HA-5033
U171	156-1984-00		MICROCKT,LINEAR:VIDEO BUFFER	34371	HA-5033
U181	156-2500-00		MICROCKT,DGTL:HEX DRIVERS	01295	SN74AS1034N

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Discont	Name & Description	Mfr. Code	Mfr. Part No.
A	119-3800-00	8010100	8010652	POWER SUPPLY: (4111 ONLY)	54407	SP556
A	119-3800-01	8010653		POWER SUPPLY: (4111,CX4111)	80009	119-3800-01
C1	118-4734-00			CAP FXD, PLASTIC:0.47UF, 250V	54407	106-21350
C2	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C3	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C4	118-4734-00			CAP FXD, PLASTIC:0.47UF, 250V	54407	106-21350
C5	118-4735-00			CAP, FXD, ELCTLT:470UF, 200V	54407	101-21323
C6	118-4735-00			CAP, FXD, ELCTLT:470UF, 200V	54407	101-21323
C7	118-4881-00			CAP, FXD, ELCTLT:0.01UF, 100V, 5%	54407	104-21016
C8	283-0059-00			CAP, FXD, CER DI:1UF, +80-20%, 50V	31433	C330C105M5R5CA
C9	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C10	283-0003-00			CAP, FXD, CER DI:0.01UF, +80-20%, 150V	59821	0103740Z5UJDCX
C11	283-0008-00			CAP, FXD, CER DI:0.1UF, 20%, 500V	51642	500-500-X7R-104M
C12	283-0059-00			CAP, FXD, CER DI:1UF, +80-20%, 50V	31433	C330C105M5R5CA
C13	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C14	118-4882-00			CAP, FXD, ELCTLT:680PF, 1KV	54407	105-20922
C15	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C16	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C17	283-0065-00			CAP, FXD, CER DI:0.001UF, 5%, 100V	59660	0835-591Y5E0102J
C18	118-4883-00			CAP, FXD, ELCTLT:330UF, 35V	54407	101-21418
C19	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C20	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C21	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C22	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C23	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C24	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C25	283-0211-00			CAP, FXD, CER DI:0.1UF, 10%, 200V	04222	SR406C104KAA
C26	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C27	290-0891-00			CAP, FXD, ELCTLT:1UF, +75 -10%, 50V	55680	ULA1H010TEA
C28	283-0024-00			CAP, FXD, CER DI:0.1UF, +80-20%, 50V	04222	SR215C104MAA
C29	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C30	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C31	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C32	283-0594-00			CAP, FXD, MICA DI:0.001UF, 1%, 100V	00853	D151F102F0
C33	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C34	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C35	118-4883-00			CAP, FXD, ELCTLT:330UF, 35V	54407	101-21418
C36	118-4884-00			CAP, FXD, ELCTLT:1000UF, 10V	54407	101-21417
C37	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C39	118-4880-00			CAP, FXD, ELCTLT:0.1UF, 250V	54407	106-21348
C40	283-0594-00			CAP, FXD, MICA DI:0.001UF, 1%, 100V	00853	D151F102F0
C41	285-1236-00			CAP, FXD, PLASTIC:0.022UF, 20%, 400V	14752	23001E223M
C42	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C43	285-1245-00			CAP, FXD, PLASTIC:0.01UF, 10%, 400V	55112	171/.01/K/400/C
C44	283-0032-00			CAP, FXD, CER DI:470PF, 5%, 500V	59660	831-000-Z5E0471J
C46	118-4734-00			CAP FXD, PLASTIC:0.47UF, 250V	54407	106-21350
C47	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C48	118-4886-00			CAPACITOR:0.0047UF, 250V	54407	106-22145
C49	118-4734-00			CAP FXD, PLASTIC:0.47UF, 250V	54407	106-21350
C51	118-4734-00			CAP FXD, PLASTIC:0.47UF, 250V	54407	106-21350
CR1	118-4733-00			SEMICON DVC, DI:4A, 600V	54407	140-20056
CR1	151-0503-00			SCR:SI, TO-92 (SCR1 IN CIRCUITRY)	04713	SCR5138
CR2	152-0066-00			SEMICON DVC, DI:RECT, SI, 400V, 1A, DO-41	05828	GP10G-020
CR3	152-0066-00			SEMICON DVC, DI:RECT, SI, 400V, 1A, DO-41	05828	GP10G-020
CR4	152-0066-00			SEMICON DVC, DI:RECT, SI, 400V, 1A, DO-41	05828	GP10G-020

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
CR5	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR6	118-4877-00		SEMICON DVC,DI:1A,850V	54407	111-21337
CR7	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR8	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR9	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR10	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR11	118-4877-00		SEMICON DVC,DI:1A,850V	54407	111-21337
CR12	118-4878-00		SEMICON DVC,DI:1A,200V	54407	111-21314
CR13	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR14	118-4877-00		SEMICON DVC,DI:1A,850V	54407	111-21337
CR15	118-4878-00		SEMICON DVC,DI:1A,200V	54407	111-21314
CR16	118-4867-00		SEMICON DVC,DI:3A,850V	54407	111-21388
CR18	152-0827-00		SEMICON DVC,DI:RECT,SI,45V,3A	04713	MBR2545CT
CR19	152-0827-00		SEMICON DVC,DI:RECT,SI,45V,3A	04713	MBR2545CT
CR20	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR21	118-4879-00		SEMICON DVC,DI:3A,200V	54407	111-21305
CR22	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR23	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR24	152-0395-00		SEMICON DVC,DI:ZEN,SI,4.3V,5%,0.4M	04713	SZG35009K18
CR25	152-0280-00		SEMICON DVC,DI:ZEN,SI,6.2V,5%,0.4M,DO-7	04713	1N753A
CR26	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR27	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR28	118-4879-00		SEMICON DVC,DI:3A,200V	54407	111-21305
CR29	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR30	152-0175-00		SEMICON DVC,DI:ZEN,SI,5.6V,5%,0.4M,DO-7	14552	TD3810976
CR31	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR32	118-4876-00		SEMICON DVC,DI:0.2A,100V	54407	111-20058
CR33	152-0066-00		SEMICON DVC,DI:RECT,SI,400V,1A,DO-41	05828	GP10G-020
CR34	152-0827-00		SEMICON DVC,DI:RECT,SI,45V,3A	04713	MBR2545CT
DS1	150-0030-00		LAMP,GLOW:60-90V MAX,0.7MA,A28-T,WIRE LEADS	58224	A28-T
F1	118-4973-00	119-3800-00	FUSE:6A,250V SLOW BLOW,M/SOLDER TAILS	80009	118-4973-00
F1	118-5219-00	119-3800-01	FUSE,CARTRIDGE:6A,250V,MED BLOW	80009	118-5219-00
J1	131-3089-00		CONN,RCPT,ELEC:HEADER,3 X 1,0.175 SPACING	00779	350789-1(MAT-N-L
J2	131-1737-00		CONN,RCPT,ELEC:CKT BD,9 CONTACTS,M/LOCKING EARS	00779	350712-1
J5	118-4885-00		CONN,RCPT,ELEC:1 X 2,0.100 SPACING	80009	118-4885-00
L1	118-4728-00		INDUCTOR:EMI	80009	118-4728-00
L2	118-4729-00		INDUCTOR:	54407	082-75005
L3	118-4729-00		INDUCTOR:	54407	082-75005
L4	118-4869-00		INDUCTOR:OUTPUT	54407	082-75819
L5	118-4873-00		INDUCTOR:EMI 082-76222 POWER ONE	54407	082-76222
L6	118-4728-00		INDUCTOR:EMI	80009	118-4728-00
P1	118-4736-00		CONN,RCPT,ELEC:AC LINE M/WIRE	54407	901-22239
Q1	118-4875-00		TRANSISTOR:PMP,60V	54407	172-10248
Q2	151-0426-00		TRANSISTOR:NPN,SI,T0-220	03508	X44HR242
Q3	151-0728-00		TRANSISTOR:NPN,SI,T0-202	04713	S05363
Q4	151-0625-00		TRANSISTOR:PMP,SI,T0-220	03508	D45H11
Q5	151-0679-00		TRANSISTOR:NPN,SI,T0-220	04713	MJE13009
Q6	118-4875-00		TRANSISTOR:PMP,60V	54407	172-10248
Q7	118-4739-00		TRANSISTOR:TIP 100,40V,8A,NPN	54407	172-21504-2
Q8	151-0302-00		TRANSISTOR:NPN,SI,T0-18	04713	ST899
Q9	118-4875-00		TRANSISTOR:PMP,60V	54407	172-10248
Q10	151-0302-00		TRANSISTOR:NPN,SI,T0-18	04713	ST899
R1	315-0106-00		RES,FXD,FILM:10M OHM,5%,0.25W	01121	CB1065
R2	301-0823-00		RES,FXD,FILM:82K OHM,5%,0.5W	19701	5053CX82K00J
R3	301-0823-00		RES,FXD,FILM:82K OHM,5%,0.5W	19701	5053CX82K00J
R4	315-0153-00		RES,FXD,FILM:15K OHM,5%,0.25W	19701	5043CX15K00J
R5	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25W	57668	NTR25JE01K0
R6	301-0101-00		RES,FXD,FILM:100 OHM,5%,0.5W	19701	5053CX100R0J

REPLACEABLE ELECTRICAL PARTS
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Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
R7	322-0210-00		RES,FXD,FILM:1.50K OHM,1%,0.25M,TC=TO	75042	CEBT0-1501F
R8	315-0100-00		RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
R9	315-0472-00		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R10	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R11	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R12	315-0220-00		RES,FXD,FILM:22 OHM,5%,0.25M	19701	5043CX22R00J
R13	118-4868-00		RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
R14	118-4868-00		RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
R15	118-4737-00		RES,FXD,FILM:0.5 OHM,5%,0.25M	54407	150-20292
R16	118-4737-00		RES,FXD,FILM:0.5 OHM,5%,0.25M	54407	150-20292
R17	118-4737-00		RES,FXD,FILM:0.5 OHM,5%,0.25M	54407	150-20292
R18	315-0100-00		RES,FXD,FILM:10 OHM,5%,0.25M	19701	5043CX10RR00J
R19	118-4737-00		RES,FXD,FILM:0.5 OHM,5%,0.25M	54407	150-20292
R20	118-4738-00		RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
R21	301-0331-00		RES,FXD,FILM:330 OHM,5%,0.5M	19701	5053CX330R0J
R22	301-0102-00		RES,FXD,FILM:1K OHM,5%,0.50M	19701	5053CX1K000J
R23	315-0432-00		RES,FXD,FILM:4.3K OHM,5%,0.25M	57668	NTR25J-E04K3
R24	315-0331-00		RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R25	315-0331-00		RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R26	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R27	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R28	118-4874-00		RES,FXD,FILM:0.12 OHM,2M,5%	54407	158-10077
R29	315-0511-00		RES,FXD,FILM:510 OHM,5%,0.25M	19701	5043CX510R0J
R30	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R31	315-0331-00		RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R32	118-4730-00		RES,FXD,FILM:100 OHM,2M,5%	54407	165-20799
R33	315-0472-00		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
R34	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R35	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R36	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R37	118-4874-00		RES,FXD,FILM:0.12 OHM,2M,5%	54407	158-10077
R38	311-1466-00		RES,VAR,NONMM:TRMR,2K OHM,0.5M	32997	3386F-T04-202
R39	315-0202-00		RES,FXD,FILM:2K OHM,5%,0.25M	57668	NTR25J-E 2K
R40	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R41	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R42	315-0331-00		RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R43	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R44	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R45	118-4868-00		RES,FXD,FILM:3.9K,5%,2M	54407	165-21193
R46	315-0122-00		RES,FXD,FILM:1.2K OHM,5%,0.25M	57668	NTR25J-E01K2
R47	315-0153-00		RES,FXD,FILM:15K OHM,5%,0.25M	19701	5043CX15K00J
R48	315-0302-00		RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
R49	311-1466-00		RES,VAR,NONMM:TRMR,2K OHM,0.5M	32997	3386F-T04-202
R51	315-0302-00		RES,FXD,FILM:3K OHM,5%,0.25M	57668	NTR25J-E03K0
R53	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R56	118-4738-00		RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
R57	315-0102-00		RES,FXD,FILM:1K OHM,5%,0.25M	57668	NTR25JE01K0
R58	118-4738-00		RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
R59	301-0220-00		RES,FXD,FILM:22 OHM,5%,0.5M	19701	5053CX22R00J
R60	301-0204-00		RES,FXD,FILM:200K OHM,5%,0.5M	19701	5053CX200K0J
R61	118-4738-00		RES,FXD,FILM:22 OHM,2M,5%	54407	165-20804
R62	315-0183-00		RES,FXD,FILM:18K OHM,5%,0.25M	19701	5043CX18K00J
R63	315-0331-00		RES,FXD,FILM:330 OHM,5%,0.25M	57668	NTR25J-E330E
R64	315-0101-00		RES,FXD,FILM:100 OHM,5%,0.25M	57668	NTR25J-E 100E
R65	315-0472-00		RES,FXD,FILM:4.7K OHM,5%,0.25M	57668	NTR25J-E04K7
RT1	118-4731-00		RES,THERMAL:10 OHM,2A	54407	159-20811
SC1	-----		(SEE CR1)		
SM1	260-2259-00		SWITCH,PUSH:DPST,5A,250V	31918	N30X 2A
SM2	260-2116-00		SWITCH,SLIDE:DPOT,10A,125VAC,LINE SEL	22753	SE1022SCCEPRHKRA

REPLACEABLE ELECTRICAL PARTS
PWRSUPL

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
SM3	118-4887-00		SWITCH,PUSH:MOMENTARY,4A	54407	909-22227
SM4	260-2116-00		SWITCH,SLIDE:DPDT,10A,125VAC,LINE SEL	22753	SE1022SCCEPRHKRA
T1	118-4727-00		TRANSFORMER:OUTPUT	54407	082-75896
U1	156-0853-00		MICROCKT,LINEAR:OPNL AMPL,DUAL	04713	LM358N
U2	156-0071-00		MICROCKT,LINEAR:VOLTAGE REGULATOR	04713	MC1723CL
U3	156-1631-00		MICROCKT,LINEAR:ADJUSTABLE SHUNT REGULATOR	01295	TL431C-LP
VR1	118-4732-00		RES,V SENSITIVE:510K,275V	54407	164-21380

REPLACEABLE ELECTRICAL PARTS

Component No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Name & Description	Mfr. Code	Mfr. Part No.
CHASSIS PARTS					
B1001 FL5003	119-3801-00 131-3371-00		FAN,TUBEAXIAL:12 VDC,3.6M,57 CEM CONN,RCPT,ELEC:D-SUBMIN,9 PIN,830PS	TK1504 13511	MS47121 FCC17E9AD-240



Section 9

DIAGRAMS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μ F).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

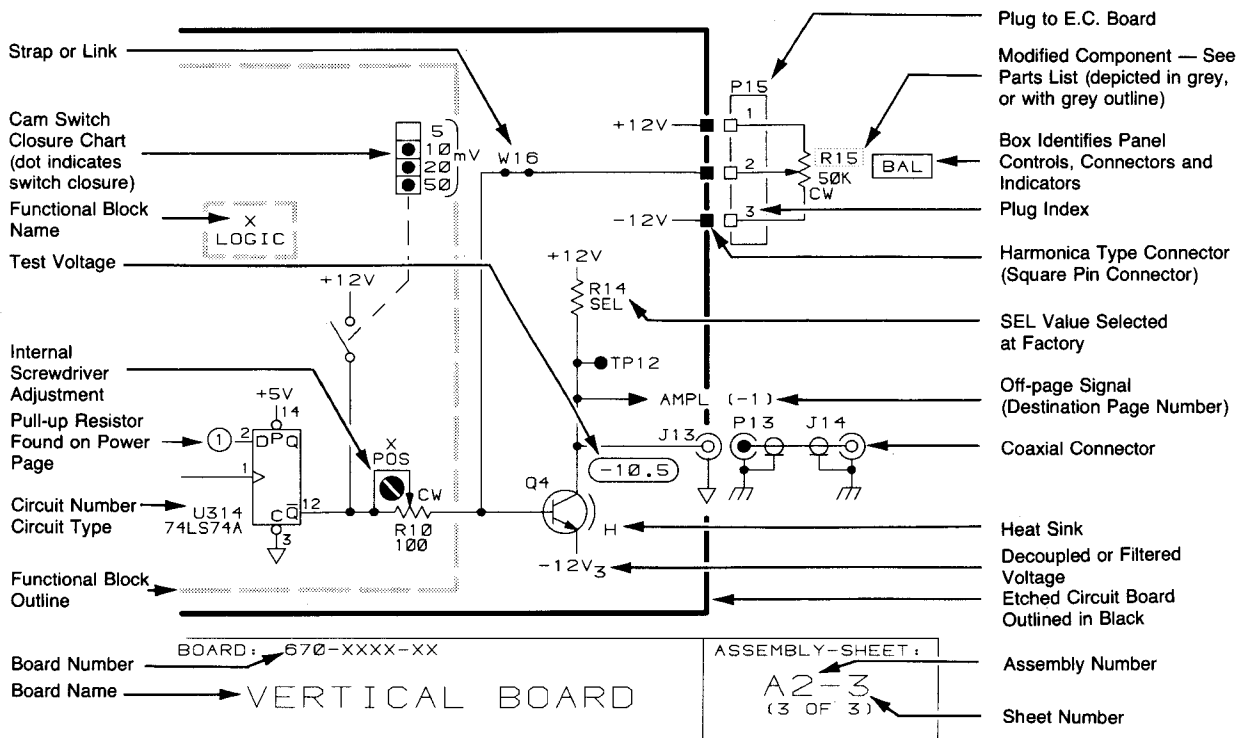
Abbreviations are based on ANSI Y1.1-1972. Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc., are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc.)	H	Heat dissipating device (heat sink, heat radiator, etc.)	S	Switch or contactor
AT	Attenuator, fixed or variable	HR	Heater	T	Transformer
B	Motor	HY	Hybrid circuit	TC	Thermocouple
BT	Battery	J	Connector, stationary portion	TP	Test point
C	Capacitor, fixed or variable	K	Relay	U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
CB	Circuit breaker	L	Inductor, fixed or variable	V	Electron tube
CR	Diode, signal or rectifier	M	Meter	VR	Voltage regulator (zener diode, etc.)
DL	Delay line	P	Connector, movable portion	W	Wirestrap or cable
DS	Indicating device (lamp)	Q	Transistor or silicon-controlled rectifier	Y	Crystal
E	Spark Gap, Ferrite bead	R	Resistor, fixed or variable	Z	Phase shifter
F	Fuse	RT	Thermistor		
FL	Filter				

The following special symbols may appear on the diagrams:



DIAGRAMS

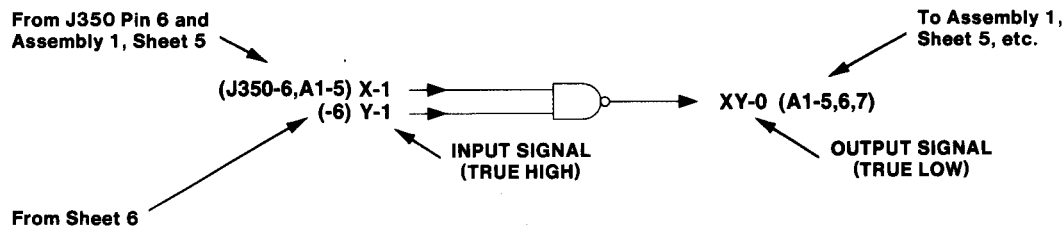
1. True High and True Low Signals

Signal names on the schematics are followed by -1 or a -0. A TRUE HIGH signal is indicated by -1, and a TRUE LOW signal is indicated by -0.

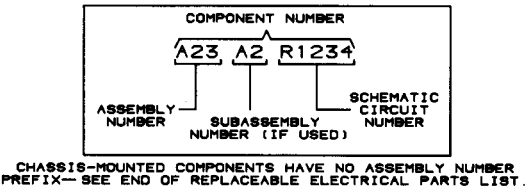
SIGNAL -1 = TRUE HIGH
SIGNAL -0 = TRUE LOW

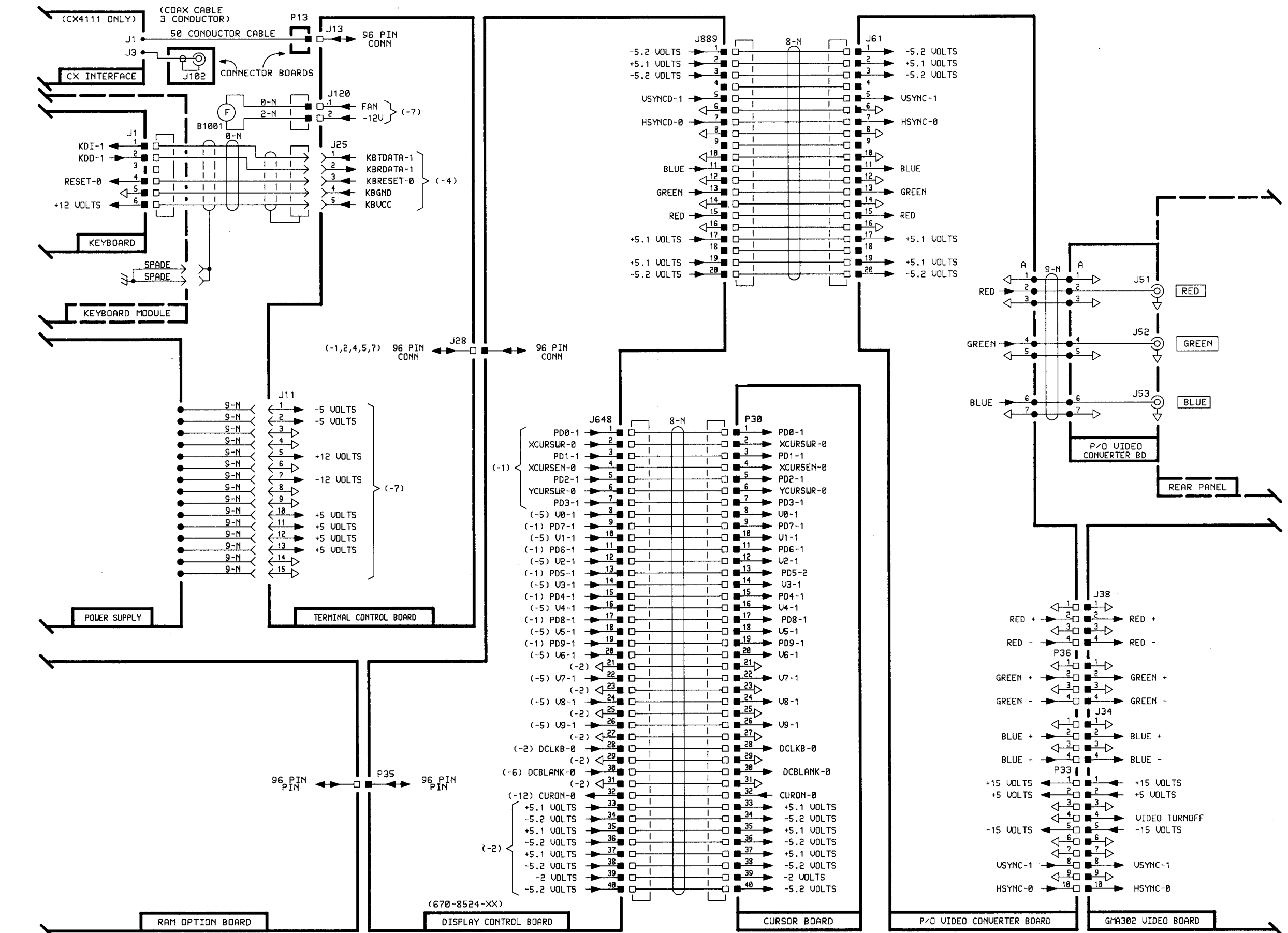
2. Cross-References

Schematic cross-references (from/to information) are included on the schematics. The "from" reference only indicates the signal "source," and the "to" reference lists all loads where the signal is used. All from/to information will be enclosed in parentheses.

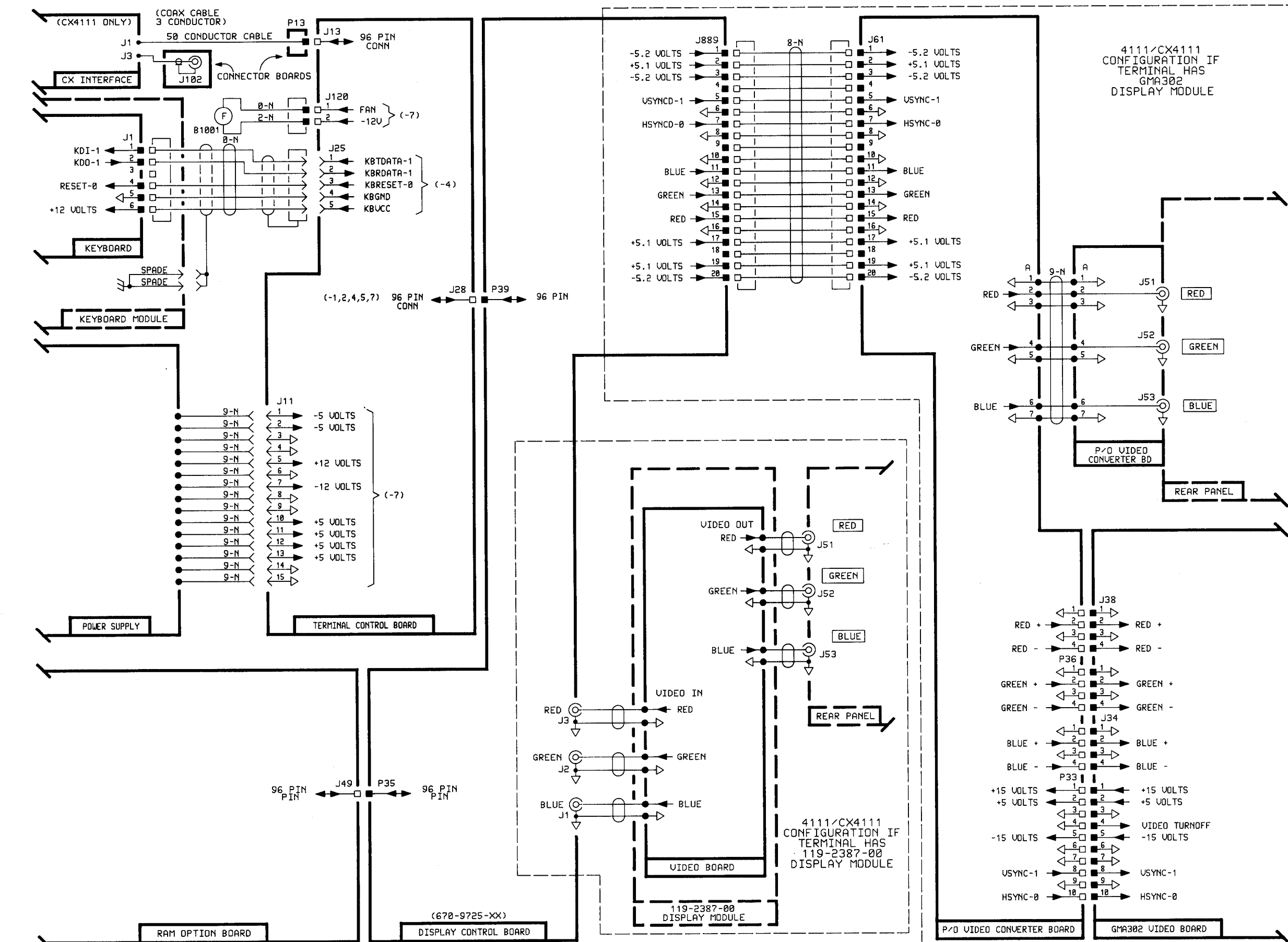


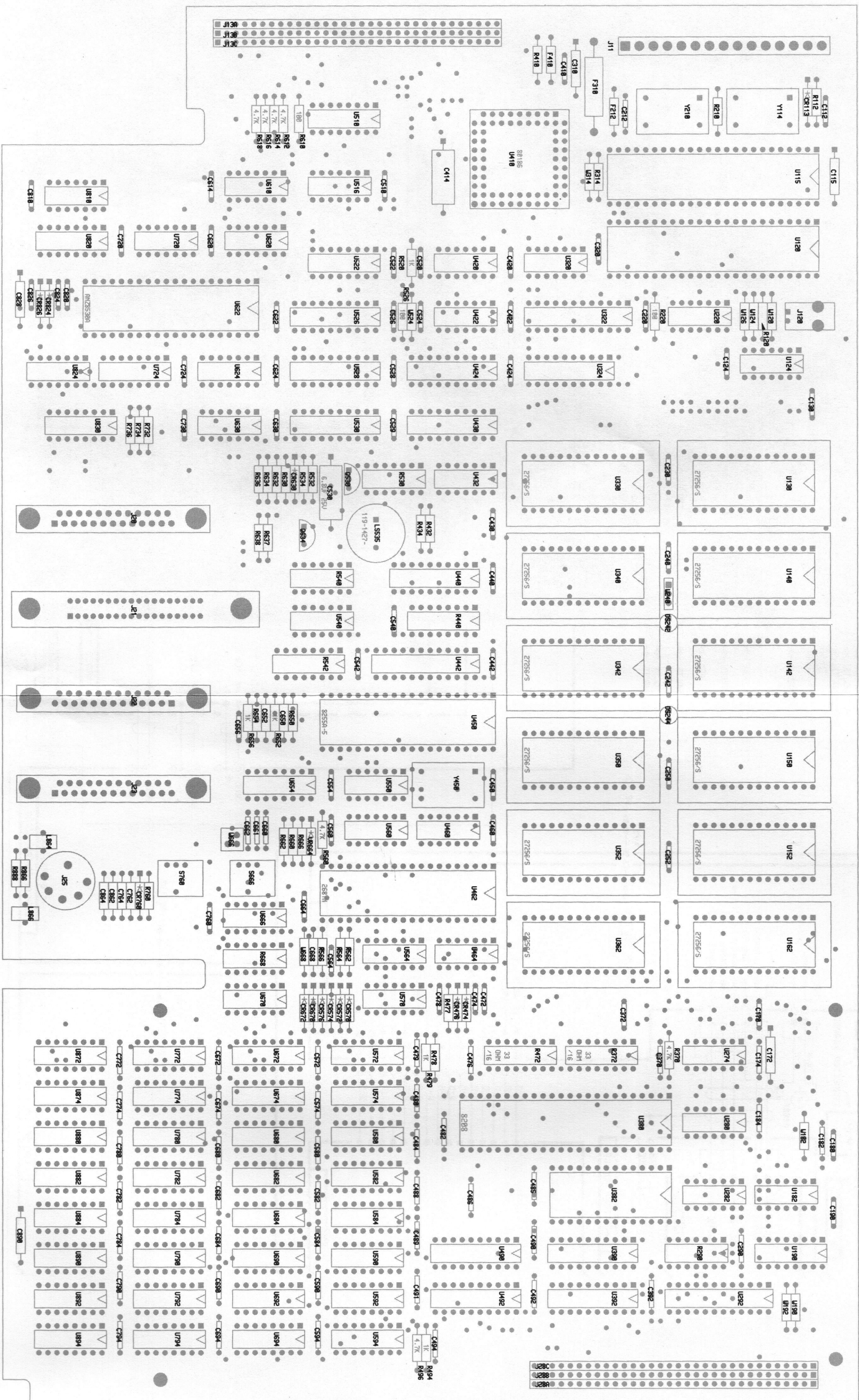
3. Component Number Example



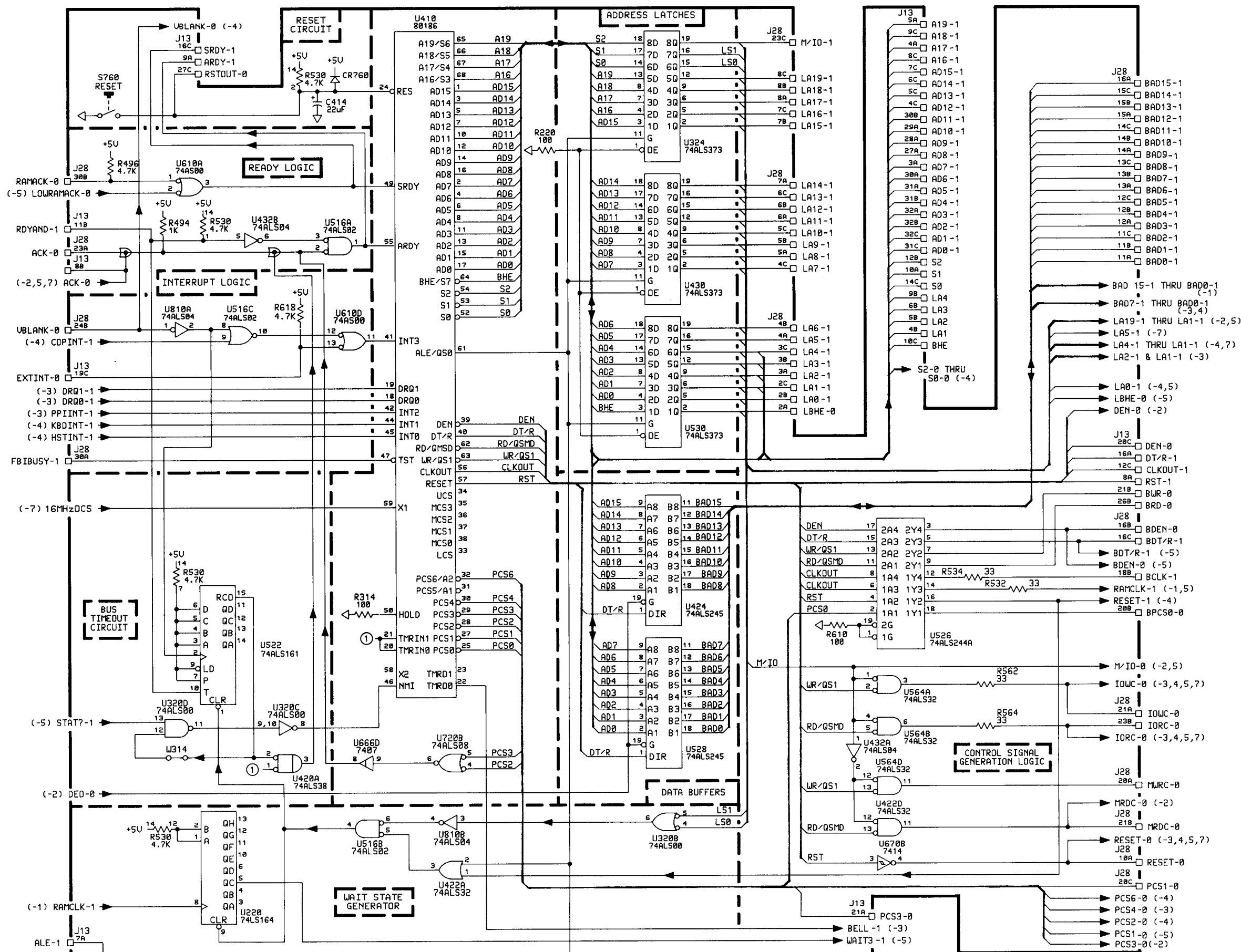


INTERCONNECT
(WITH 670-9725-XX DC BD.)





Terminal Control Component Locations (670-8523-00-02).



FIRST USE: 4111
 DATE: REV, 24 SEPT 85
 CONTROL NO.: SSA120.000

OTHER USES:

NOTES:

TEKTRONIX, INC. © 1985

TITLE: 670-8523-00,01,02

TERMINAL CONTROL BOARD

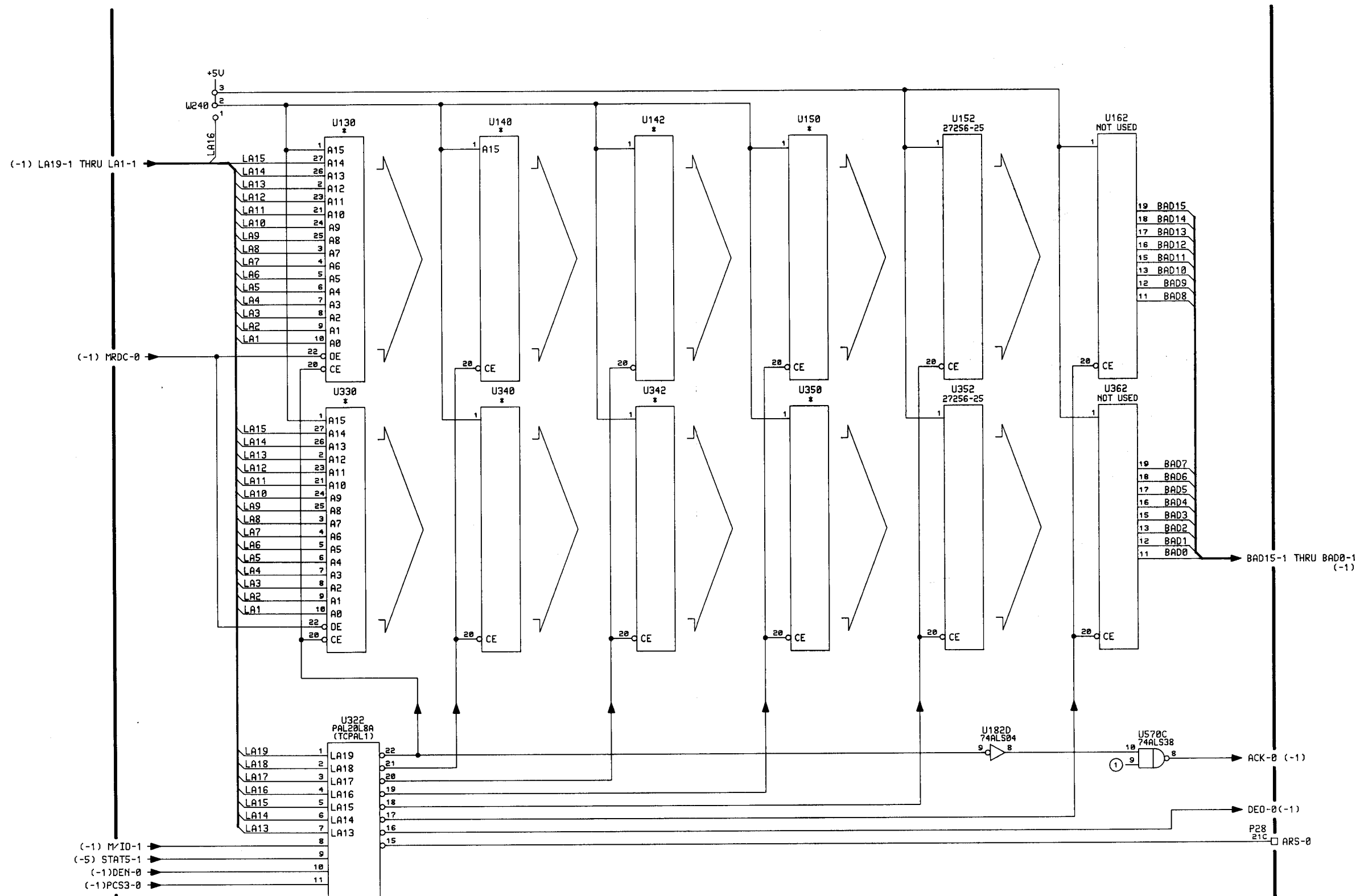
Tektronix®

ASSEMBLY:

TERMCTL

SHEET: 1 OF 7

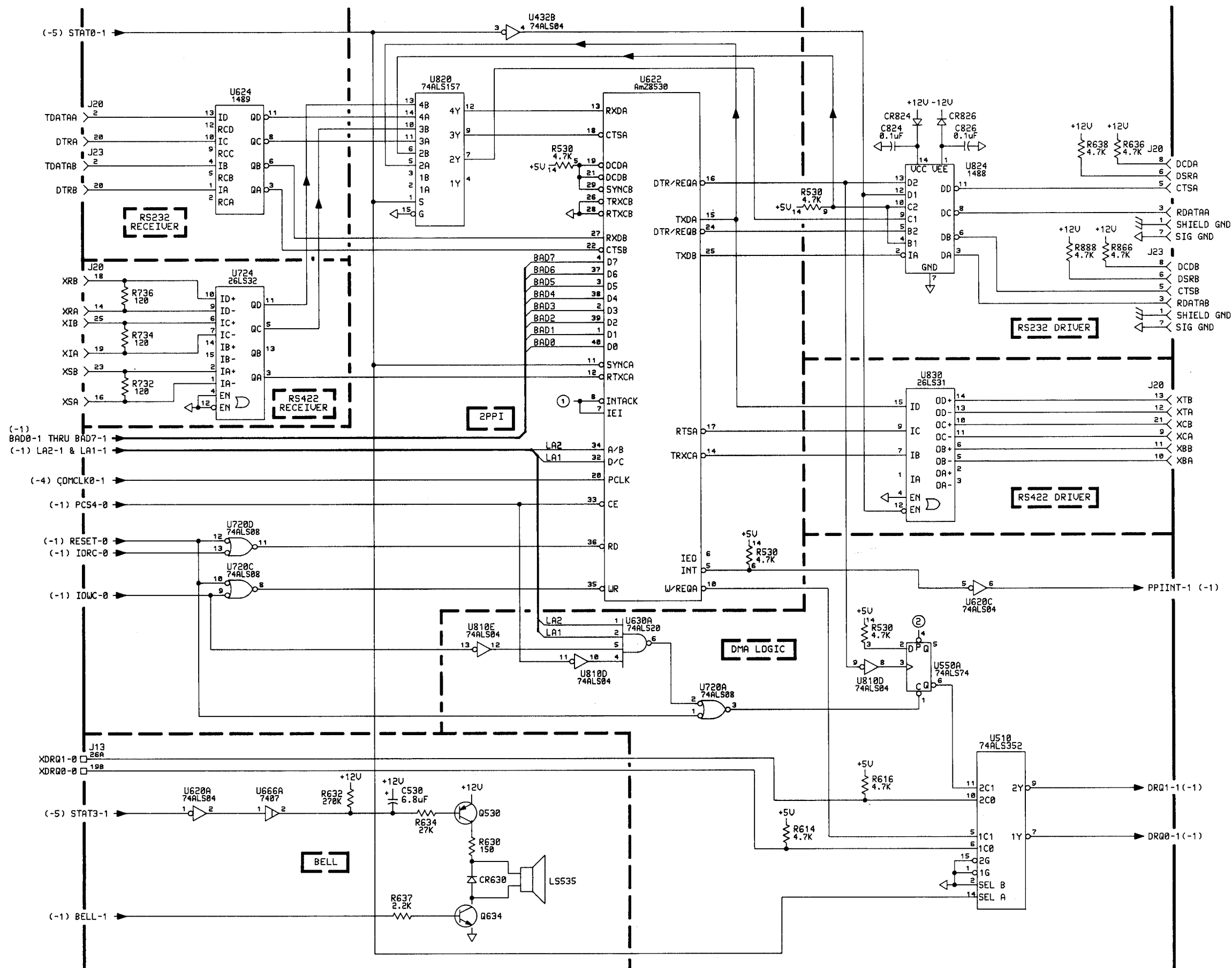
TERMINAL CONTROL BOARD
 (670-8523-00-02) TERMCTL-1

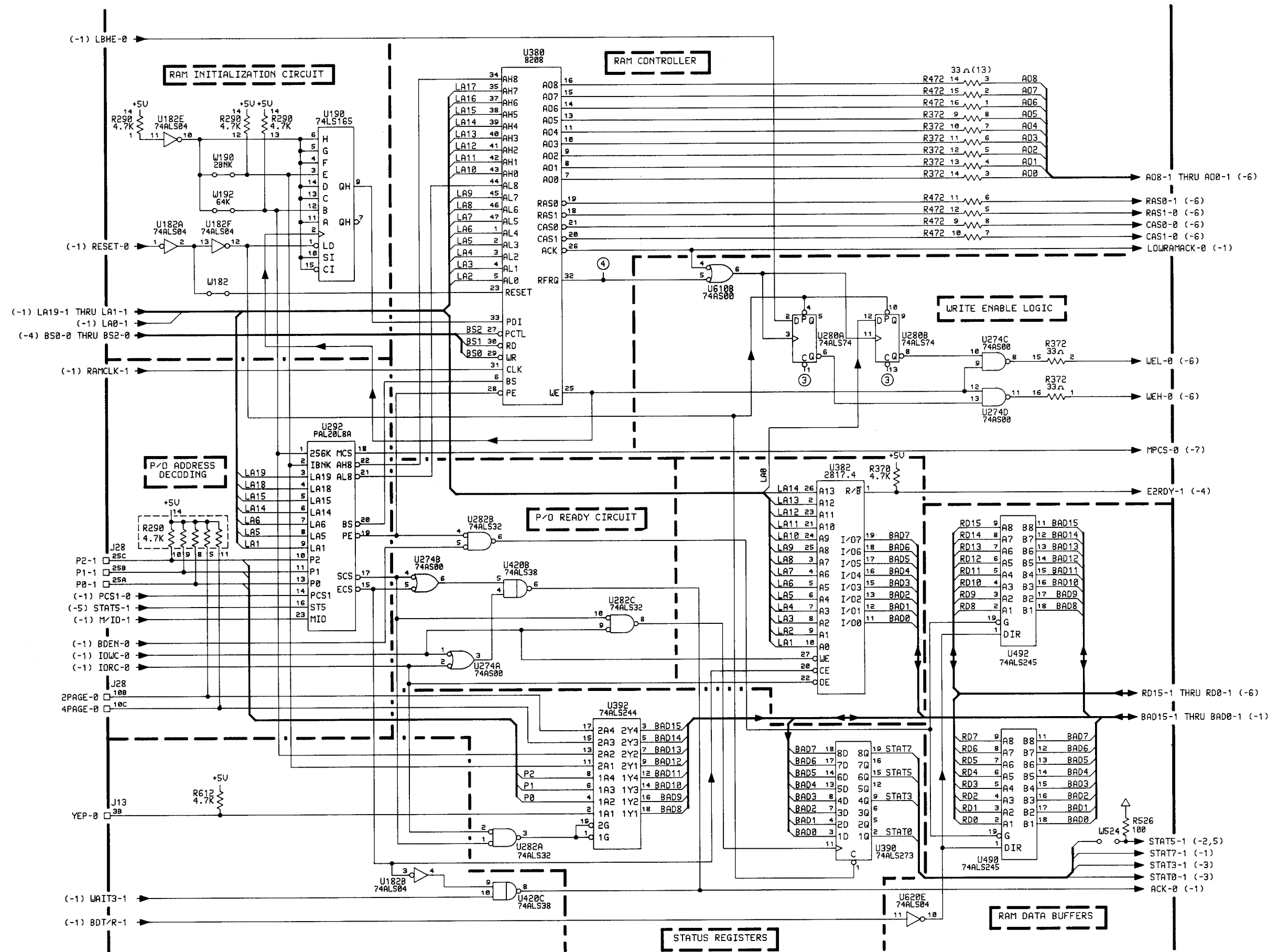


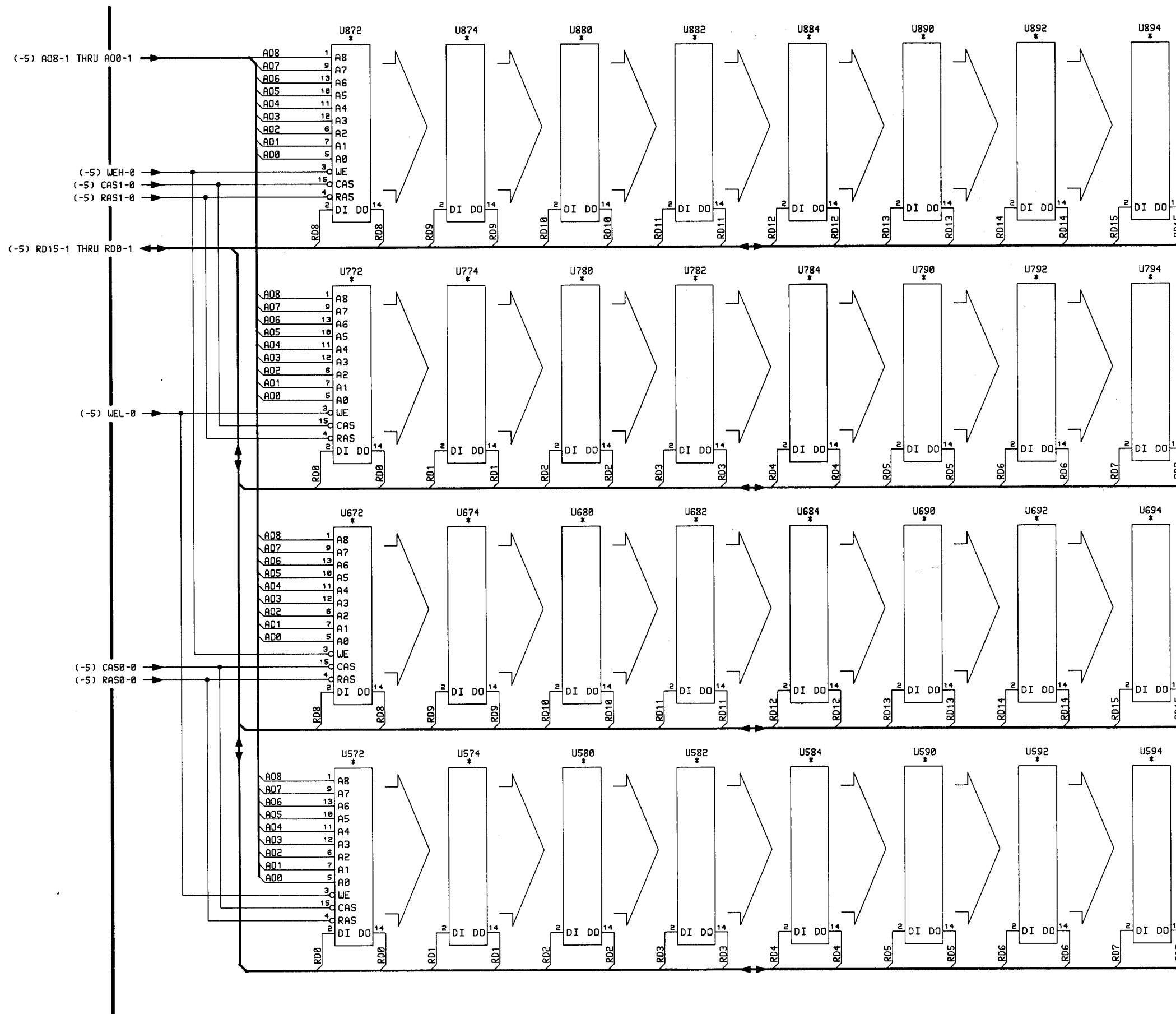
P/O ADDRESS DECODING

FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8523-00, 01, 02	ASSEMBLY:
DATE:	REV, 16 OCT 85		* MAY BE 27256-25 OR 27512-25. FOR LATTER, CUT STRAP BETWEEN U130-2 & 3, AND SHORT W130-1 & 2.	TERMINAL CONTROL BOARD	TERMCTL
CONTROL NO.:	SSA120.000		TEKTRONIX, INC. © 1985		SHEET: 2 OF 7

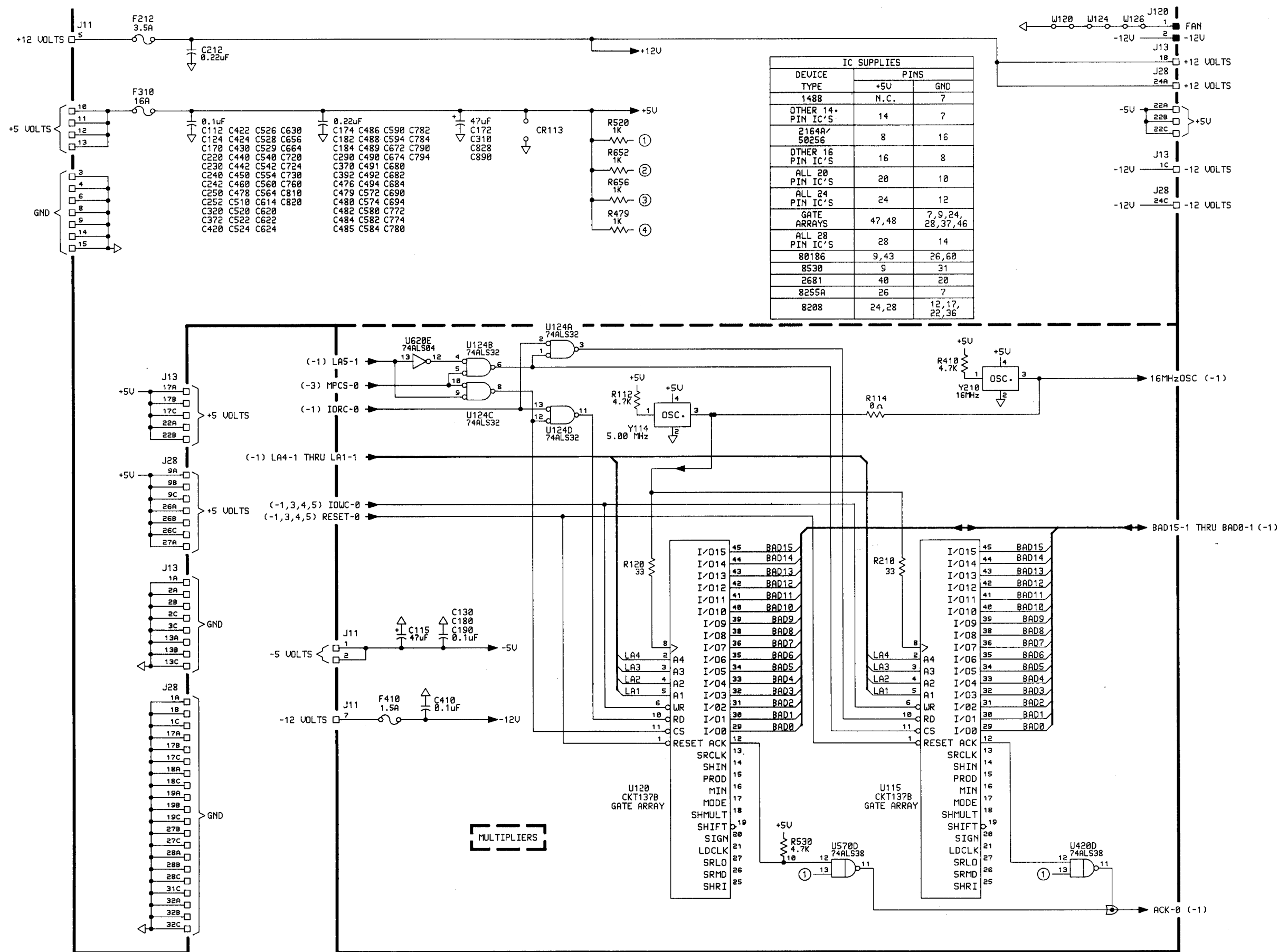
Tektronix®

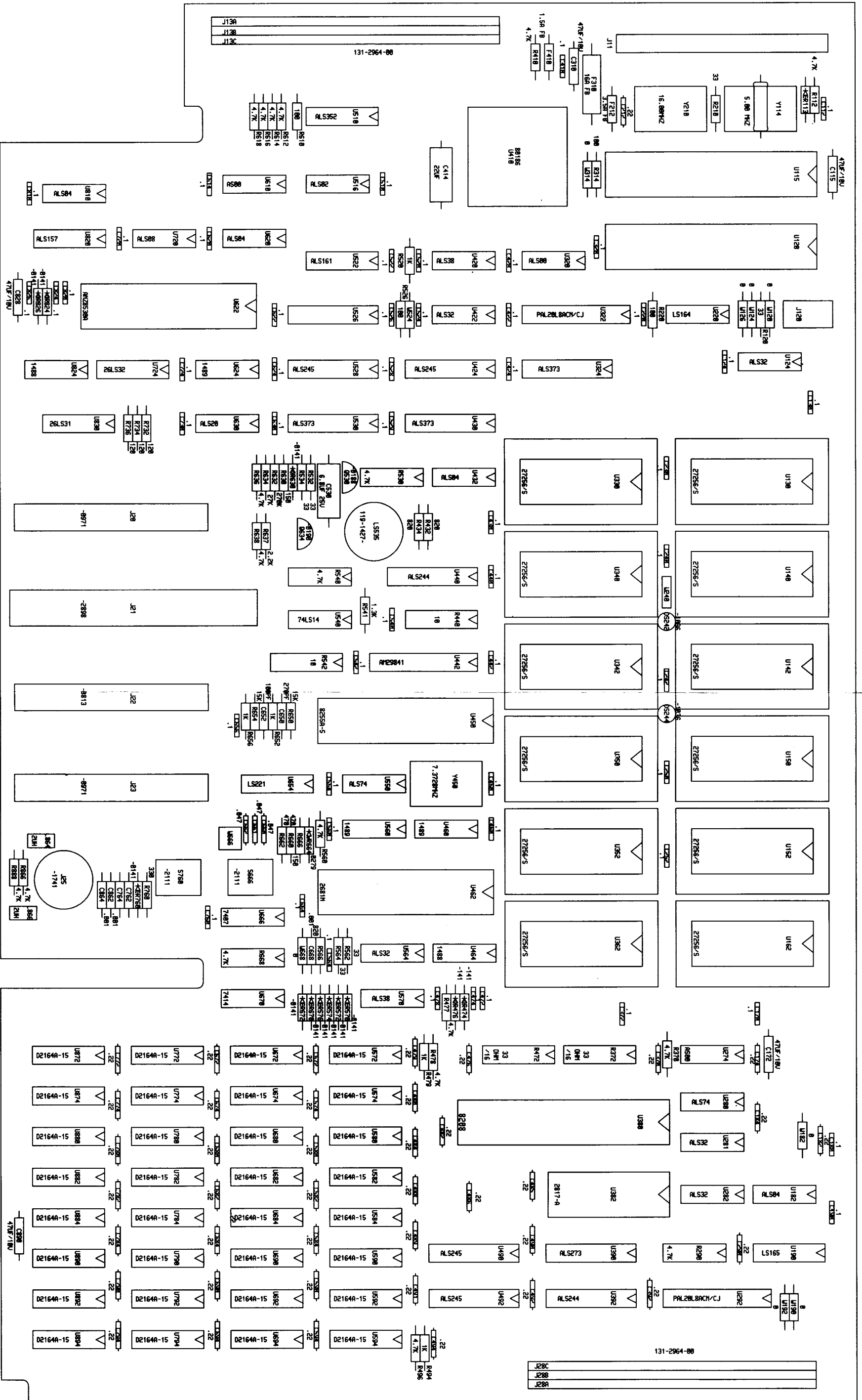




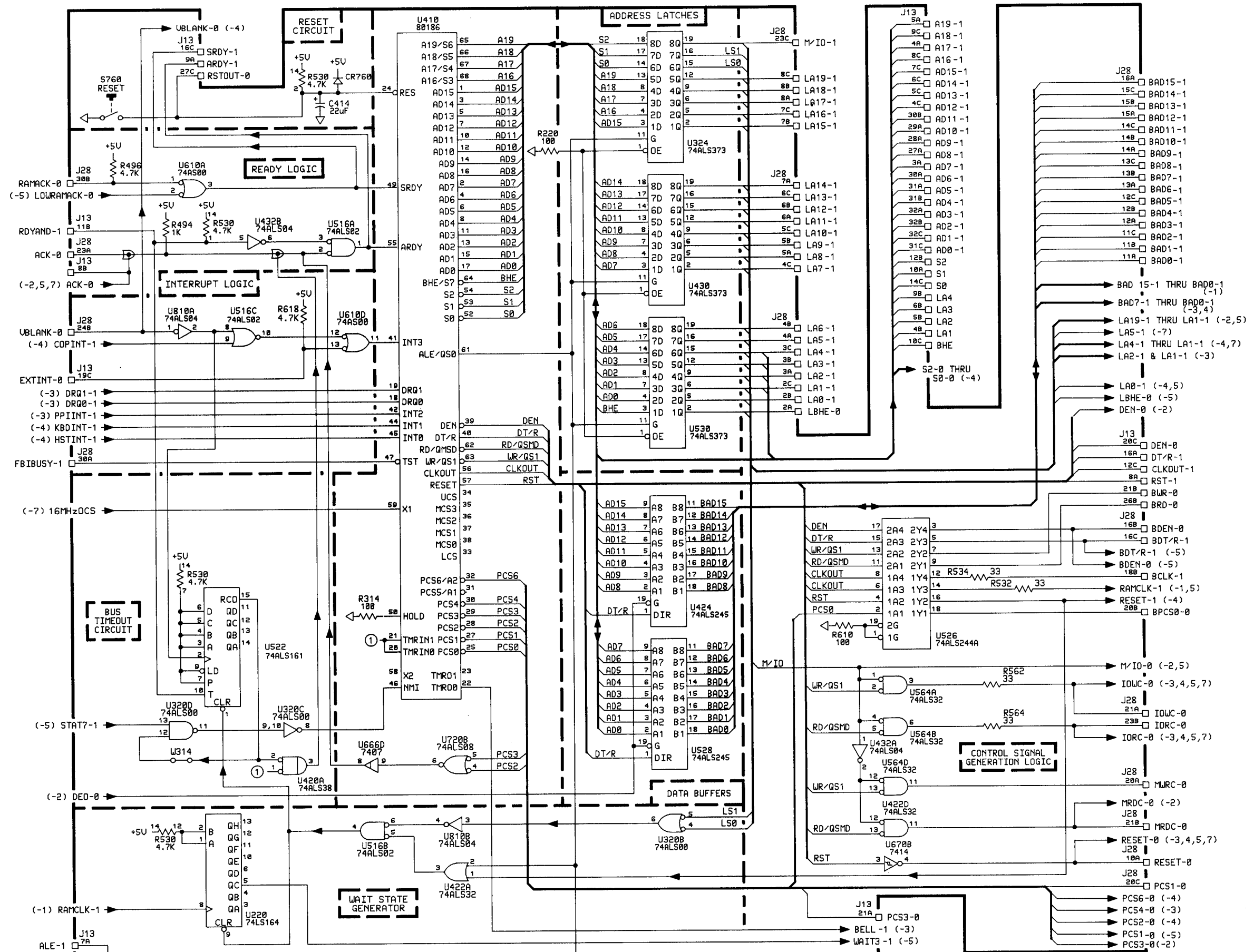


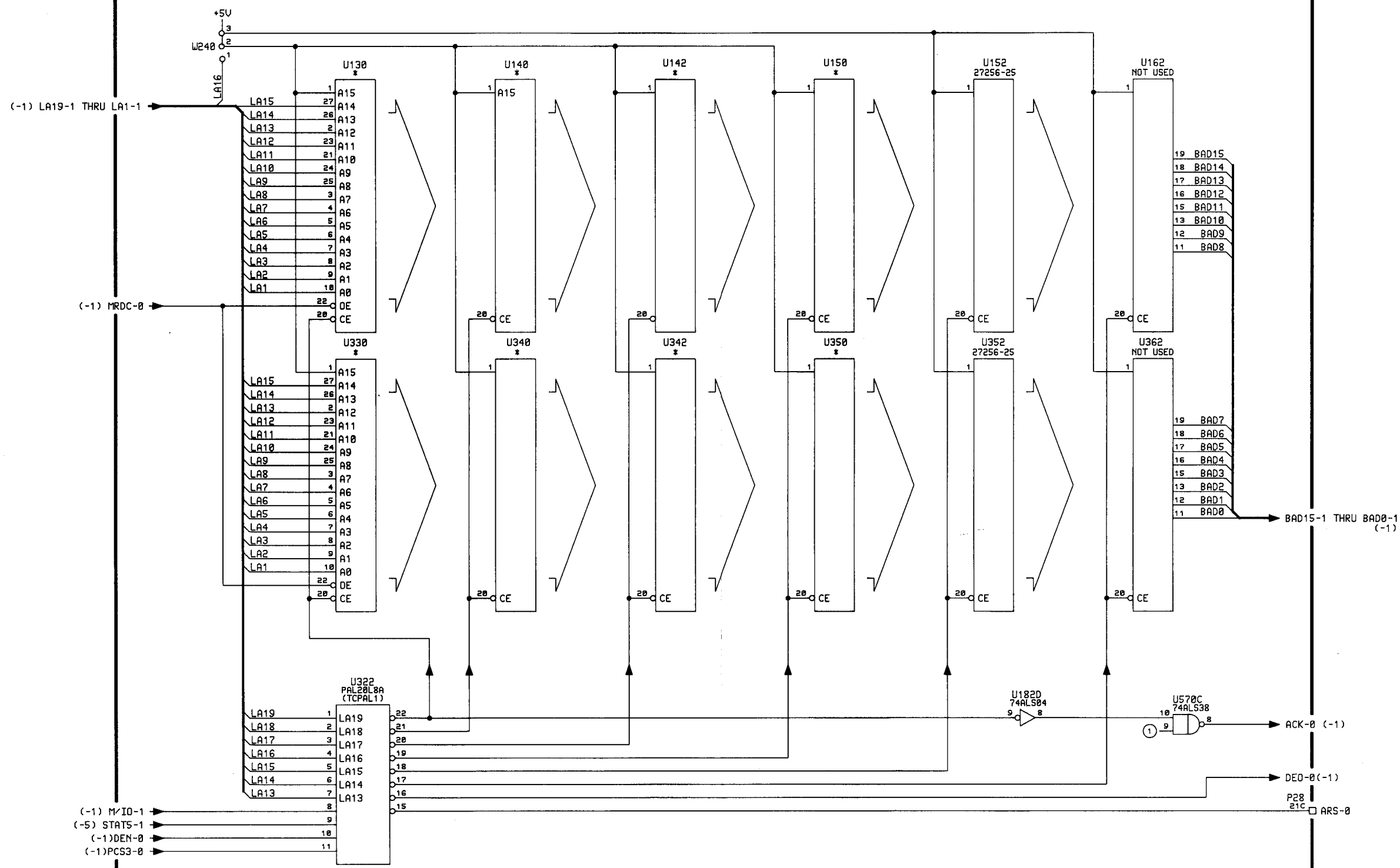
FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8523-00 ,01,02	ASSEMBLY:
DATE:	REV, 24 SEPT 85		* 2164A-15 STANDARD , OPTIONAL HM50256-15 OR UPD41256-15	TERMINAL CONTROL BOARD	TERMCTL
CONTROL NO.:	SSA120.000		TEKTRONIX, INC. © 1985	Tektronix®	SHEET: 6 OF 7



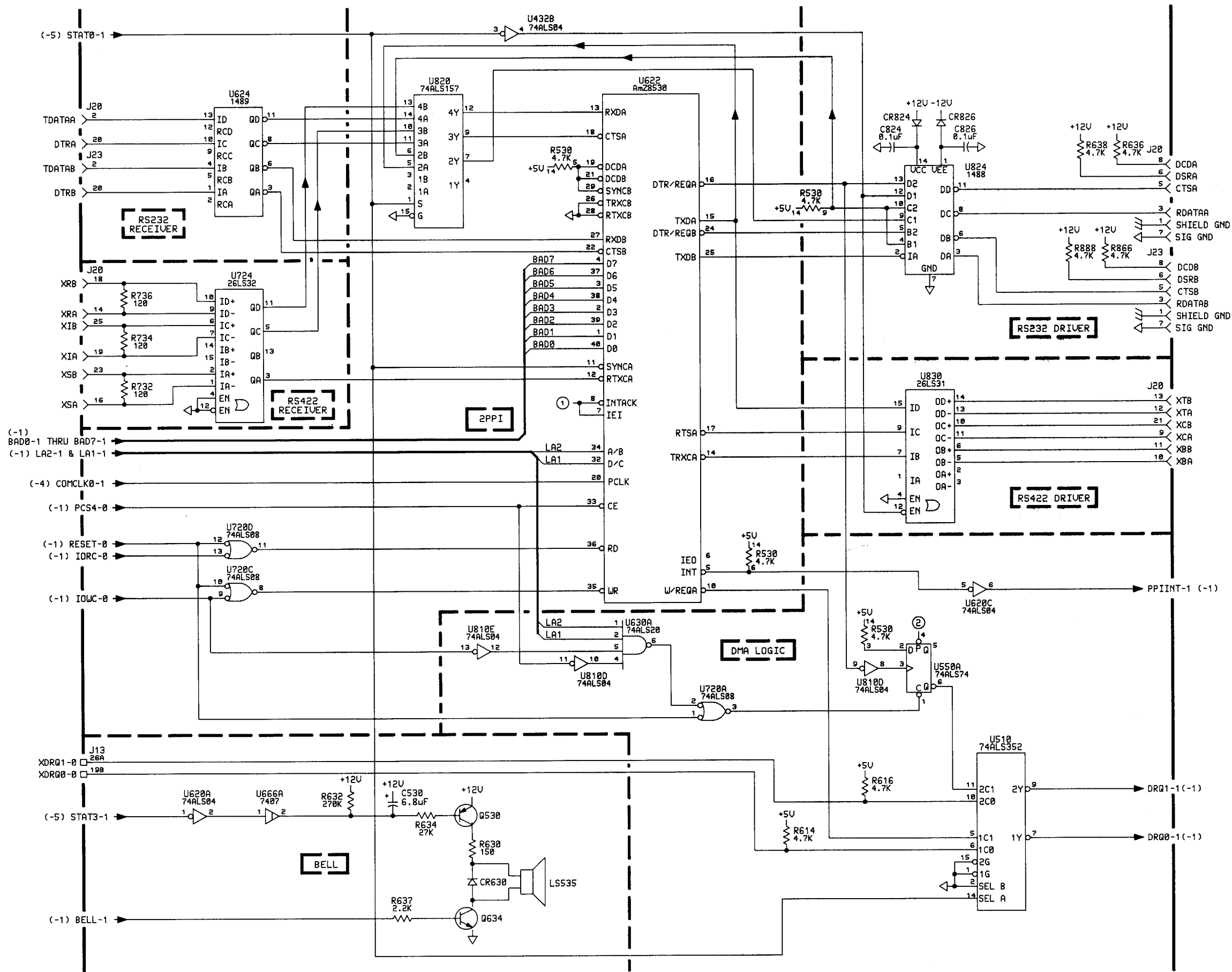


Terminal Control Component Locations (670-8523-03).

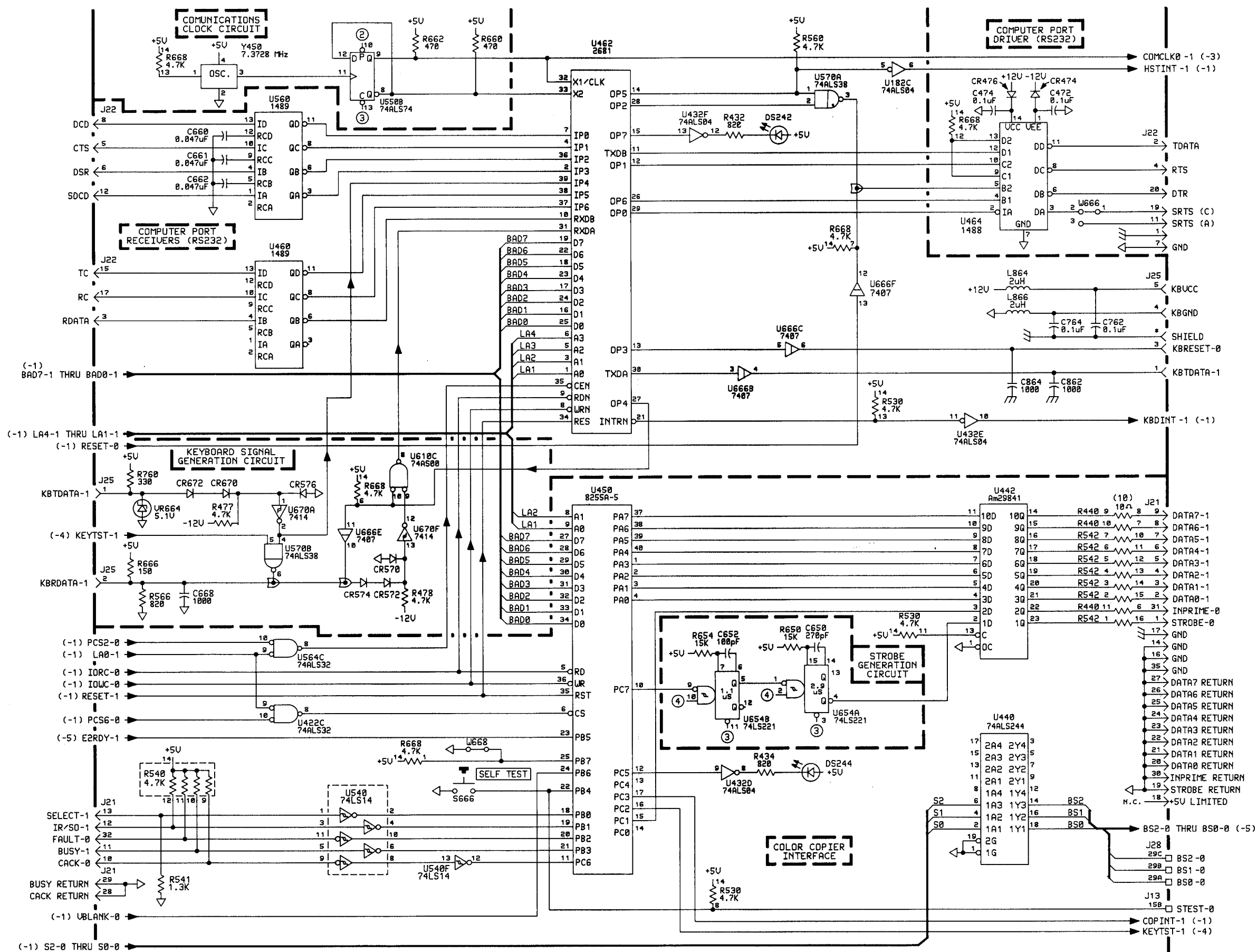


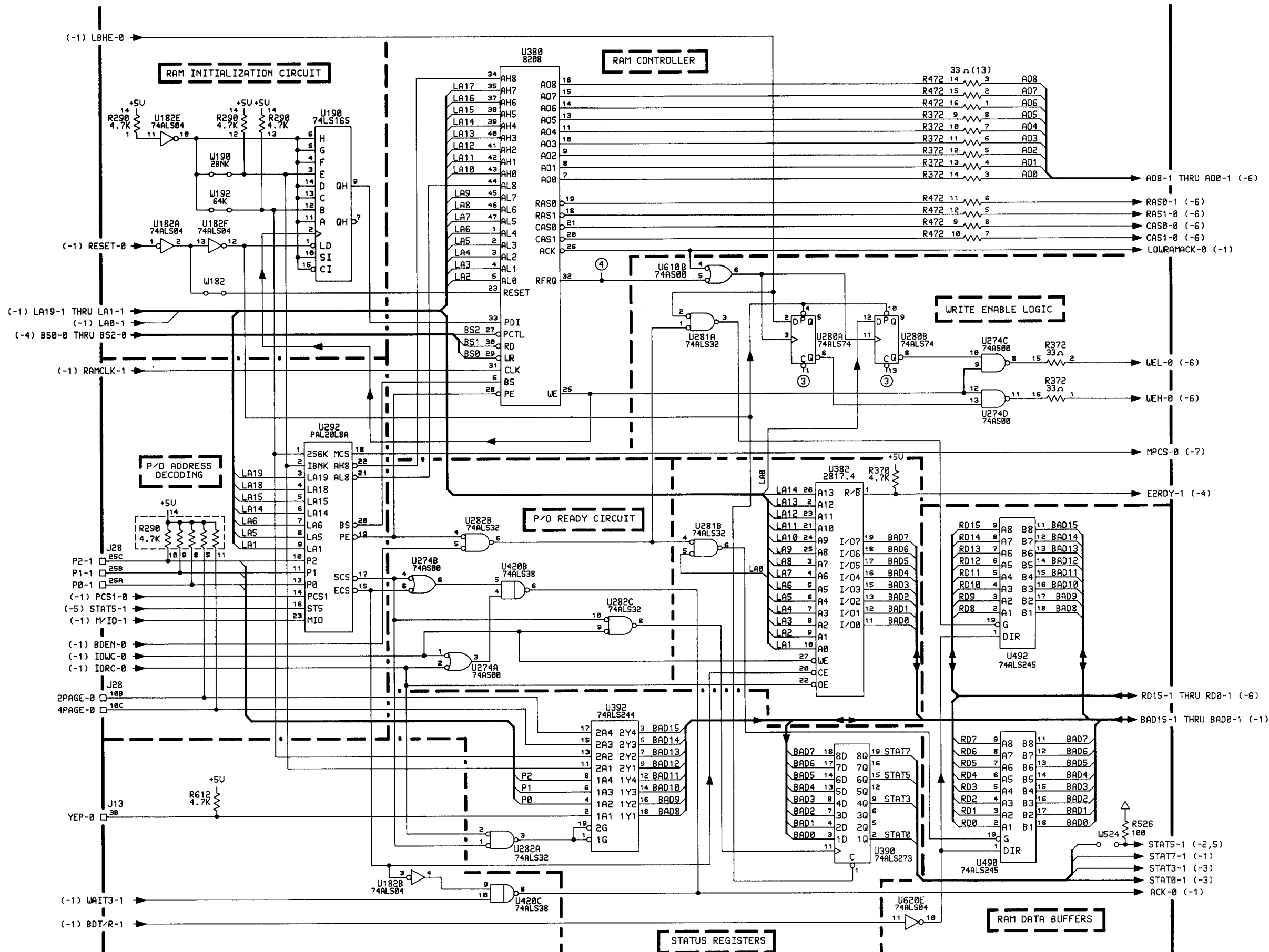


P/O ADDRESS DECODING

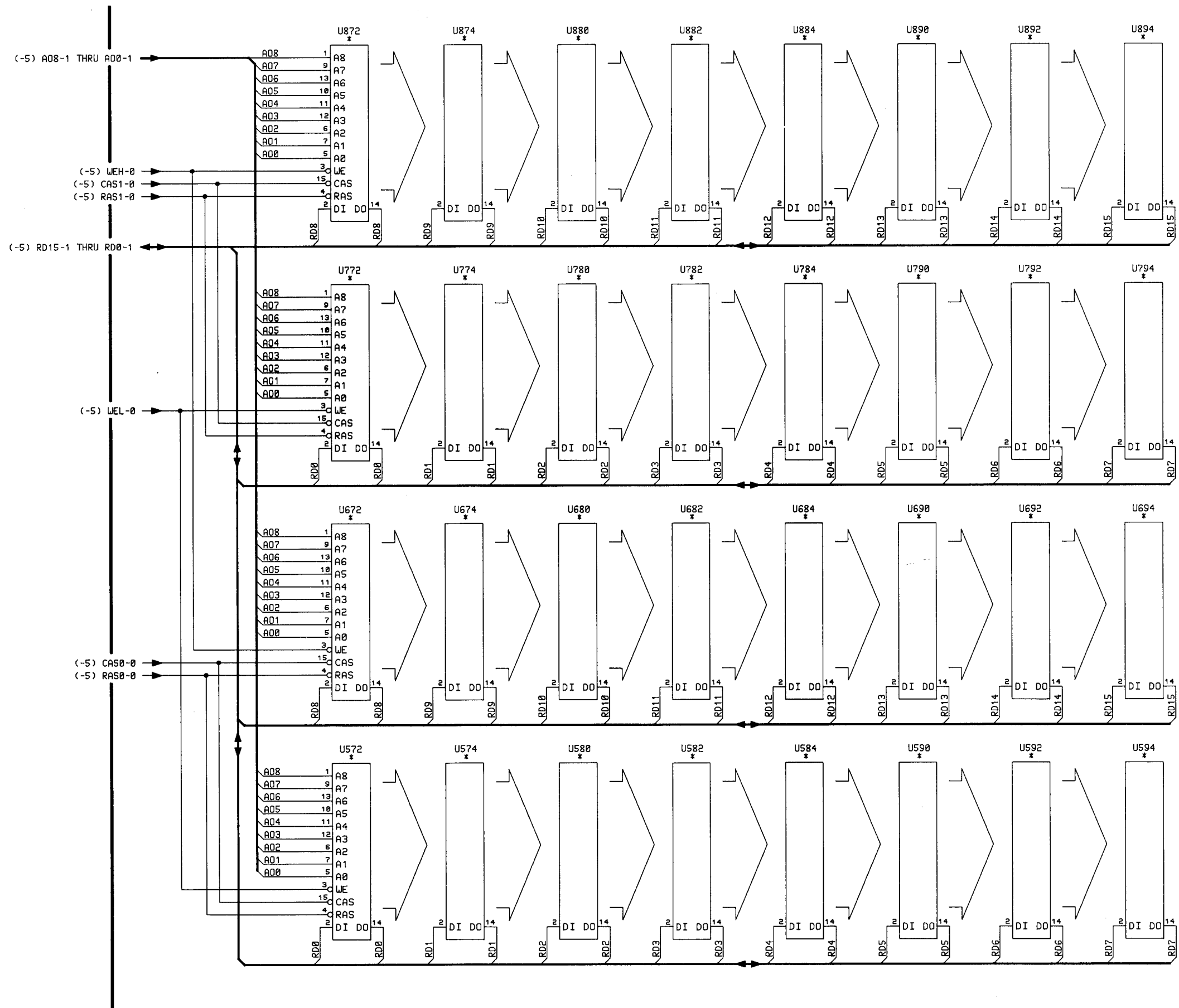


FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8523-03	ASSEMBLY:
DATE:	REV, 10 JUN 1986			TERMINAL CONTROL BOARD	TERMCTL
CONTROL NO.:	SSA120.000		TEKTRONIX, INC. © 1985		SHEET: 3 OF 7



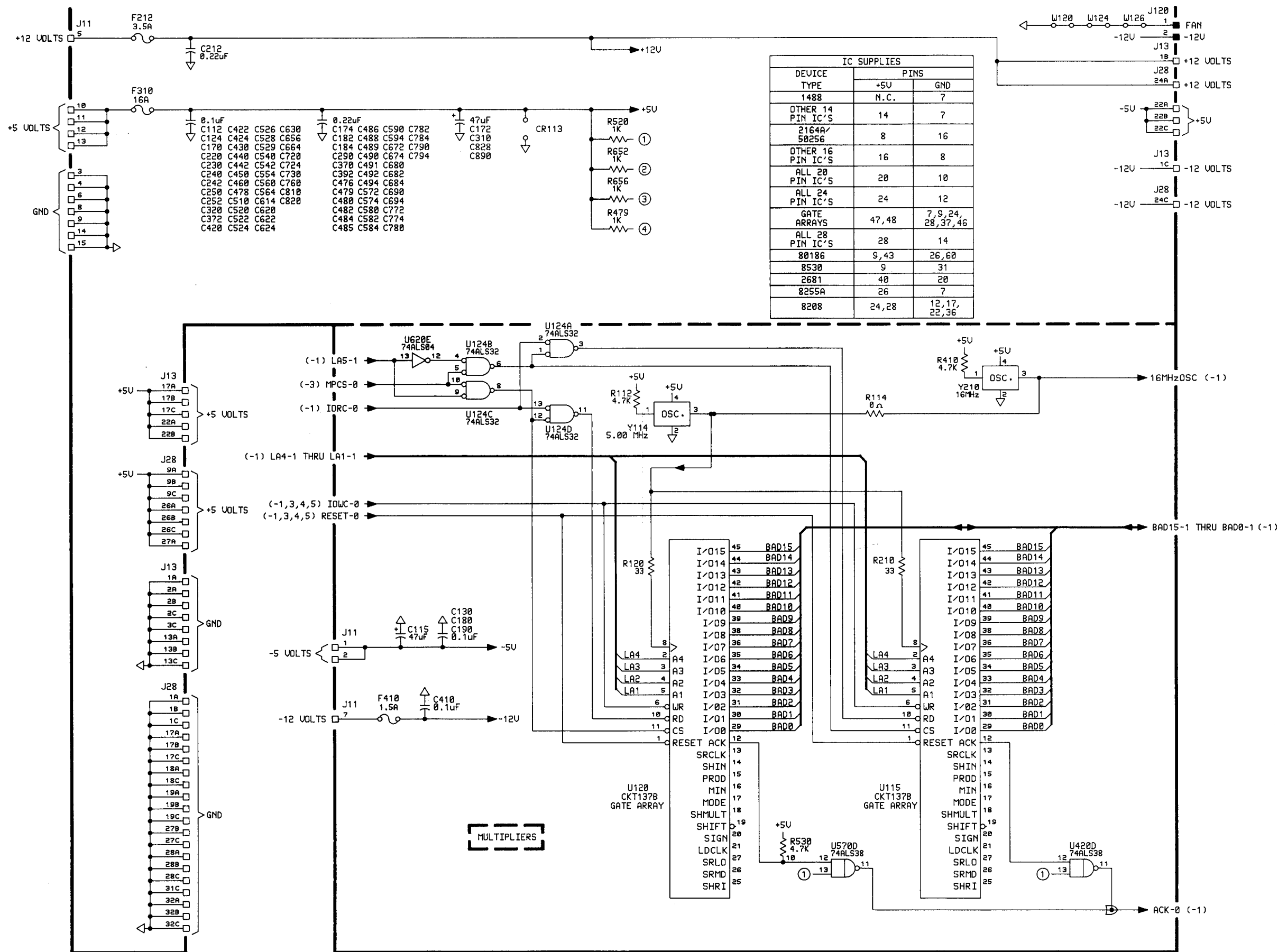


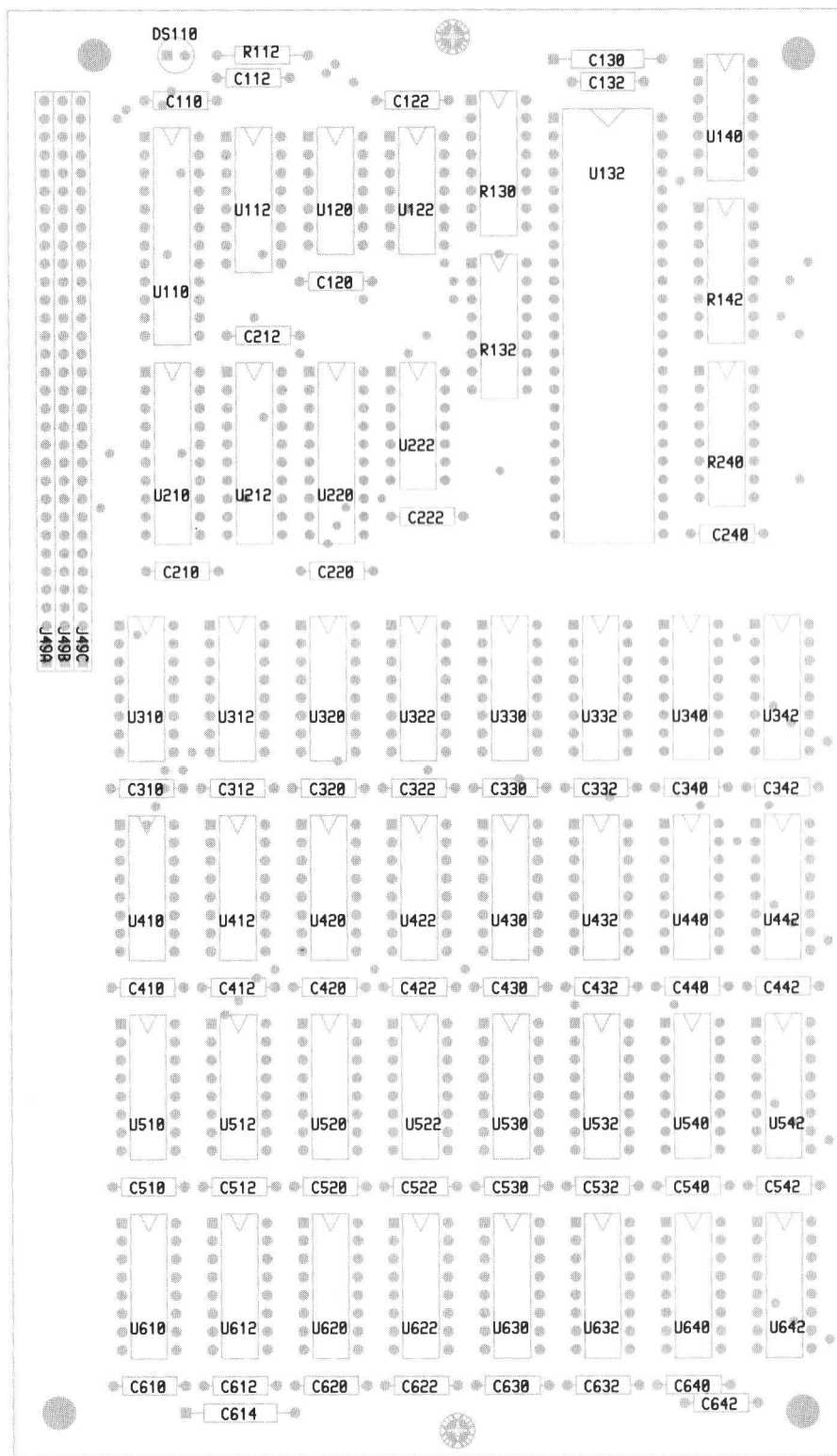
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DATE:	REV, 10 JUN 1986			TERMINAL CONTROL BOARD	TERMCTL
CONTROL NO.:	SSA120.000		TEKTRONIX, INC. © 1985		SHEET: 5 OF 7



FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8523-03	ASSEMBLY:
DATE:	REV, 10 JUN 1986		* 2164A-15 STANDARD , OPTIONAL HM50256-15 OR UPD41256-15	TERMINAL CONTROL BOARD	TERMCTL
CONTROL NO.:	SSA120.000		TEKTRONIX, INC. © 1985		SHEET: 6 OF 7

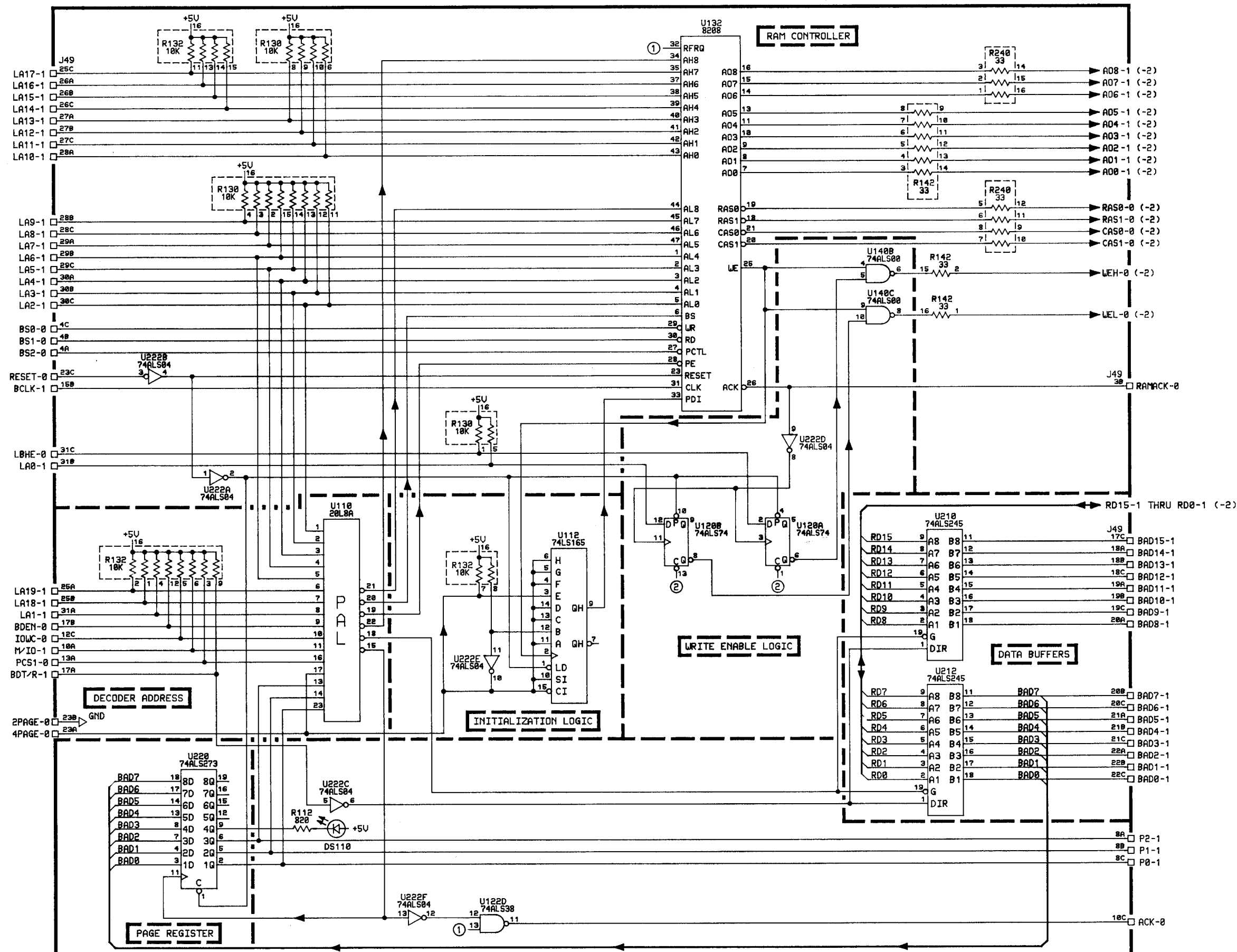
Tektronix®

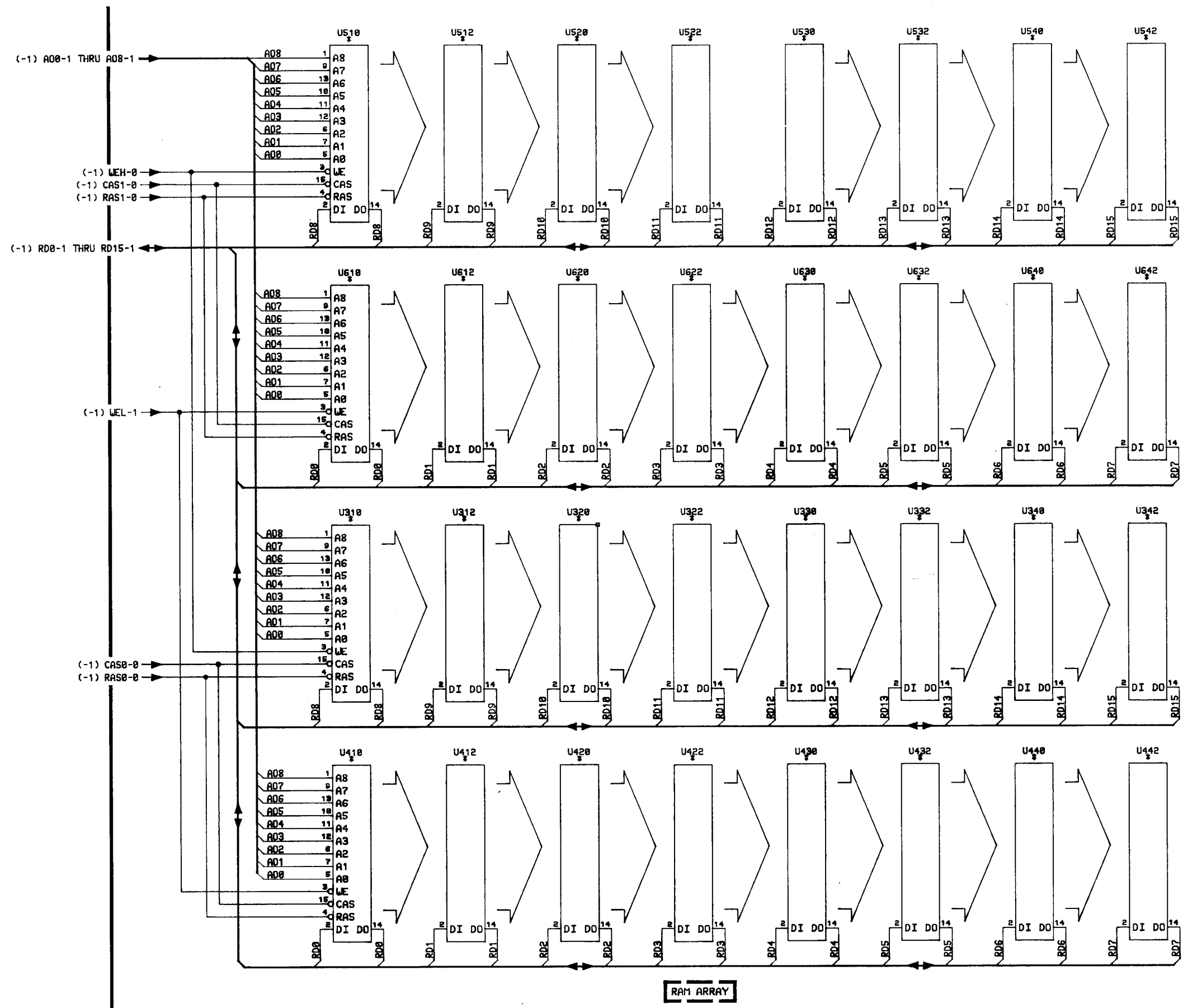




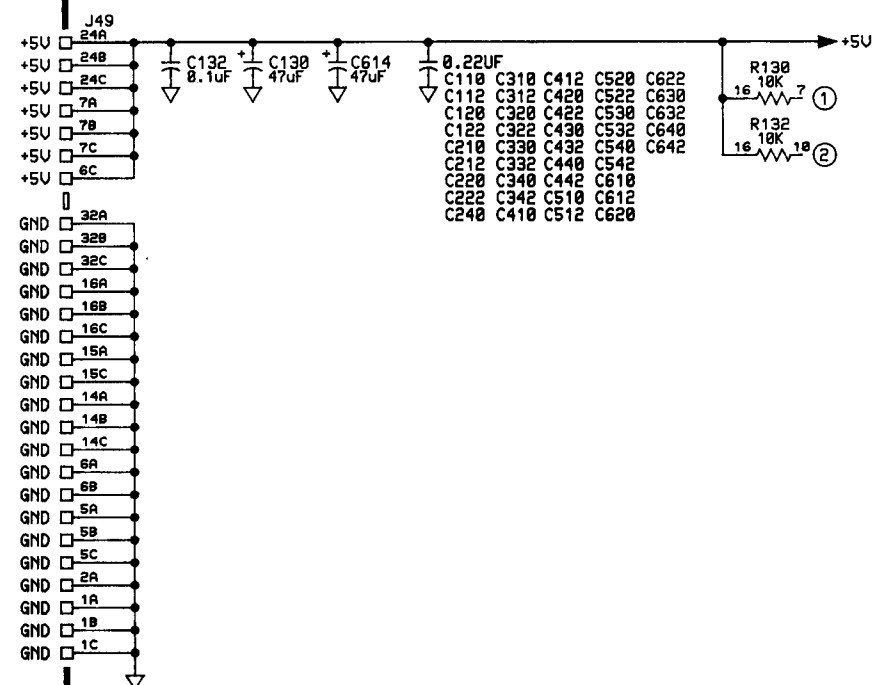
5644-61

RAM Option Board Component Locations (670-8526-00).

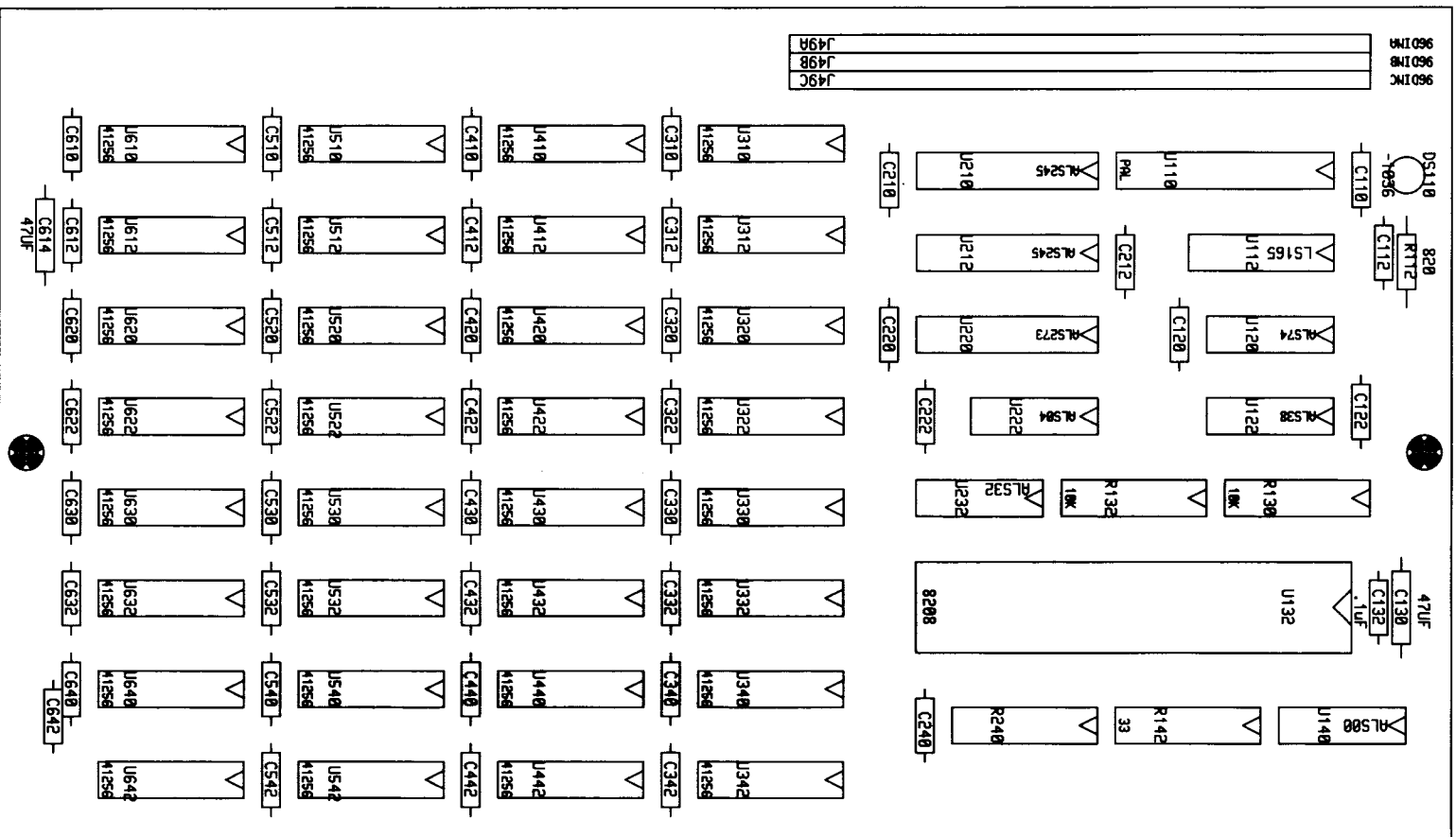




FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8526-00		ASSEMBLY:
DATE:	REV, 20 AUG 85		* MAY BE EITHER HM50256-15 OR UPD41256-15	RAM OPTION BOARD		RAMOPT
CONTROL NO.:	SSA119.000		TEKTRONIX, INC. © 1985			SHEET: 2 OF 3

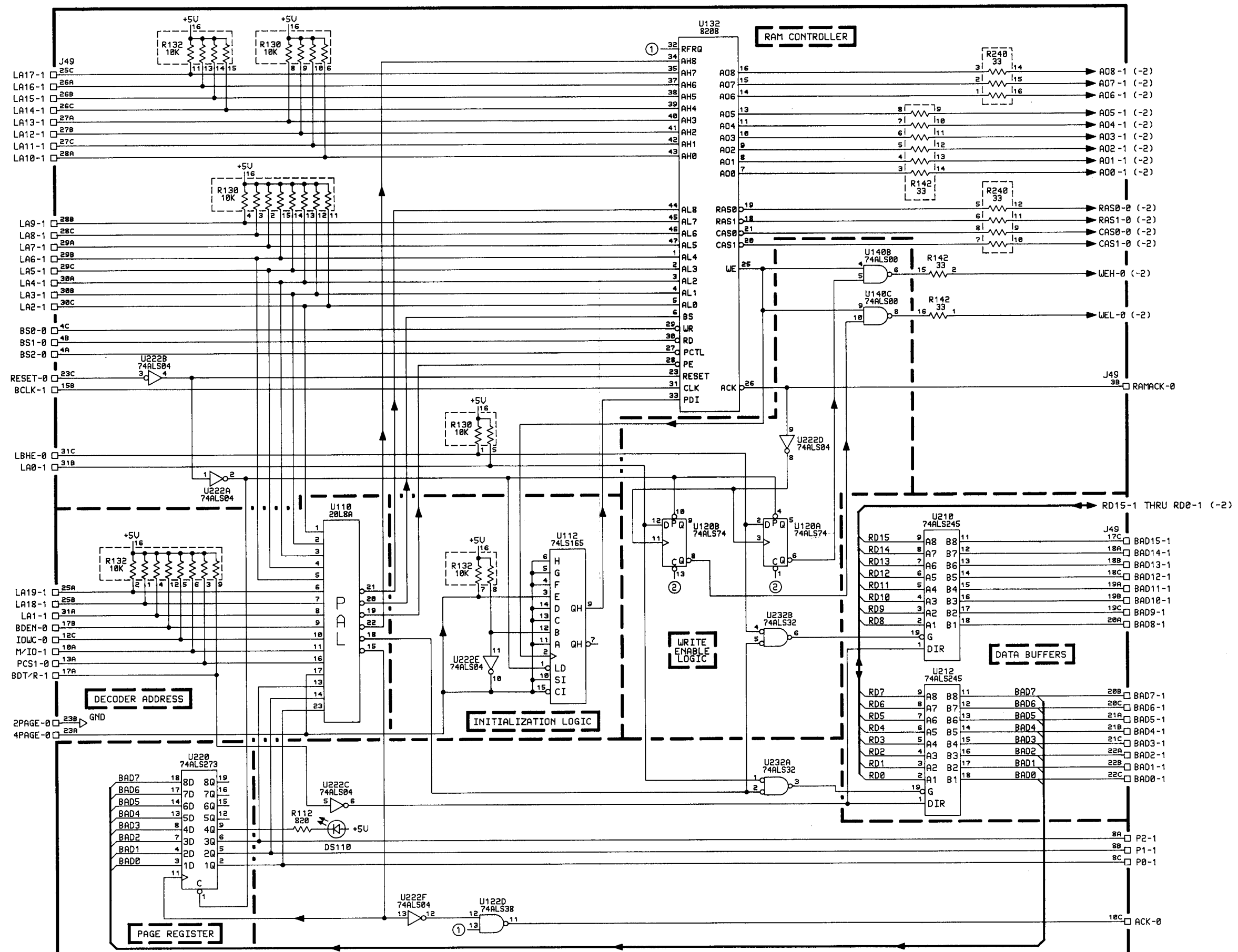


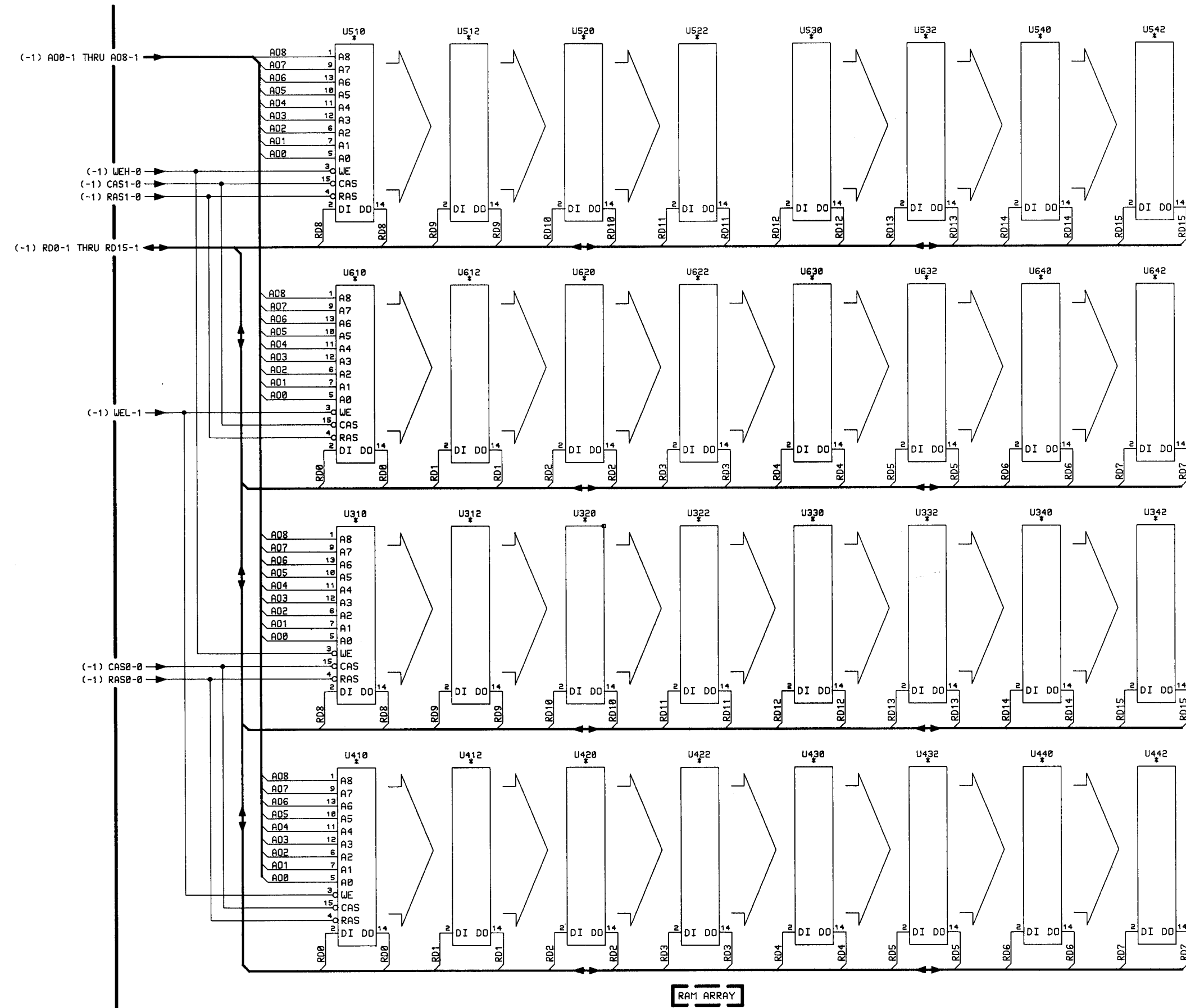
I.C. SUPPLIES		
DEVICE TYPE	PINS	
	+5V	GND
8208	24, 48	12, 17, 22, 36
ALL 14 PIN IC'S	14	7
HM50256-15/ UPD41256-15	8	16
ALL 20 PIN IC'S	20	10
ALL 24 PIN IC'S	24	12



RAM Option Board Component Locations (670-8526-01).

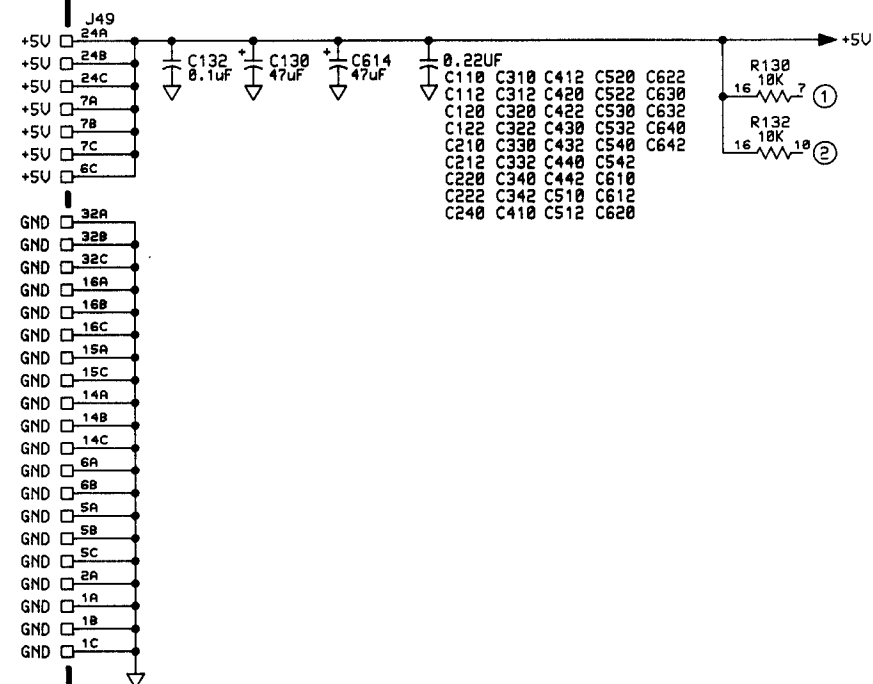
5644-118



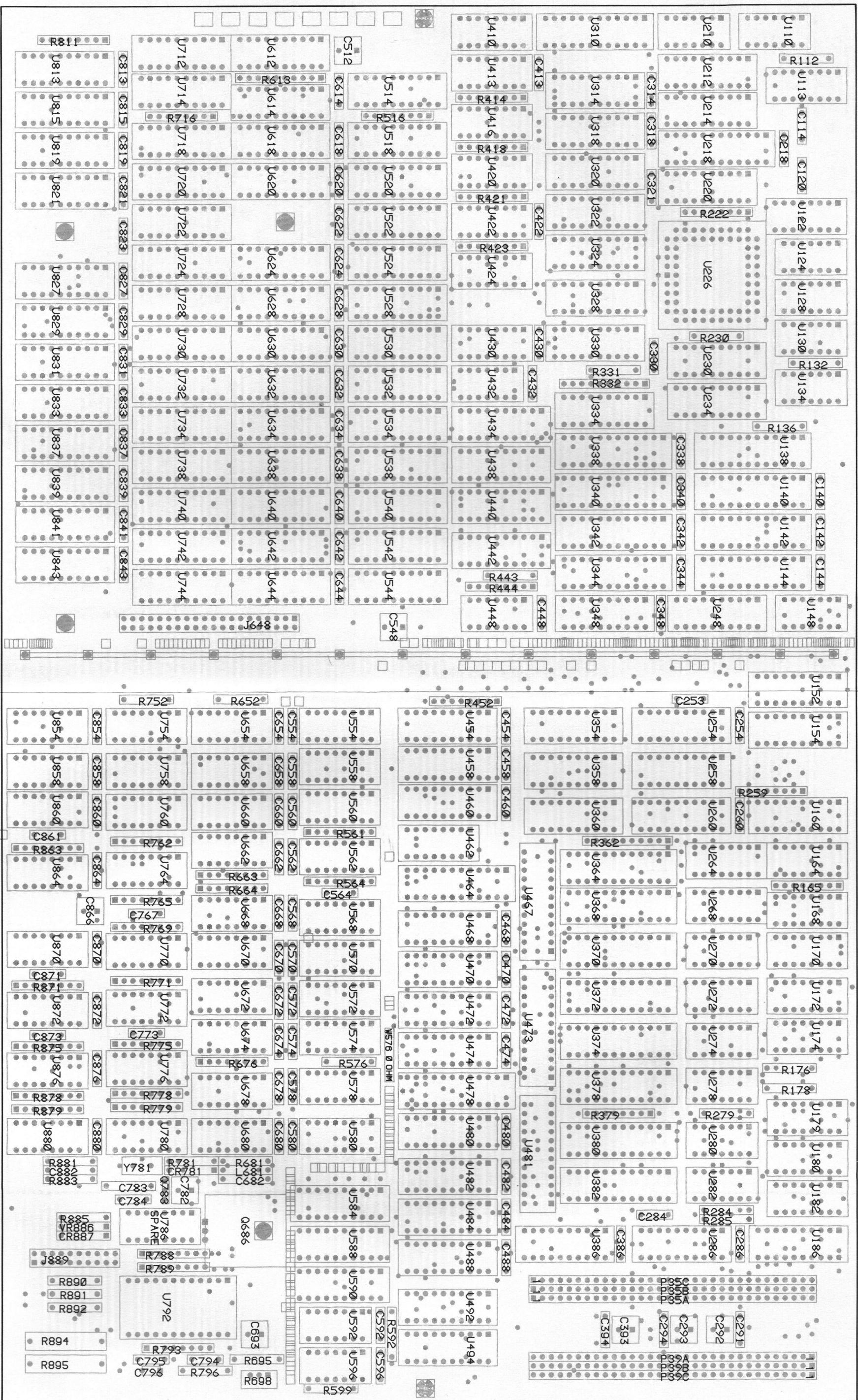


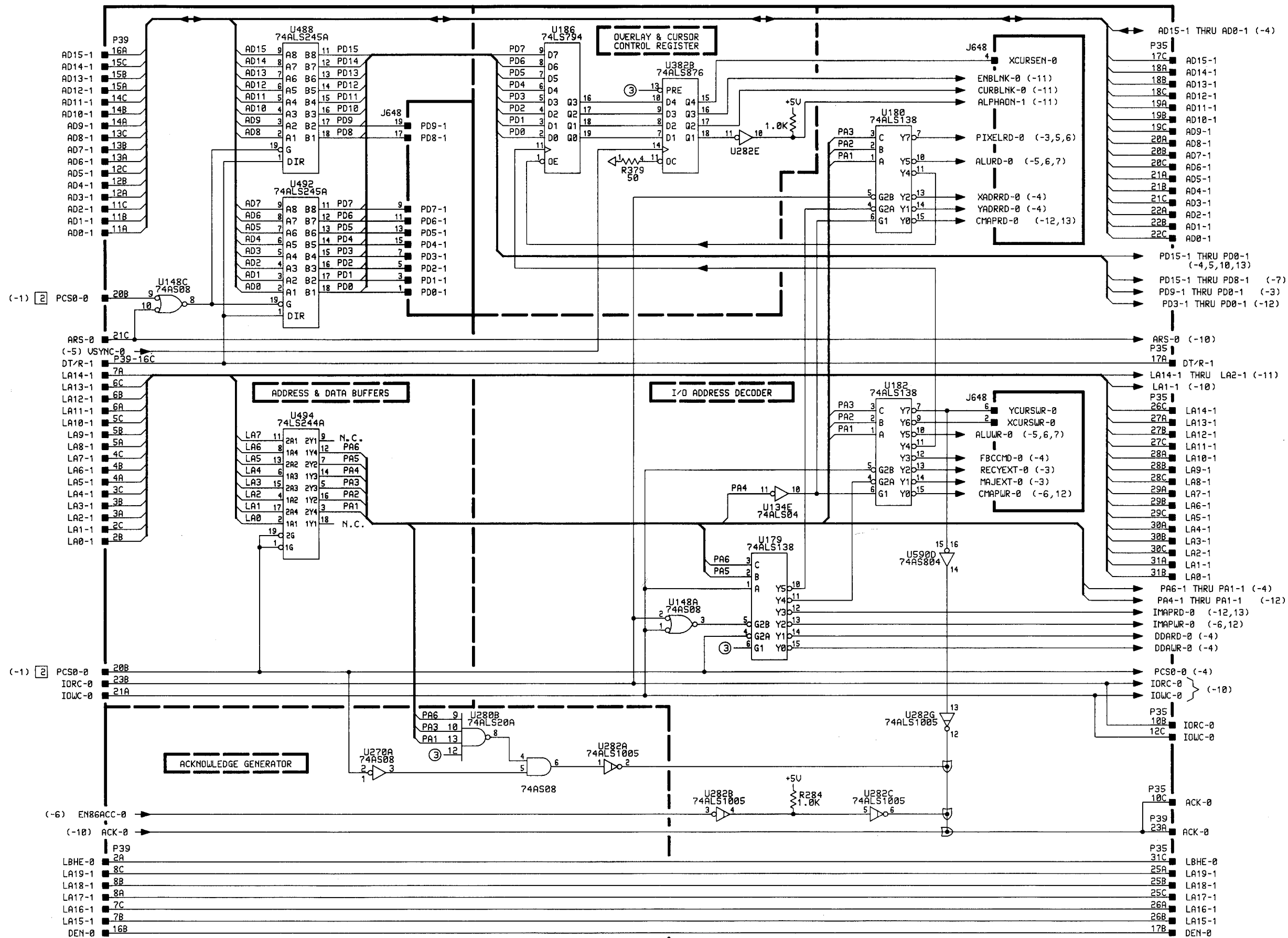
FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8526-01	ASSEMBLY:
DATE:	REV, 20 AUG 85		* MAY BE EITHER HM50256-15 OR UPD41256-15	RAM OPTION BOARD	RAMOPT
CONTROL NO.:	SSA119.000		TEKTRONIX, INC. © 1985		SHEET: 2 OF 3

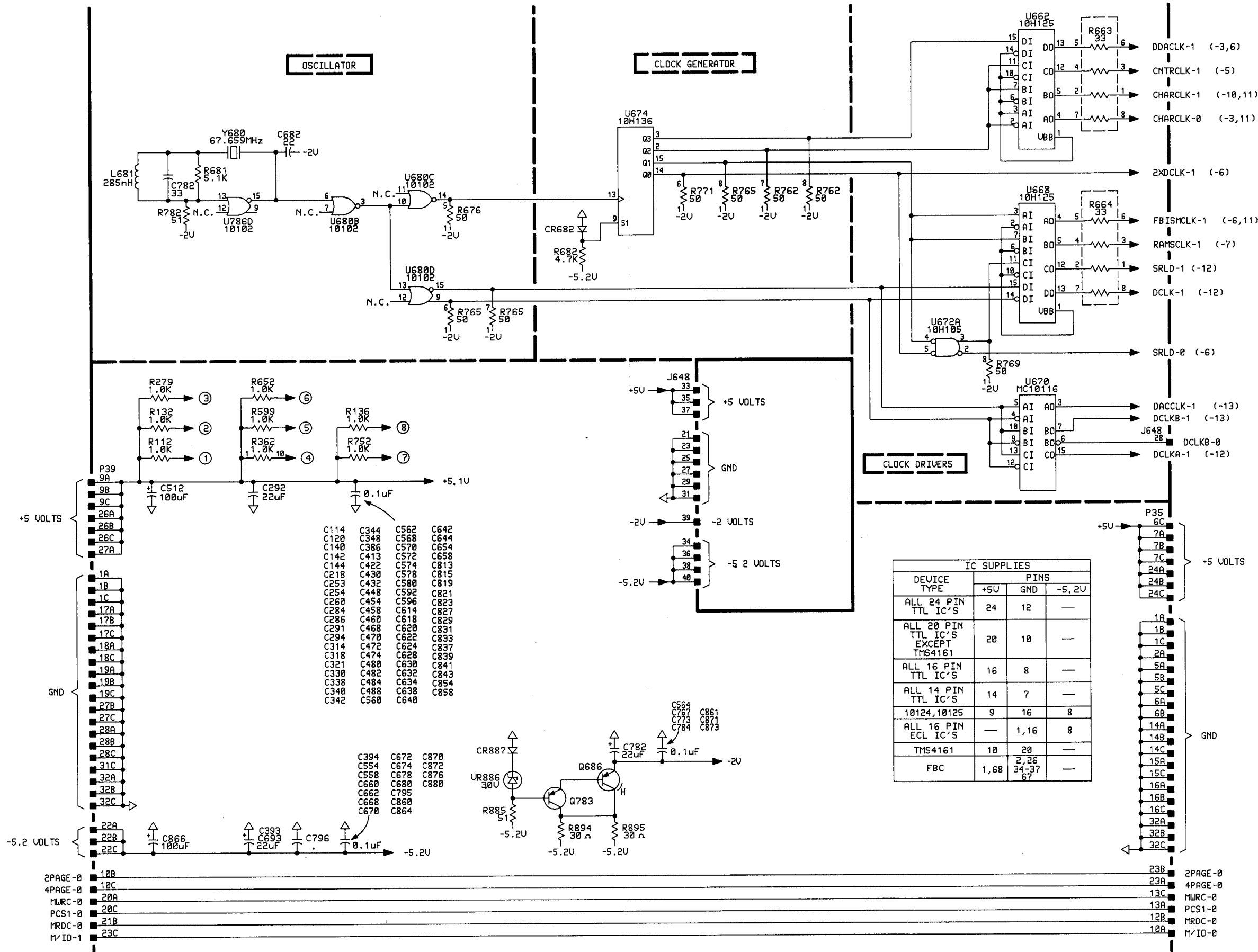


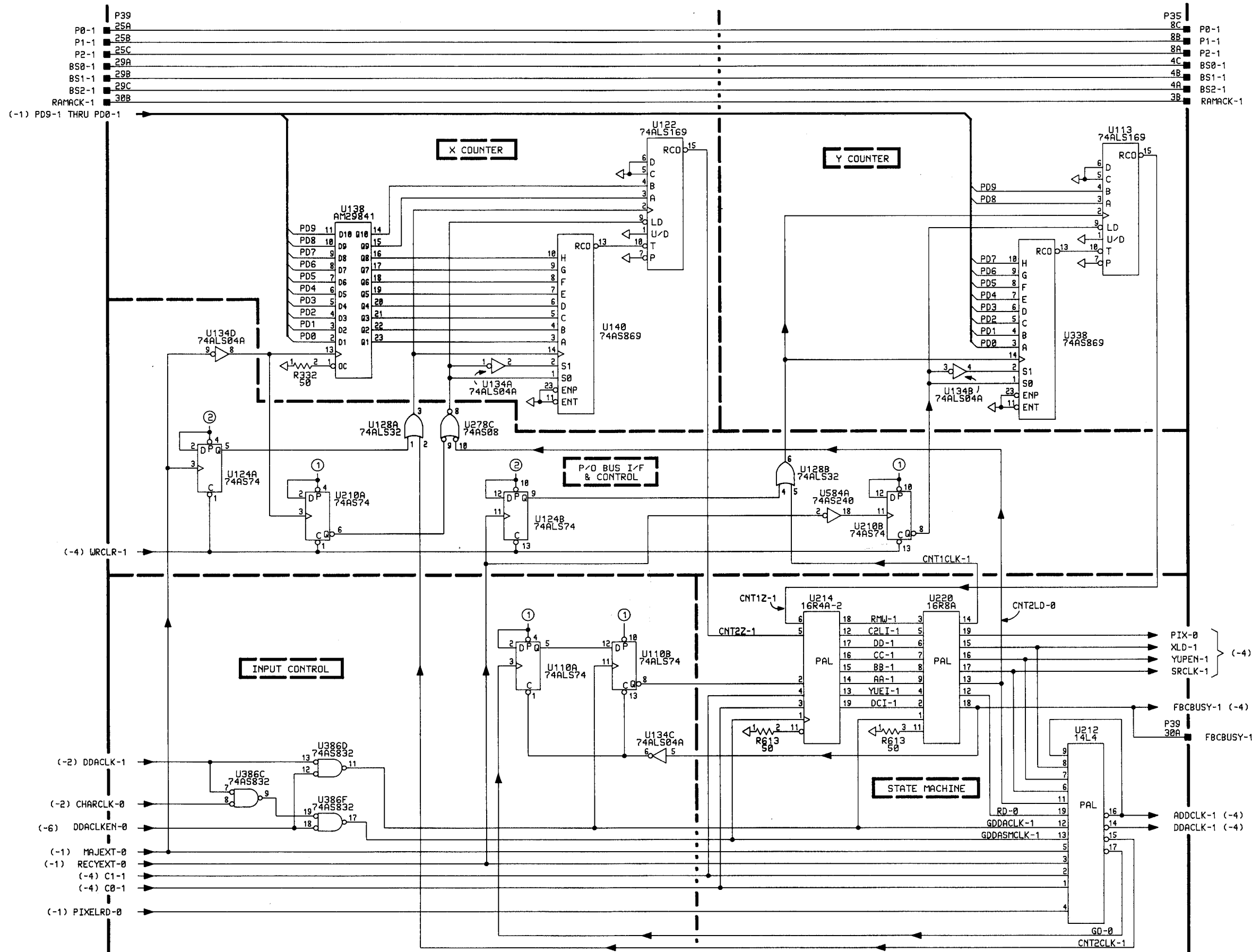


I.C. SUPPLIES		
DEVICE TYPE	PINS	
	+5V	GND
8208	24, 48	12, 17, 22, 36
ALL 14 PIN IC'S	14	7
HMS0256-15/ UPD41256-15	8	16
ALL 20 PIN IC'S	20	10
ALL 24 PIN IC'S	24	12

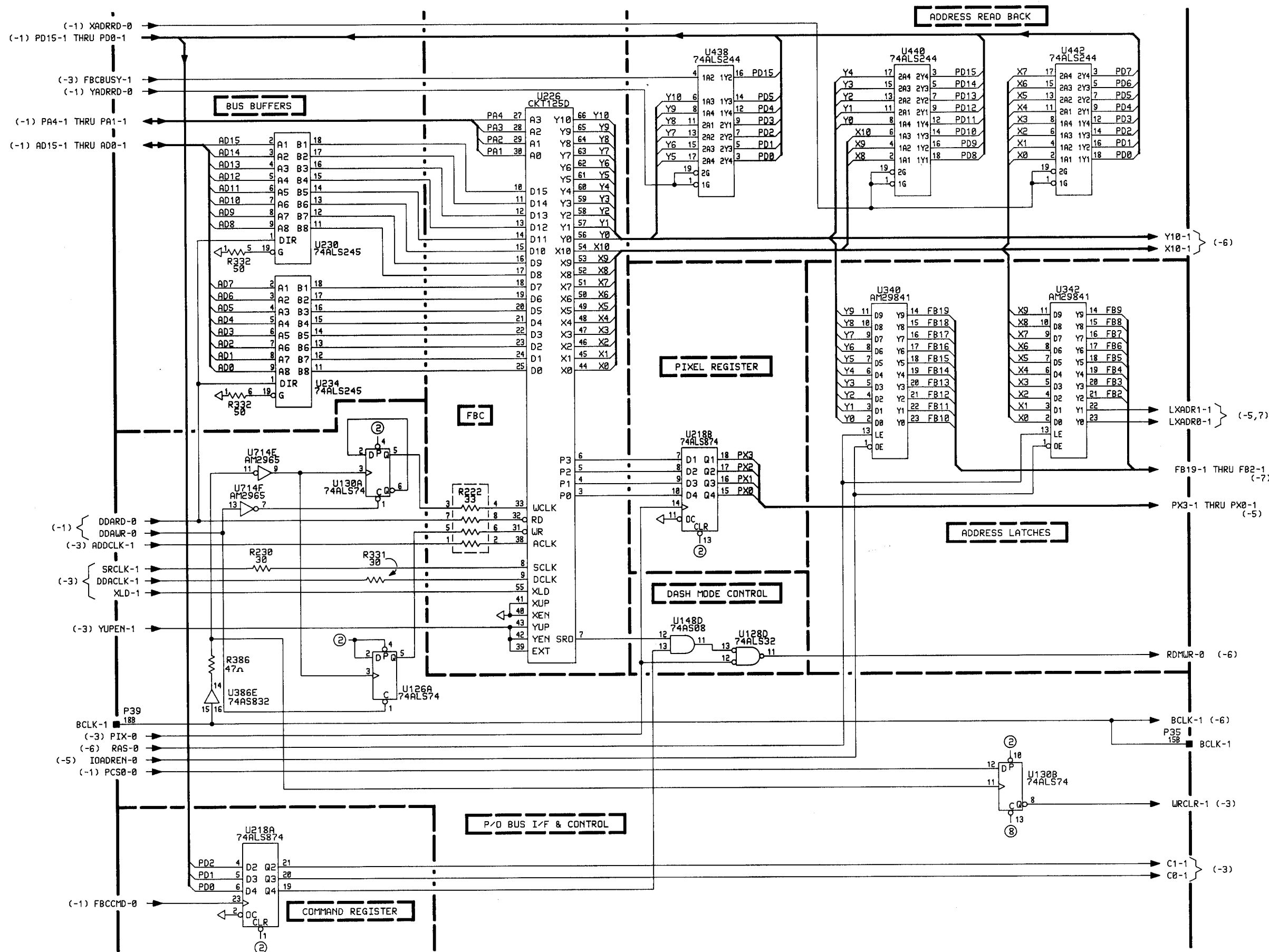




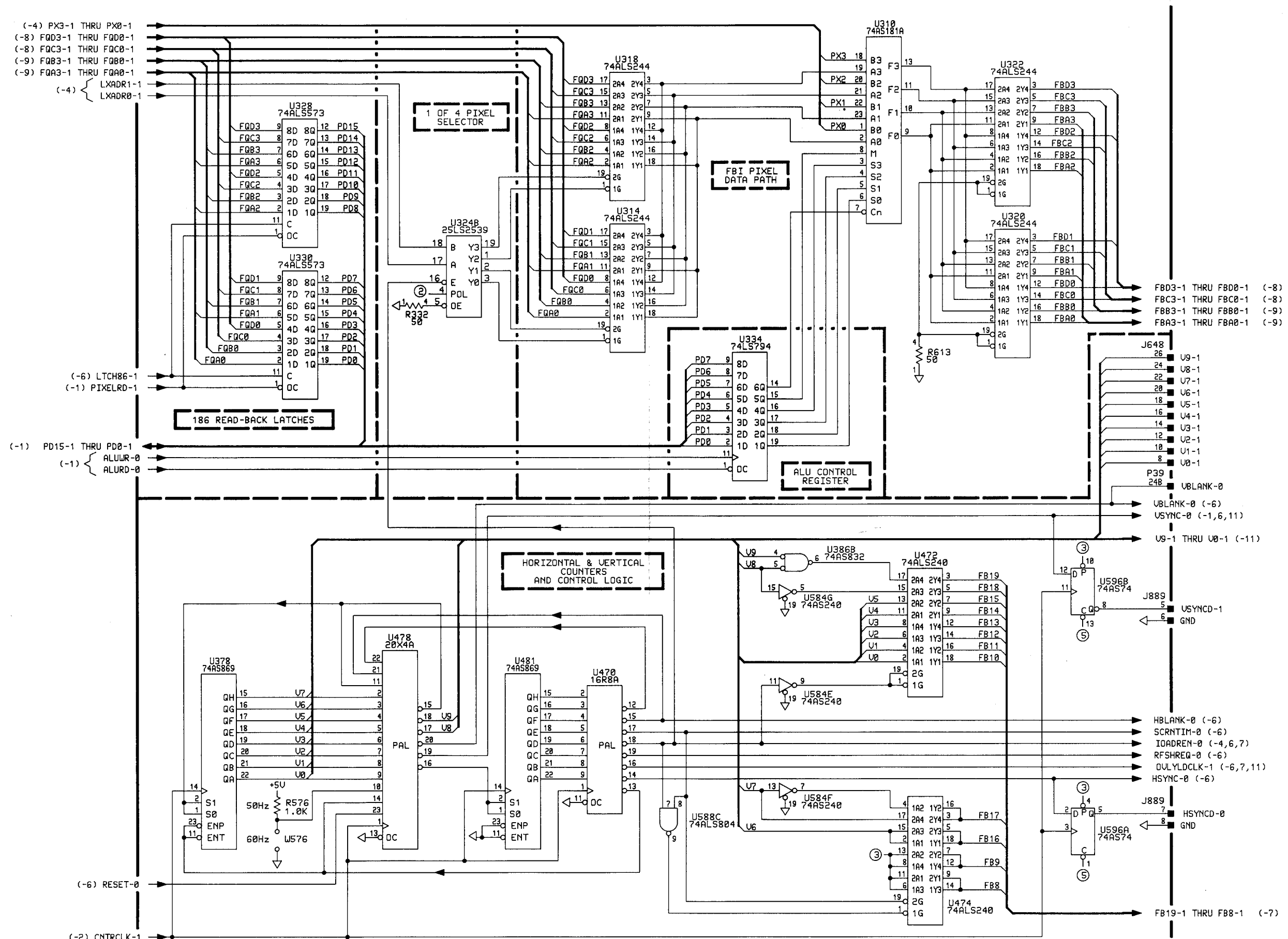


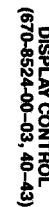



FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00, 01, 02, 03, 40, 41, 42, 43	Tektronix®	ASSEMBLY:
DATE:	REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986			SHEET: 3 OF 13

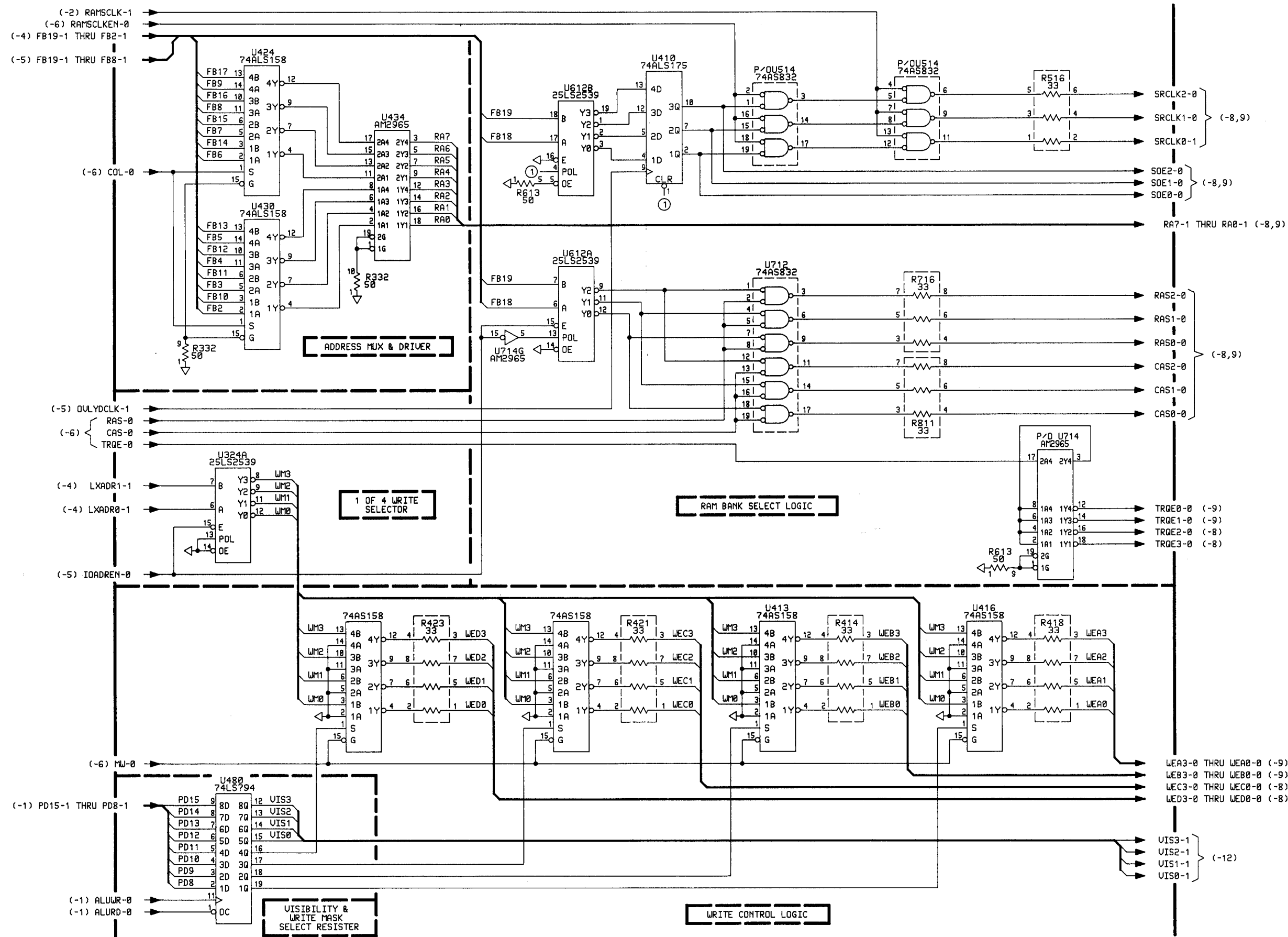


FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00,01,02,03,40,41,42,43	Tektronix®	ASSEMBLY:
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CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986			SHEET: 4 OF 13

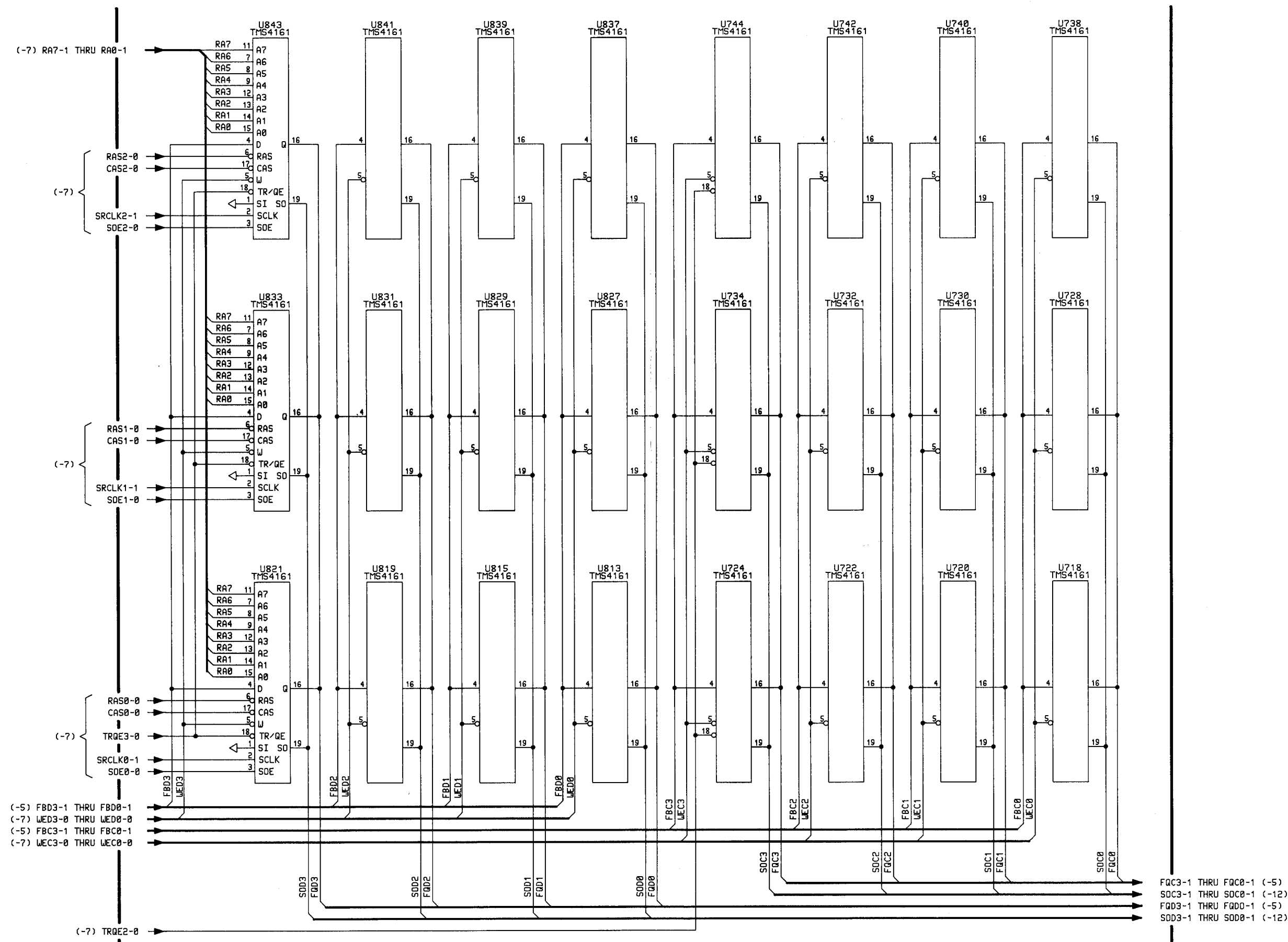




FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00,01,02,03,40,41,42,43	DISPLAY CONTROL BOARD		ASSEMBLY:	
DATE:	REV, 10 MAR 86						CX4111	DSPLCTL
CONTROL NO.:	SSA121.000						TEKTRONIX, INC. © 1986	SHEET: 6 OF 13

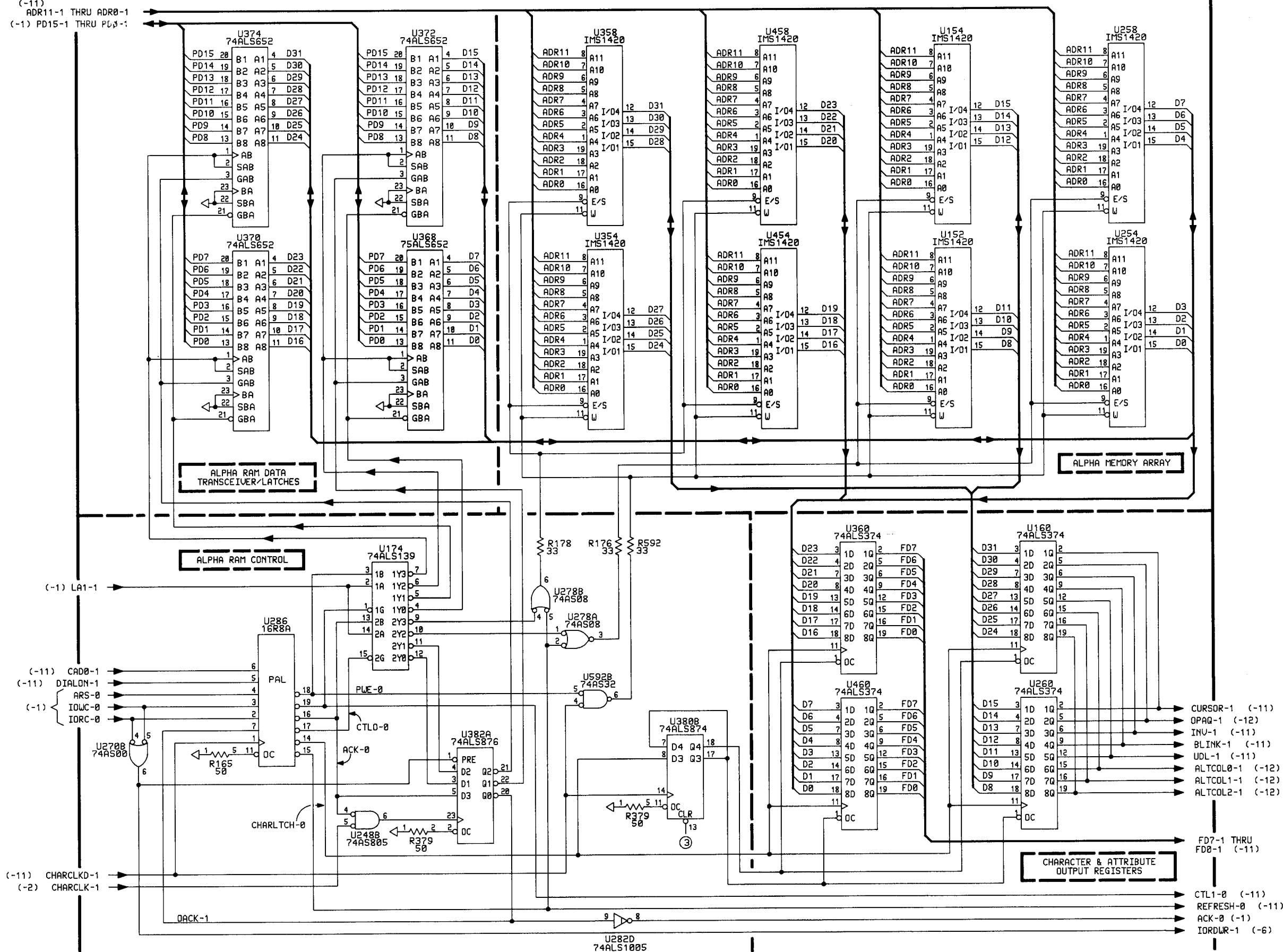


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DATE:	REV, 10 MAR 86	CX4111				DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000				TEKTRONIX, INC. © 1986			SHEET: 7 OF 13

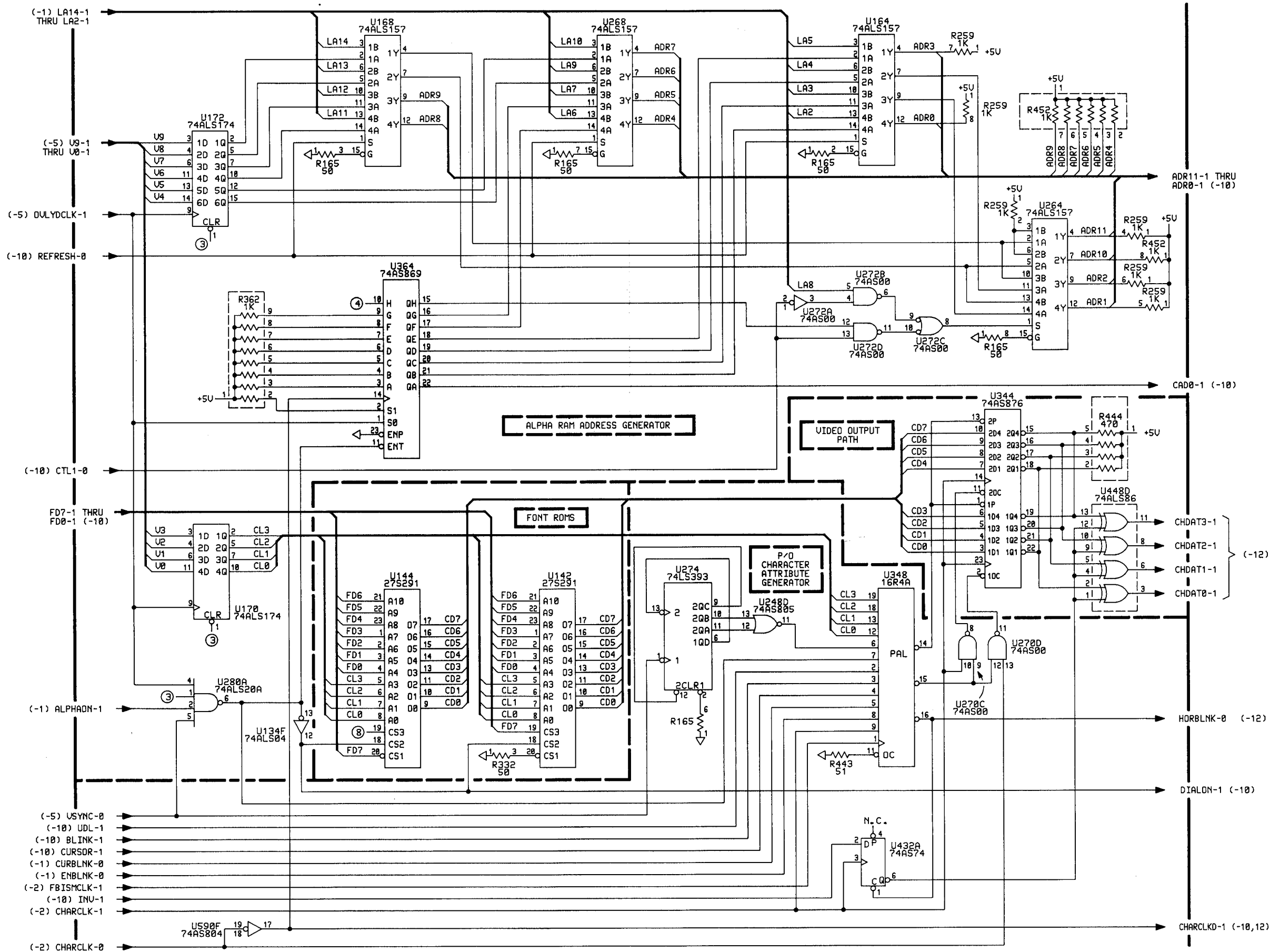


FIRST USE: 4111	OTHER USES:	NOTES:	TITLE: 670-8524-00, 01, 02, 03, 40, 41, 42, 43	ASSEMBLY:
DATE: REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.: SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 8 OF 13

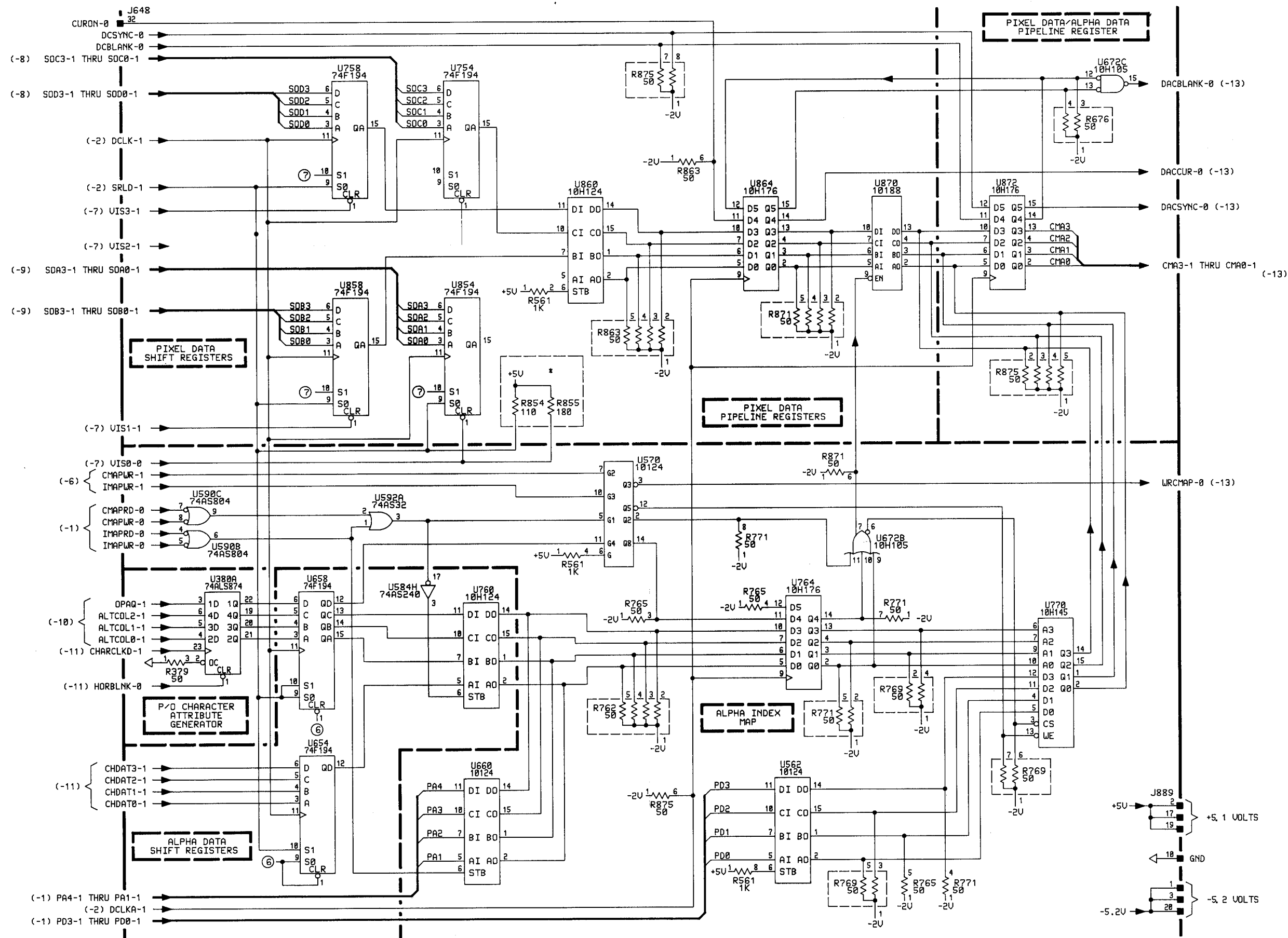
(-11)
ADR11-1 THRU ADR0-1
(-1) PD15-1 THRU PD0-1



FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00, 01, 02, 03, 40, 41, 42, 43	ASSEMBLY:
DATE:	REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 10 OF 13

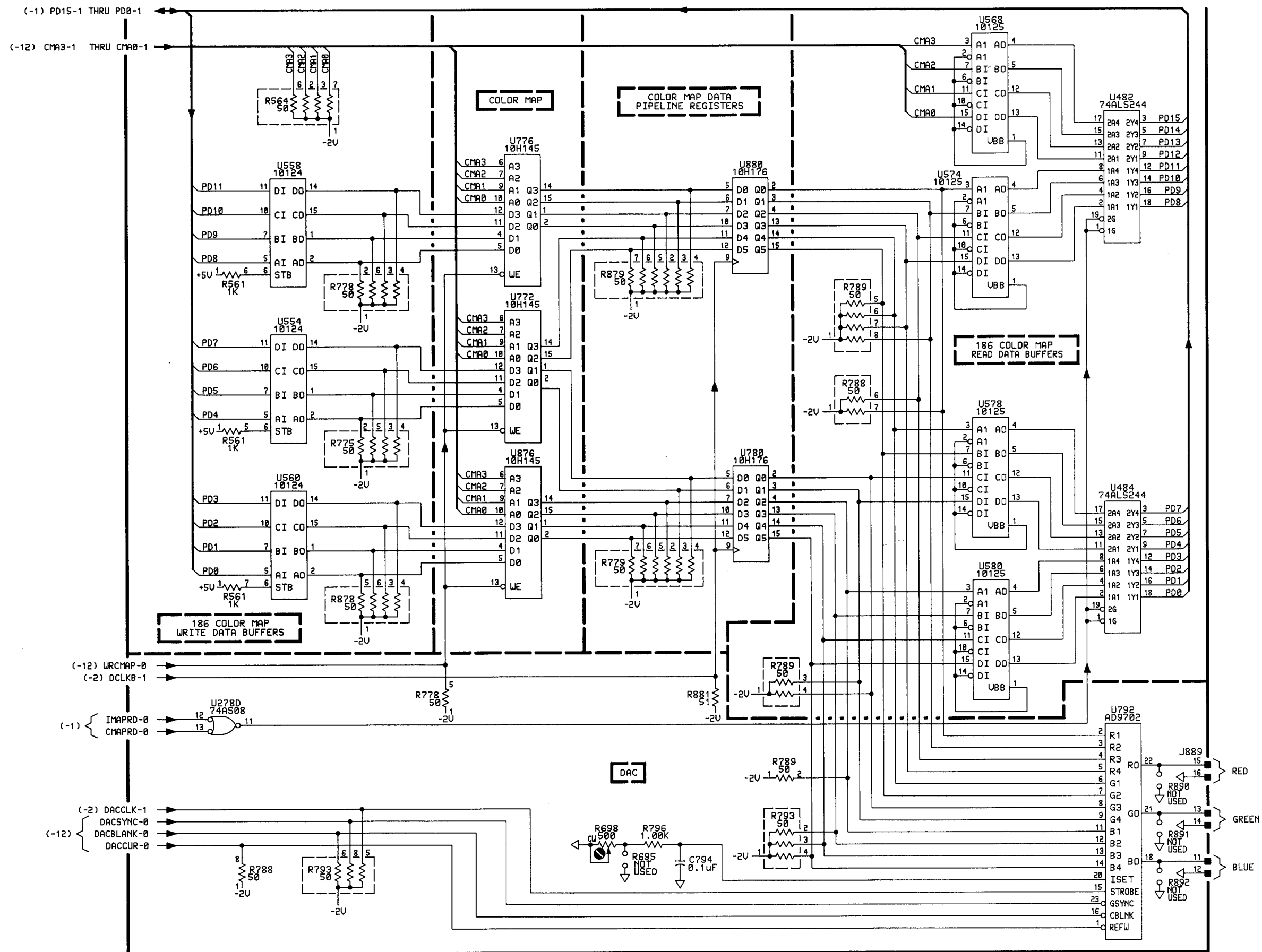


FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00,01,02,03,40,41,42,43	Tektronix®	ASSEMBLY:
DATE:	REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986			SHEET: 11 OF 13

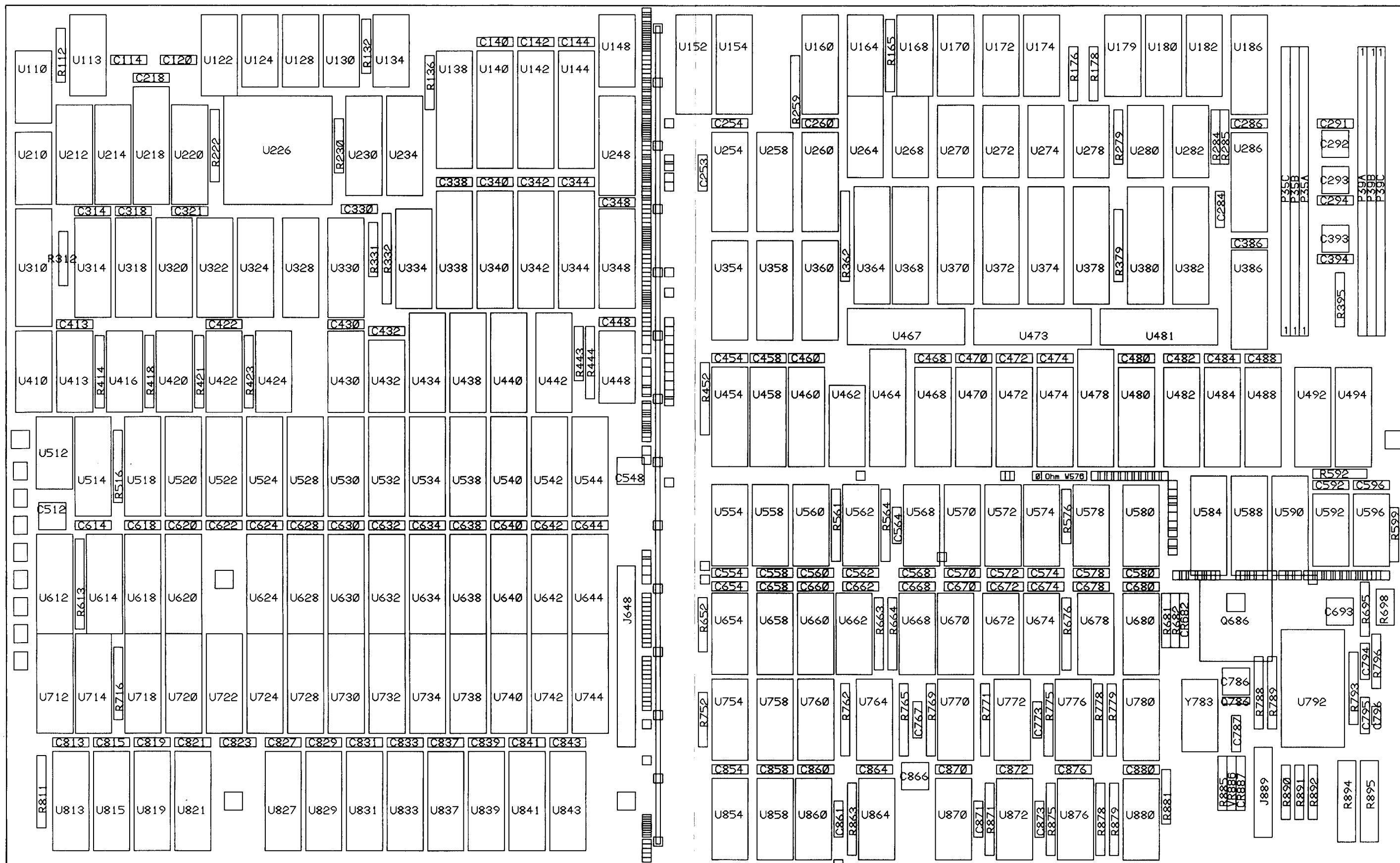


FIRST USE:	4111	OTHER USES:	NOTES: * 670-8524-03/43 INCLUDES THESE RESISTORS.	TITLE: 670-8524-00,01,02,03,40,41,42,43	ASSEMBLY:
DATE:	REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 12 OF 13

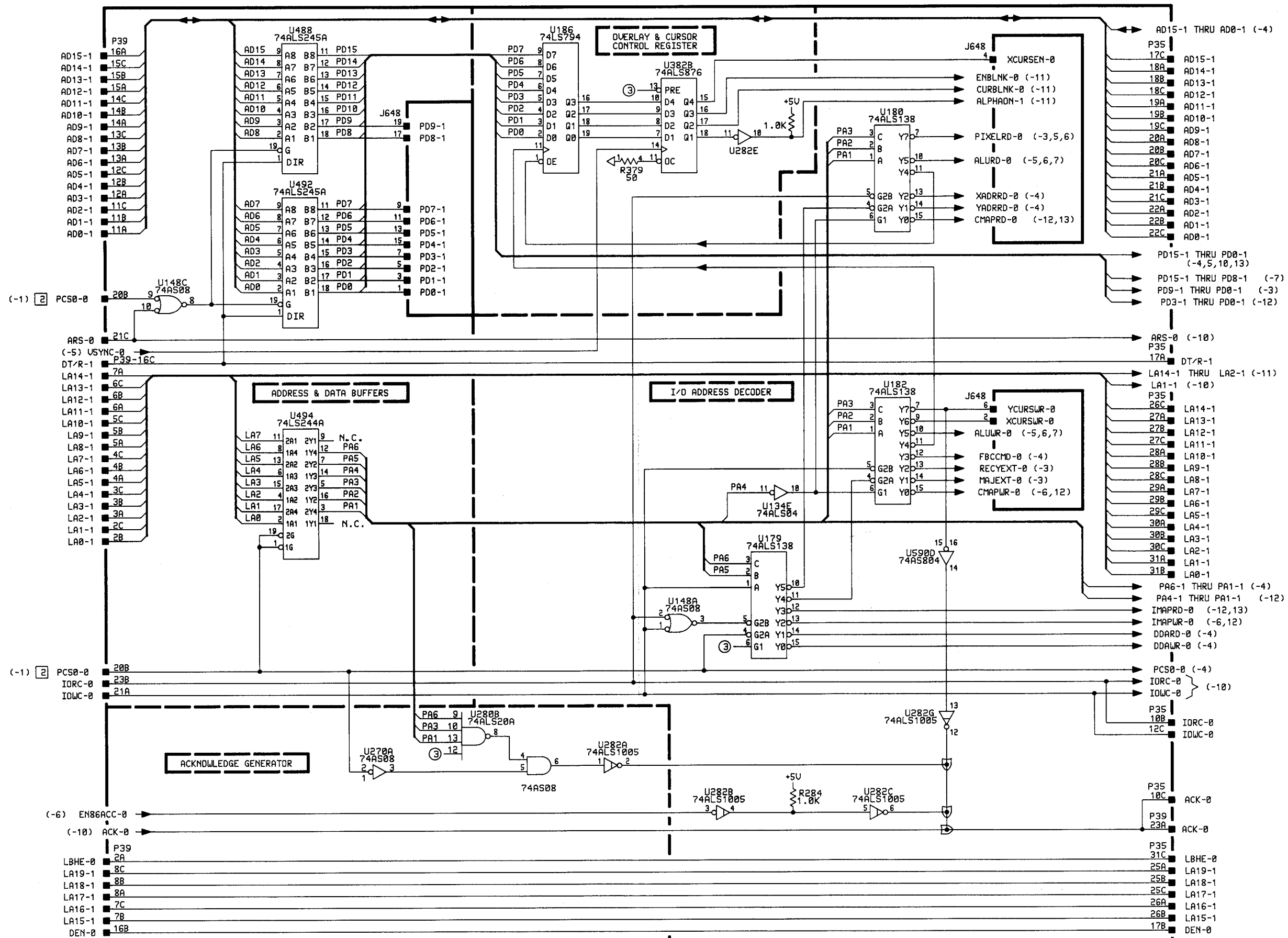
DISPLAY CONTROL BOARD
DSPLCTL-12



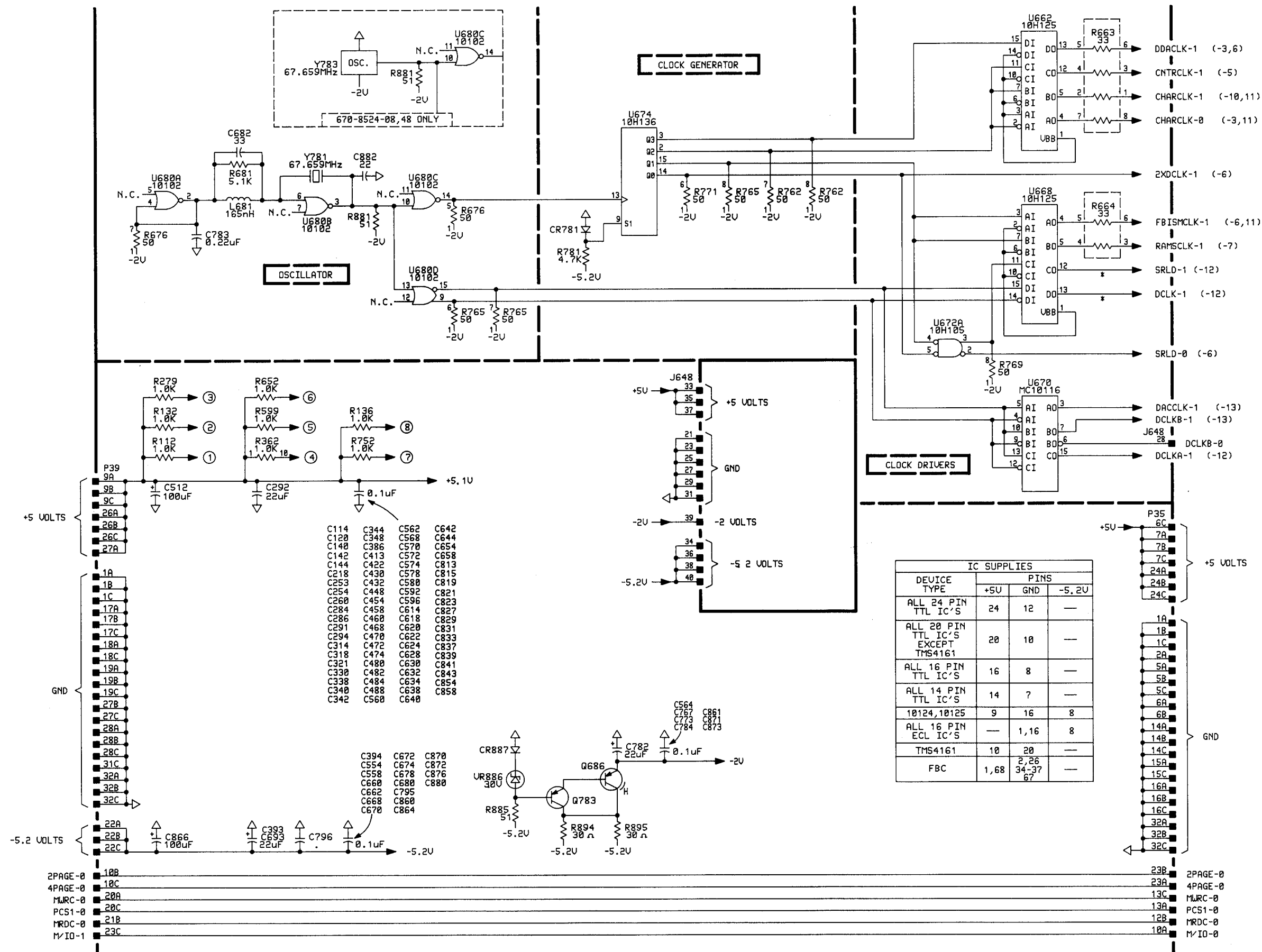
FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-00, 01, 02, 03, 40, 41, 42, 43		ASSEMBLY:
DATE:	REV, 10 MAR 86	CX4111		DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986			SHEET: 13 OF 13

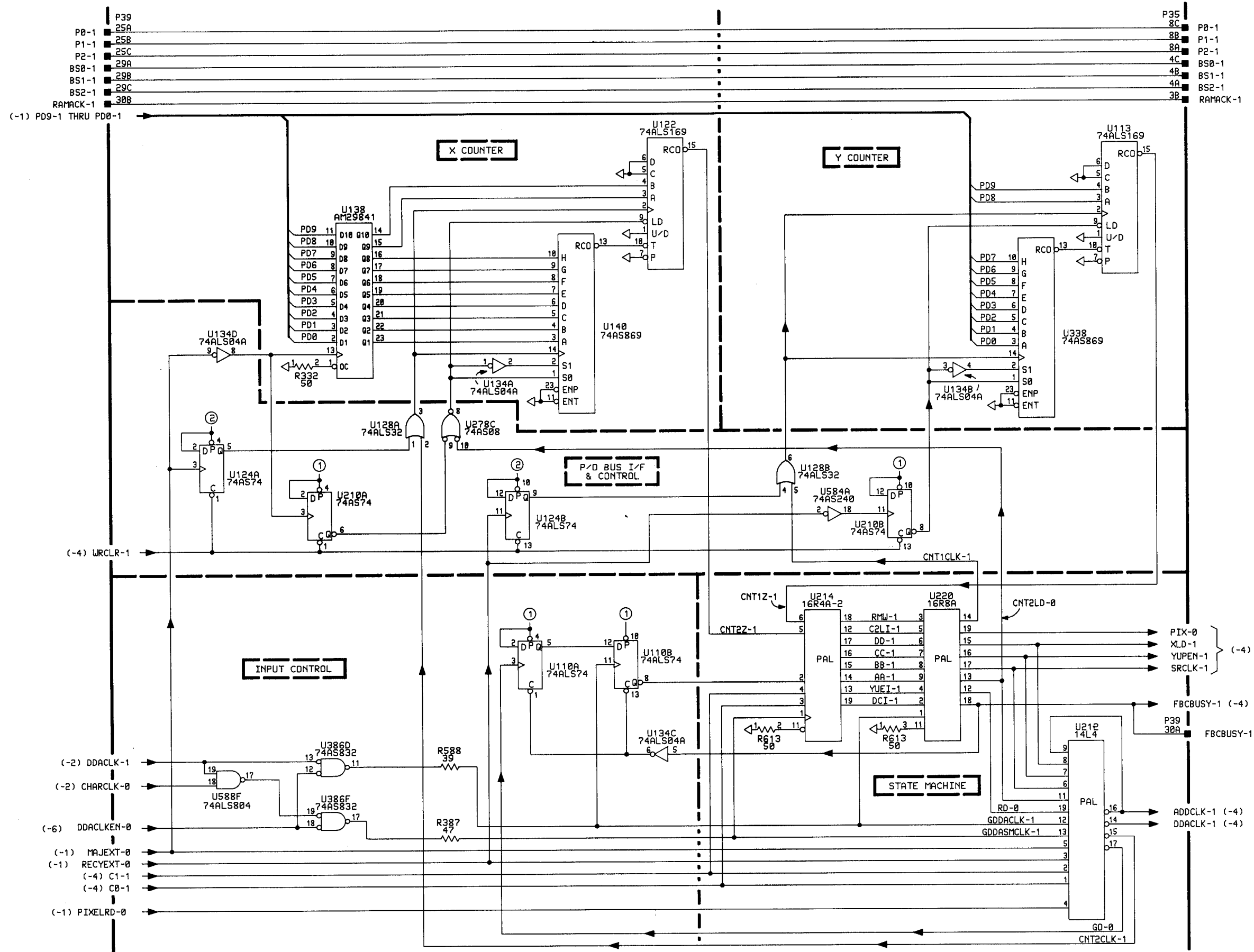


Display Control Component Locations (670-8524-04-08, 44-48).

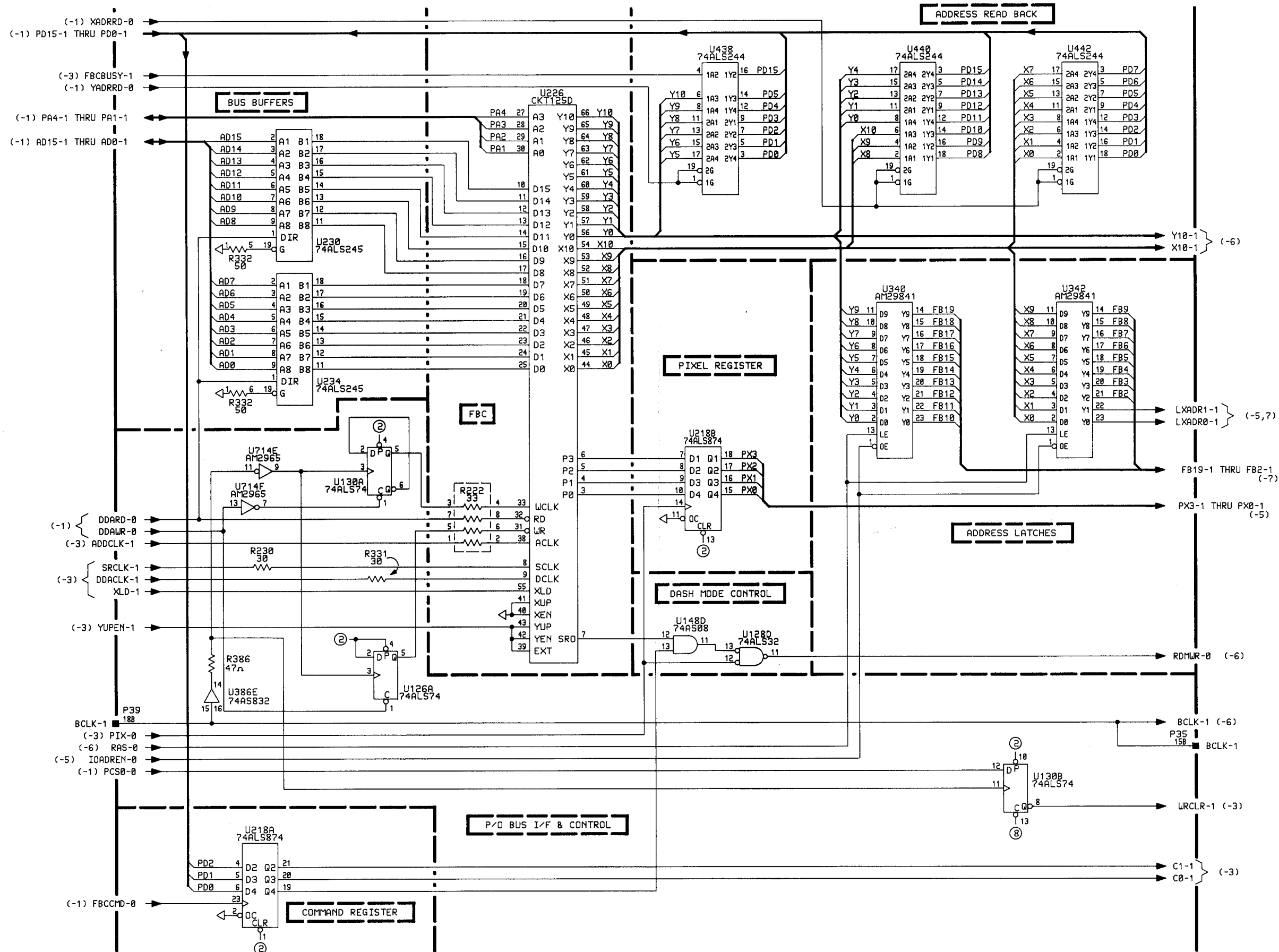


FIRST USE:	4111	OTHER USES:	NOTES: <input type="checkbox"/> INDICATES SHOWN MORE THAN ONCE & WHERE (-)	TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 1 OF 13





FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48	Tektronix®	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111		DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986			SHEET: 3 OF 13

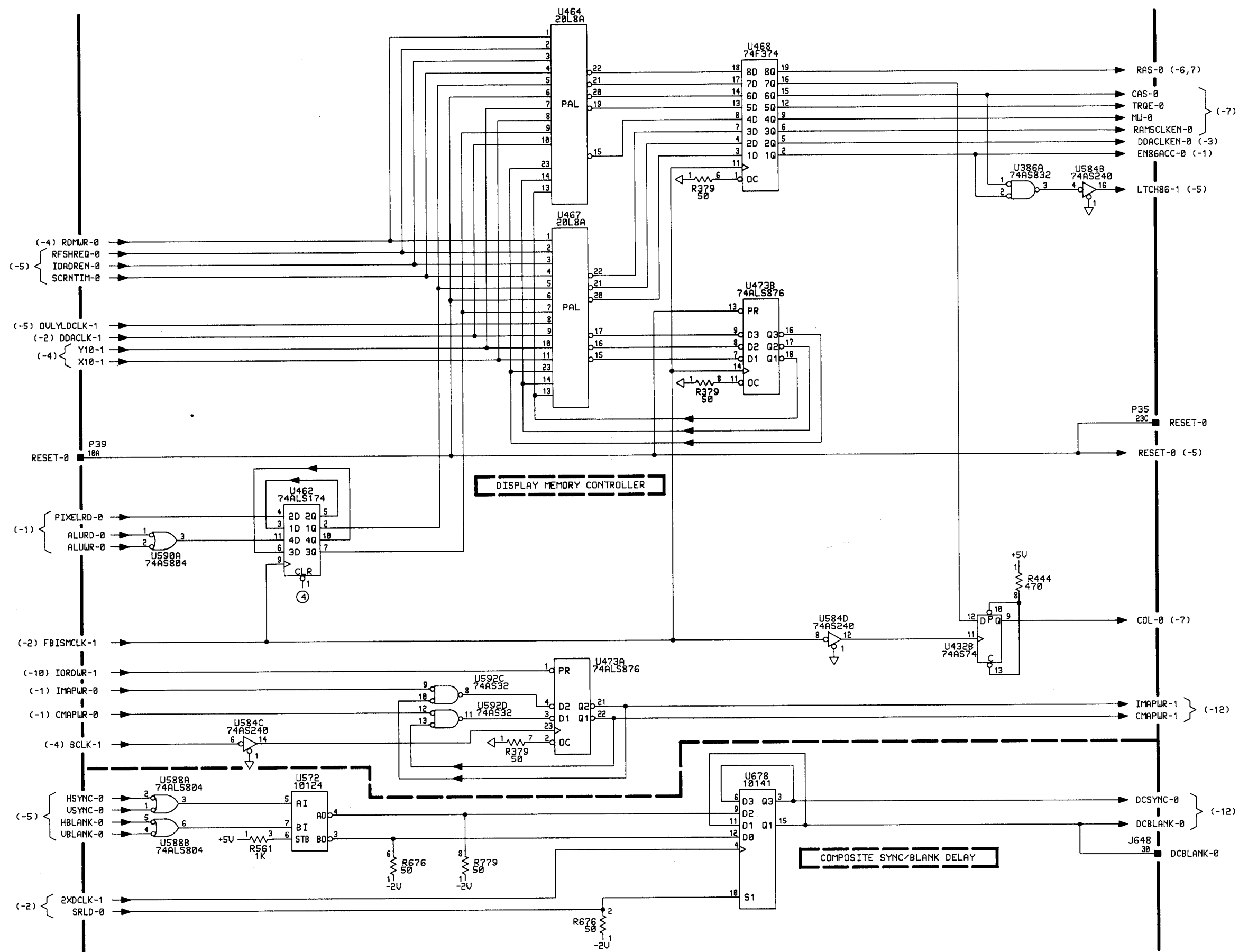


FIRST USE:	4111	OTHER USES:		NOTES:		TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111				DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000				TEKTRONIX, INC. © 1986		SHEET: 4 OF 13

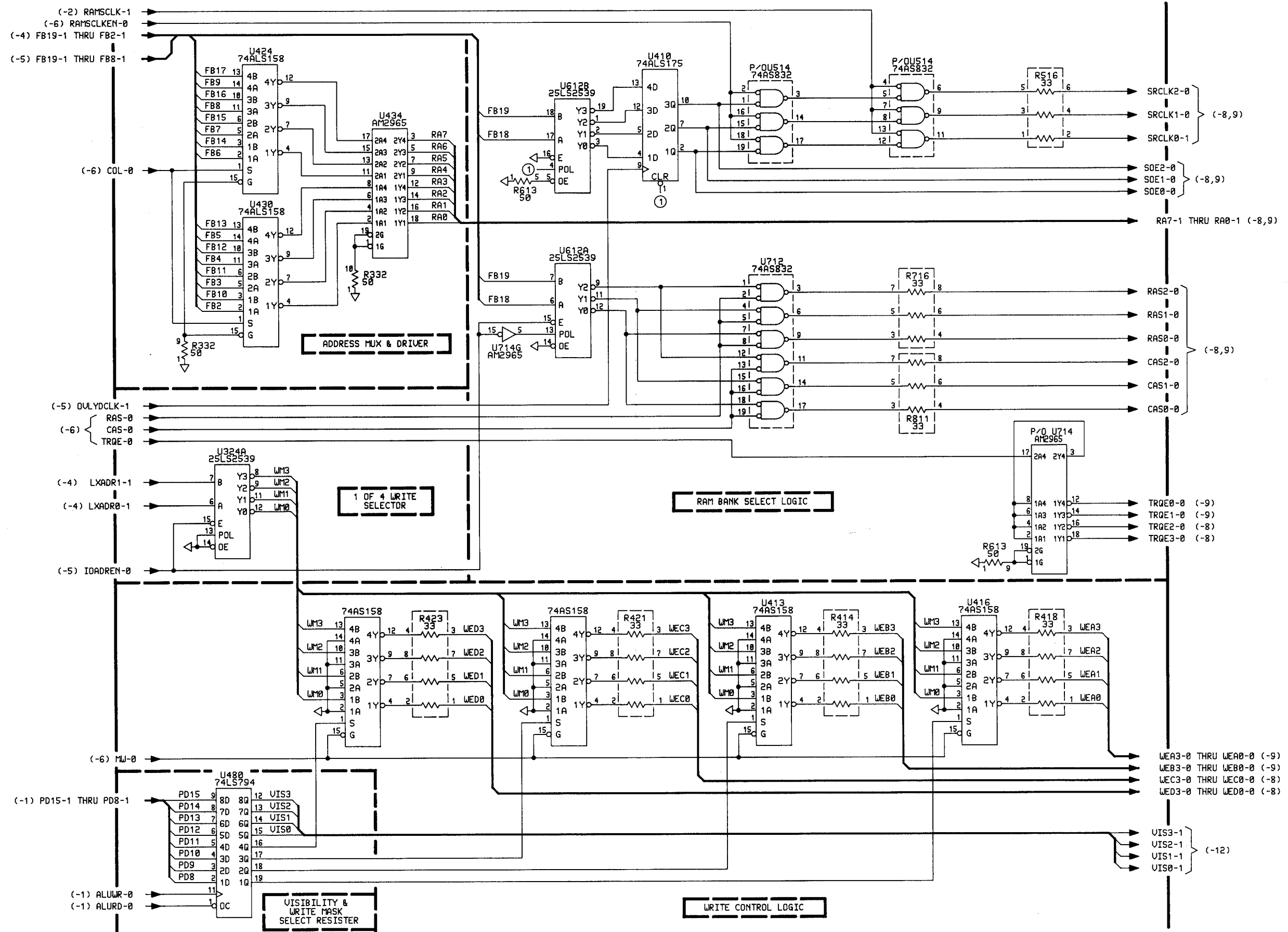


DISPLAY CONTROL
(670-8524-04-08, 44-48)

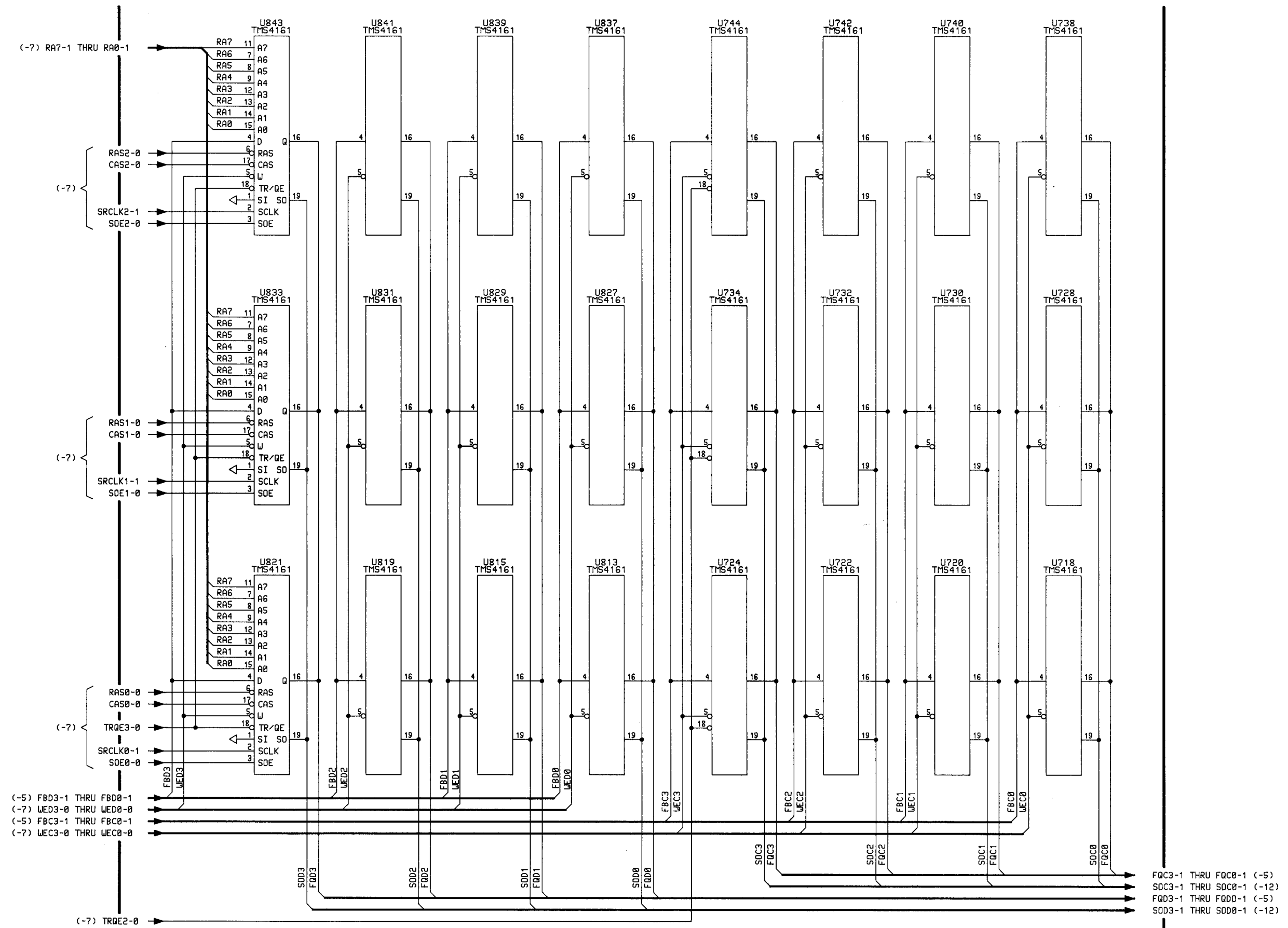
DSP LCTL-5

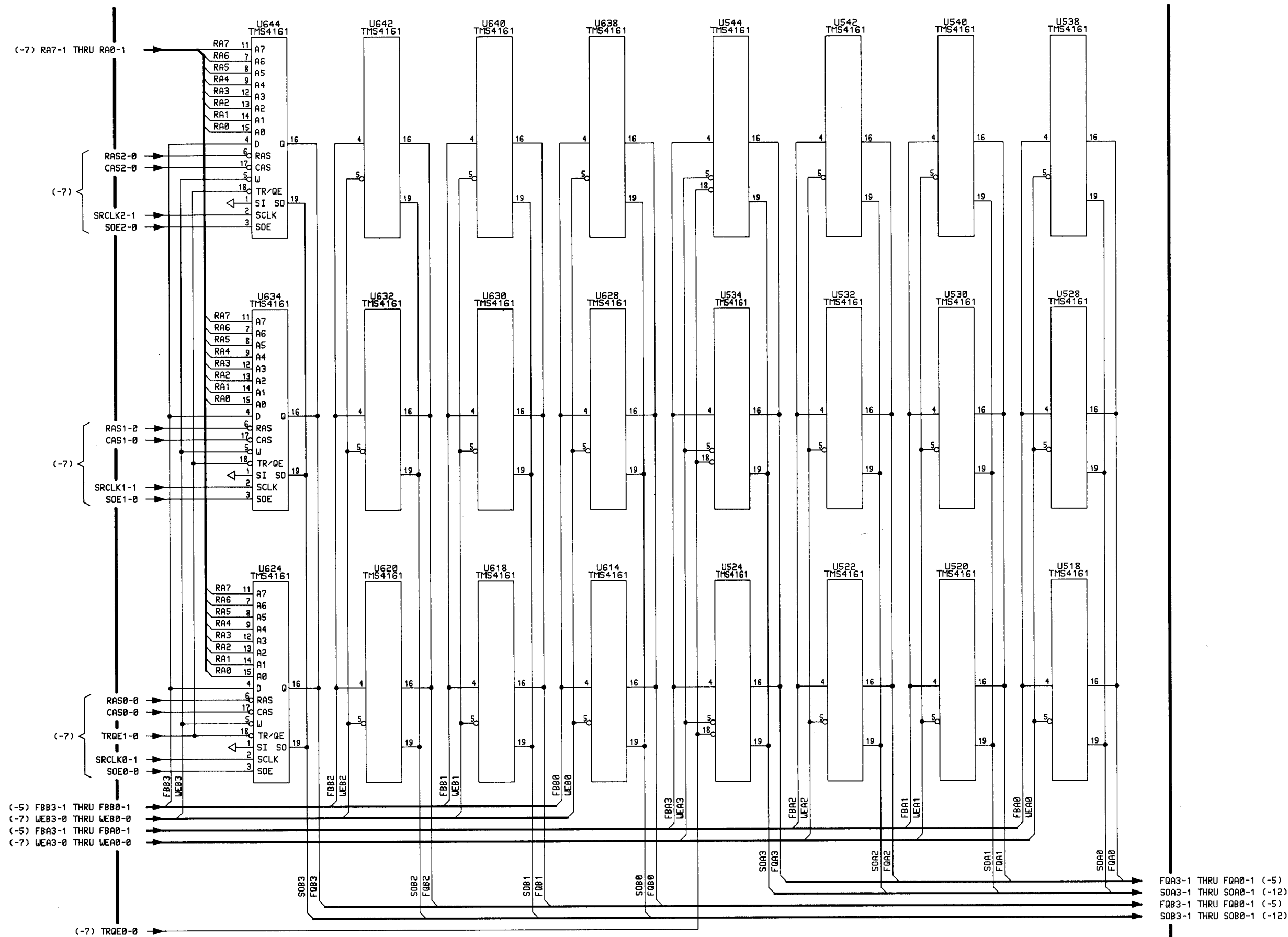


FIRST USE:	4111	OTHER USES:		NOTES:		TITLE: 670-8524-04, 05, 06, 07, 08, 44, 45, 46, 47, 48	Tektronix®	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111				DISPLAY CONTROL BOARD		DSPLCTL
CONTROL NO.:	SSA121.000				TEKTRONIX, INC. © 1986			SHEET: 6 OF 13

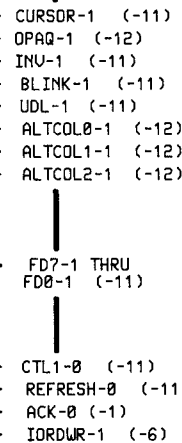


FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 7 OF 13

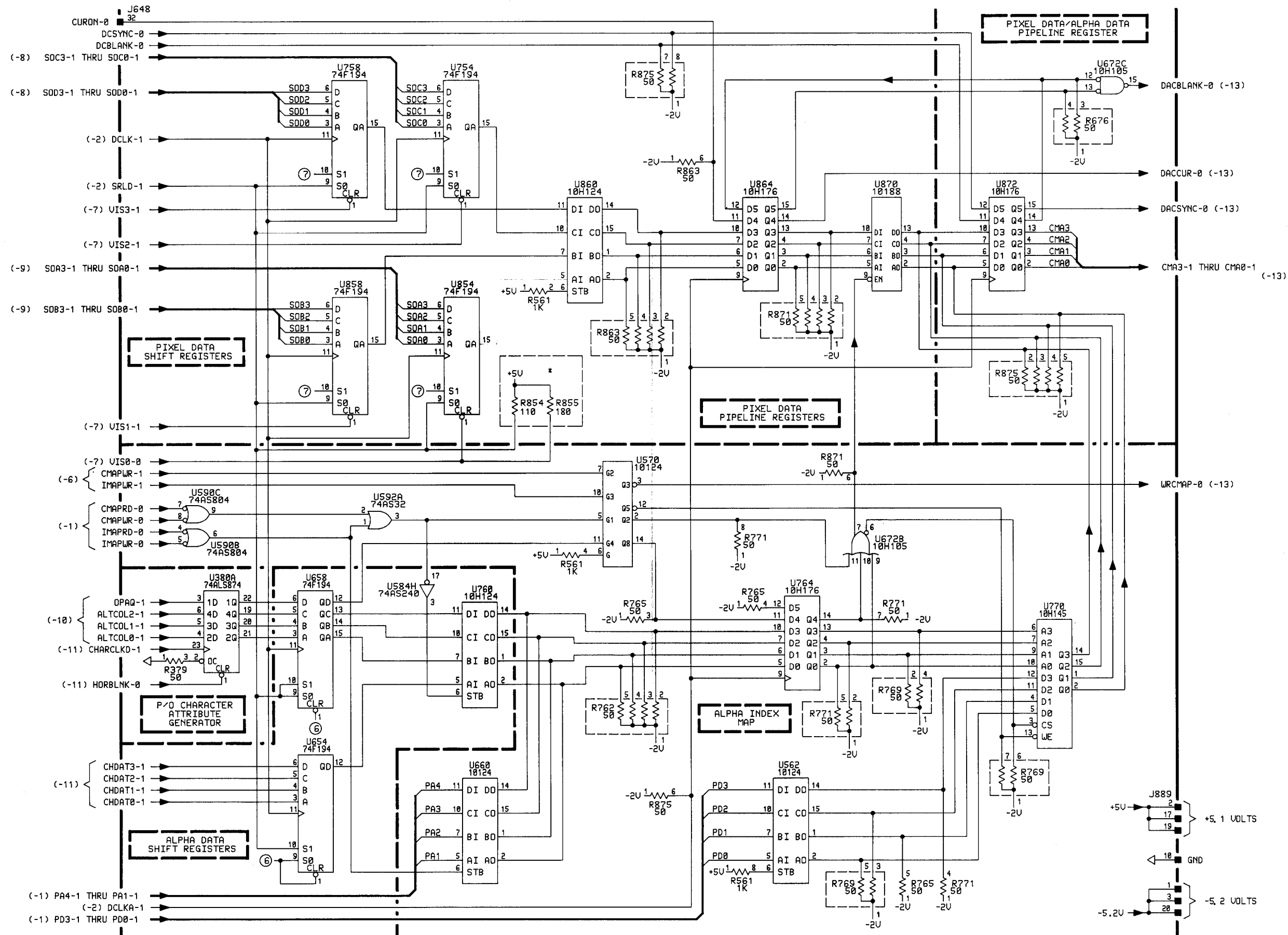




FIRST USE: 4111	OTHER USES:	NOTES:	TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48	ASSEMBLY:
DATE: REV, 13 JUN 1986	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.: SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 9 OF 13



Tektronix®



FIRST USE: 4111
 DATE: REV, 13 JUN 1986
 CONTROL NO.: SSA121.000

OTHER USES:
 CX4111

NOTES: * 670-8524-03/43 INCLUDES THESE RESISTORS.

TEKTRONIX, INC. © 1986

TITLE: 670-8524-04,05,06,07,08,44,45,46,47,48

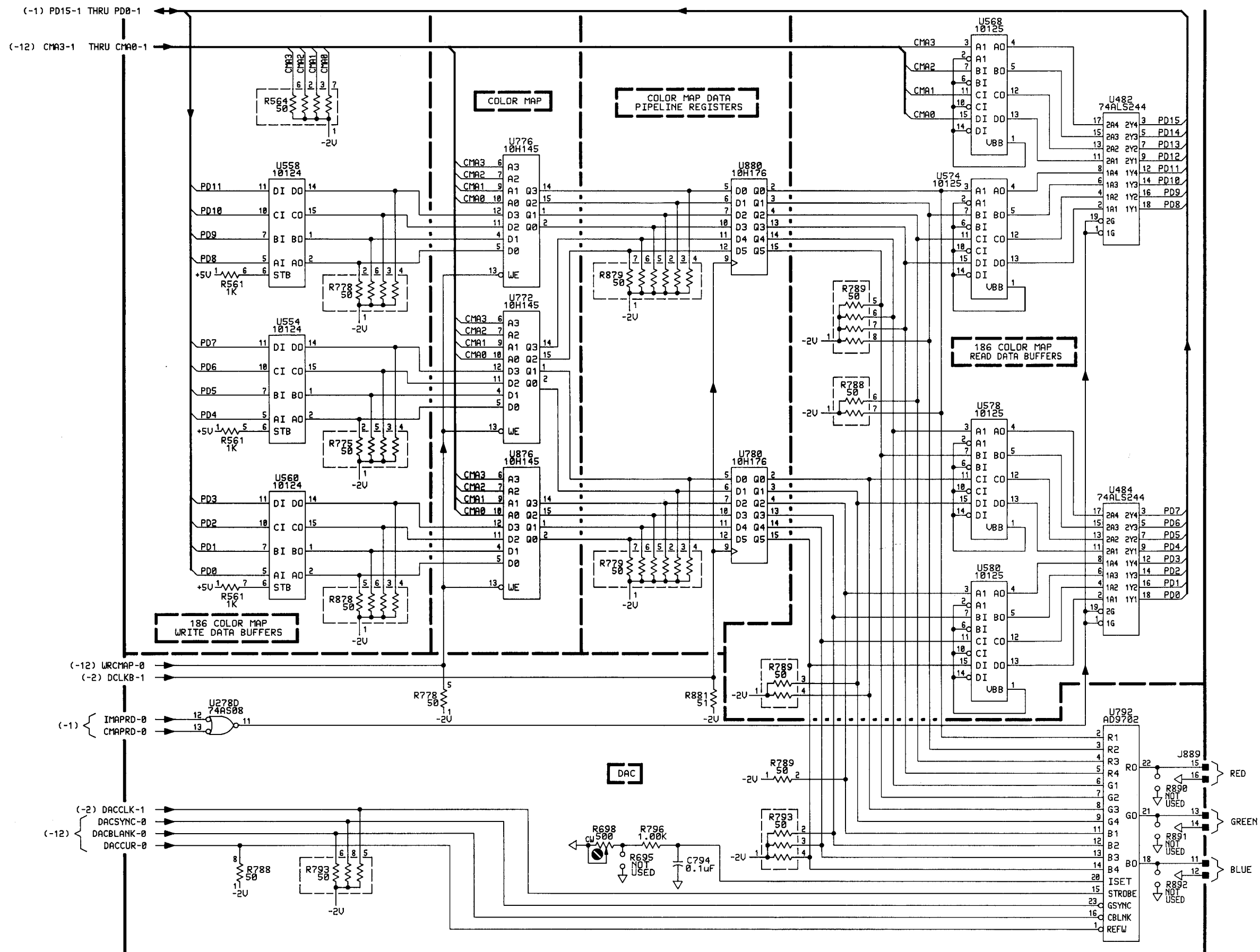
DISPLAY CONTROL BOARD

Tektronix®

ASSEMBLY:
 DSPLCTL
 SHEET: 12 OF 13

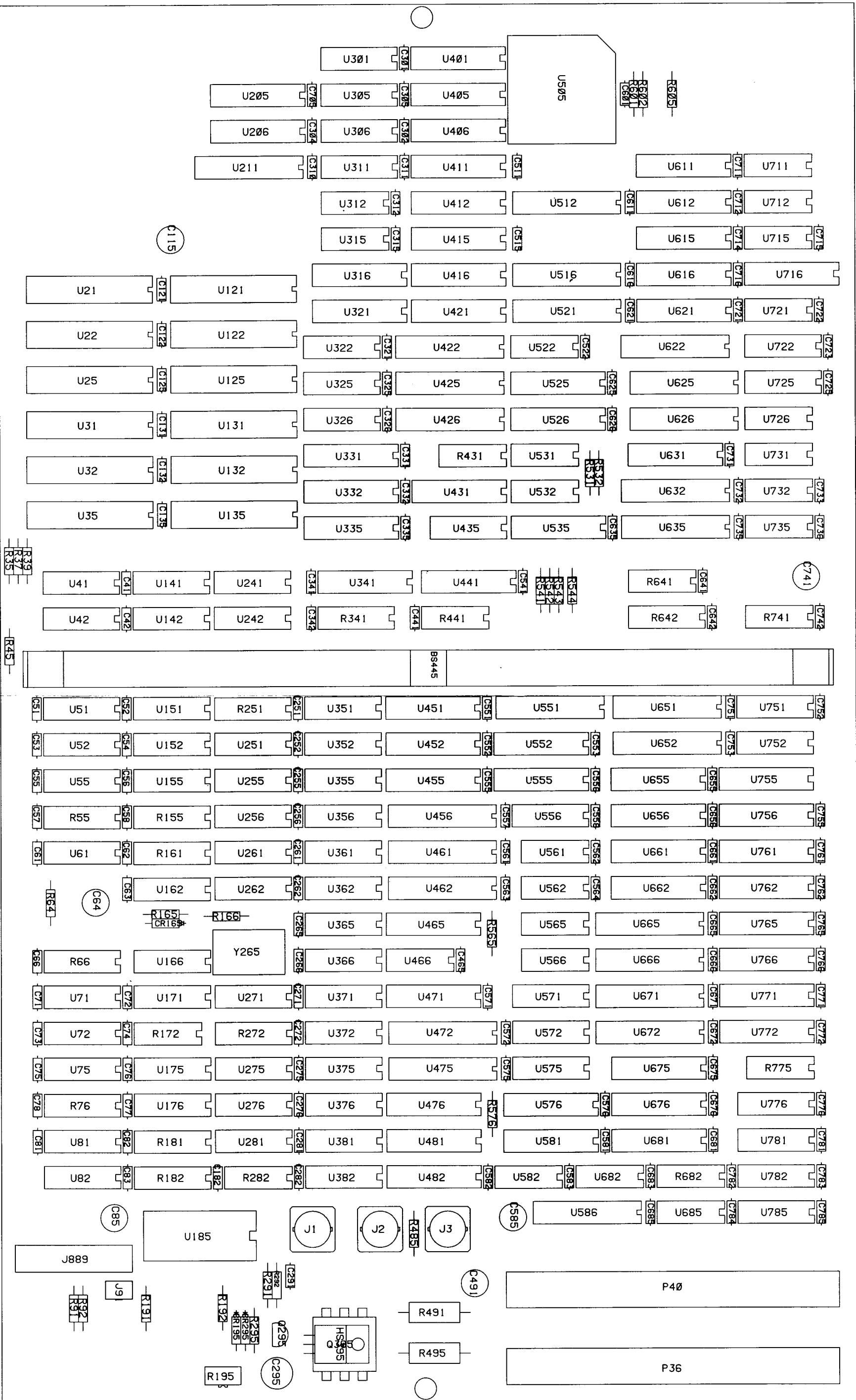
DISPLAY CONTROL
 (670-8524-04-06,44-48)

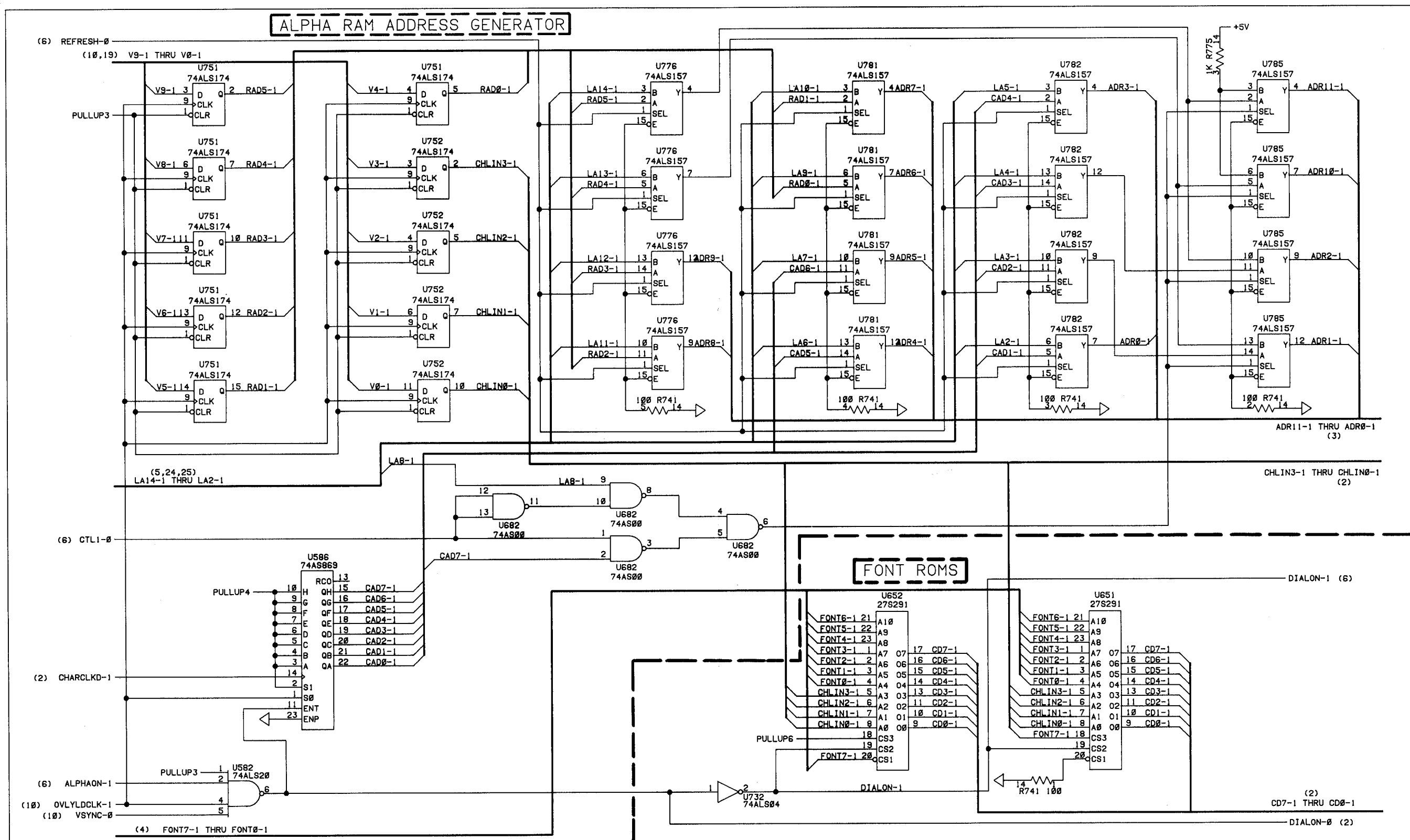
DSPLCTL-12



FIRST USE:	4111	OTHER USES:	NOTES:	TITLE: 670-8524-04, 05, 06, 07, 08, 44, 45, 46, 47, 48	ASSEMBLY:
DATE:	REV, 13 JUN 1986	CX4111		DISPLAY CONTROL BOARD	DSPLCTL
CONTROL NO.:	SSA121.000		TEKTRONIX, INC. © 1986		SHEET: 13 OF 13

Display Control Component Locations (670-9725-00).





REVISION DATE:

PLOT DATE: 06-03-86

ARTWORK NUMBER:

NOTES: PULLUP RESISTORS ARE ON PAGE 26.

PCB NUMBER: UA923801

TEKTRONIX®

TEKTRONIX INC. © 1986

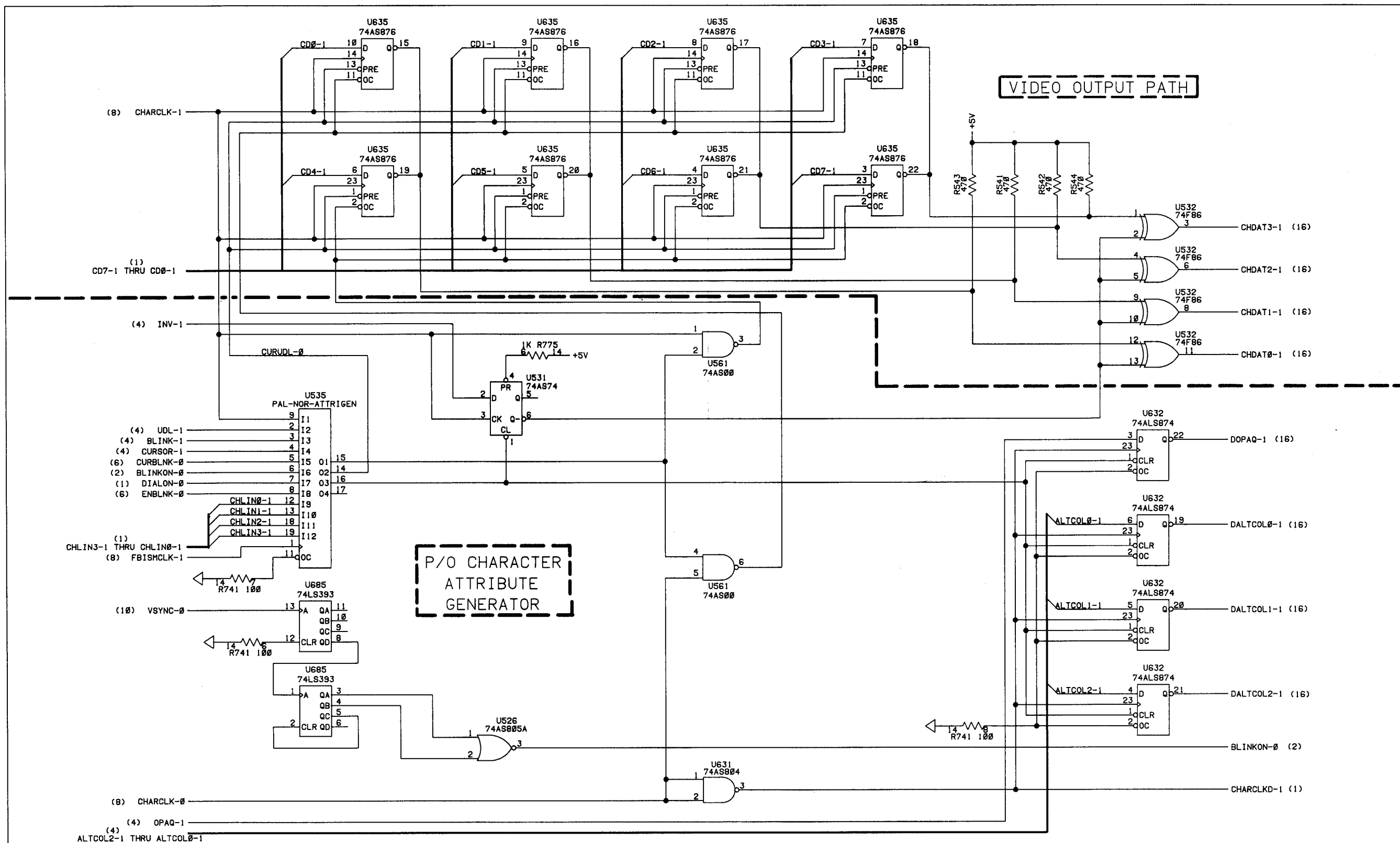
BOARD NUMBER: 670-9725-00

TITLE:

DISPLAY CONTROL BOARD

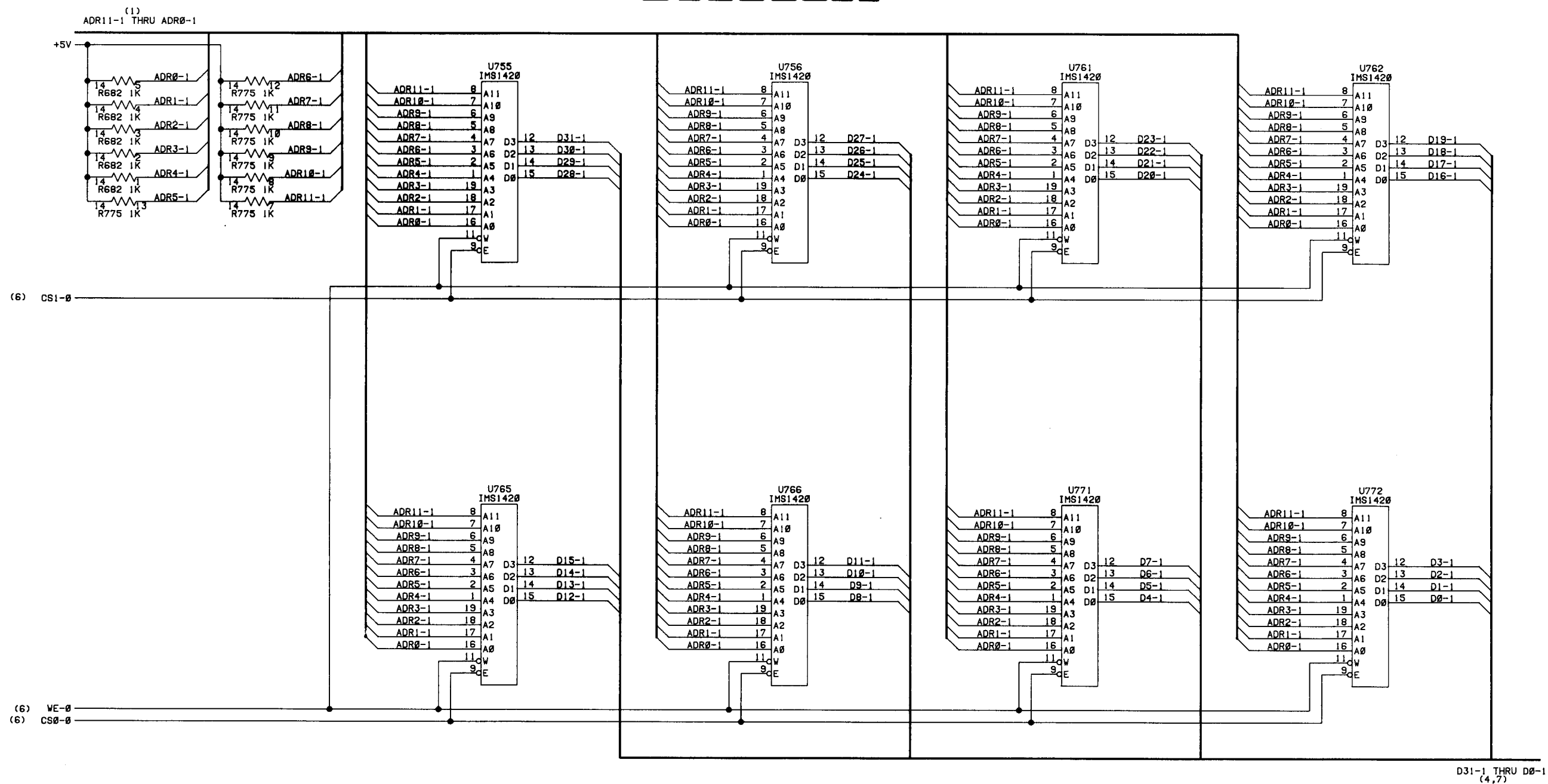
SHEET:

1 of 26



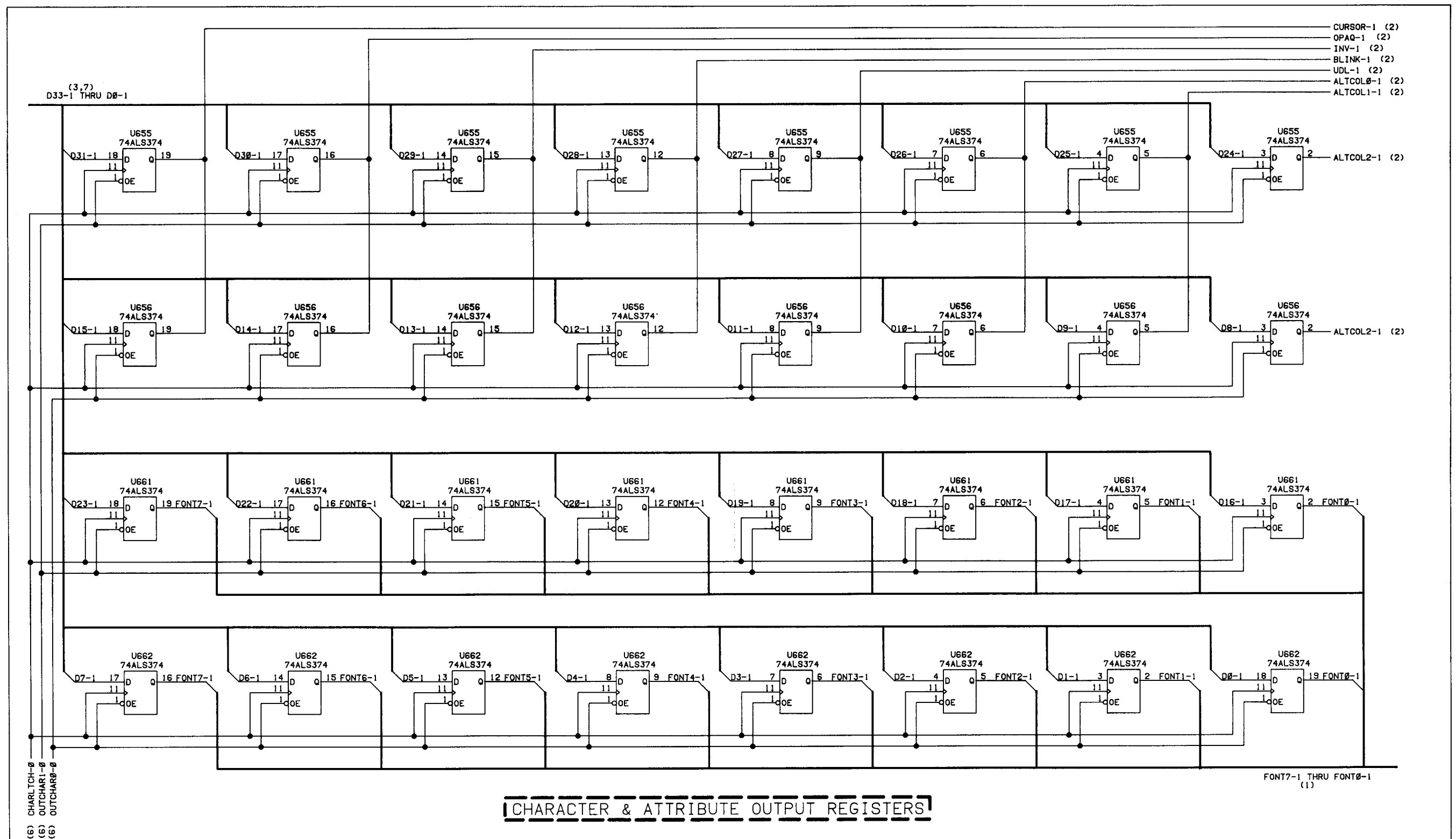
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	2 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	

ALPHA MEMORY ARRAY

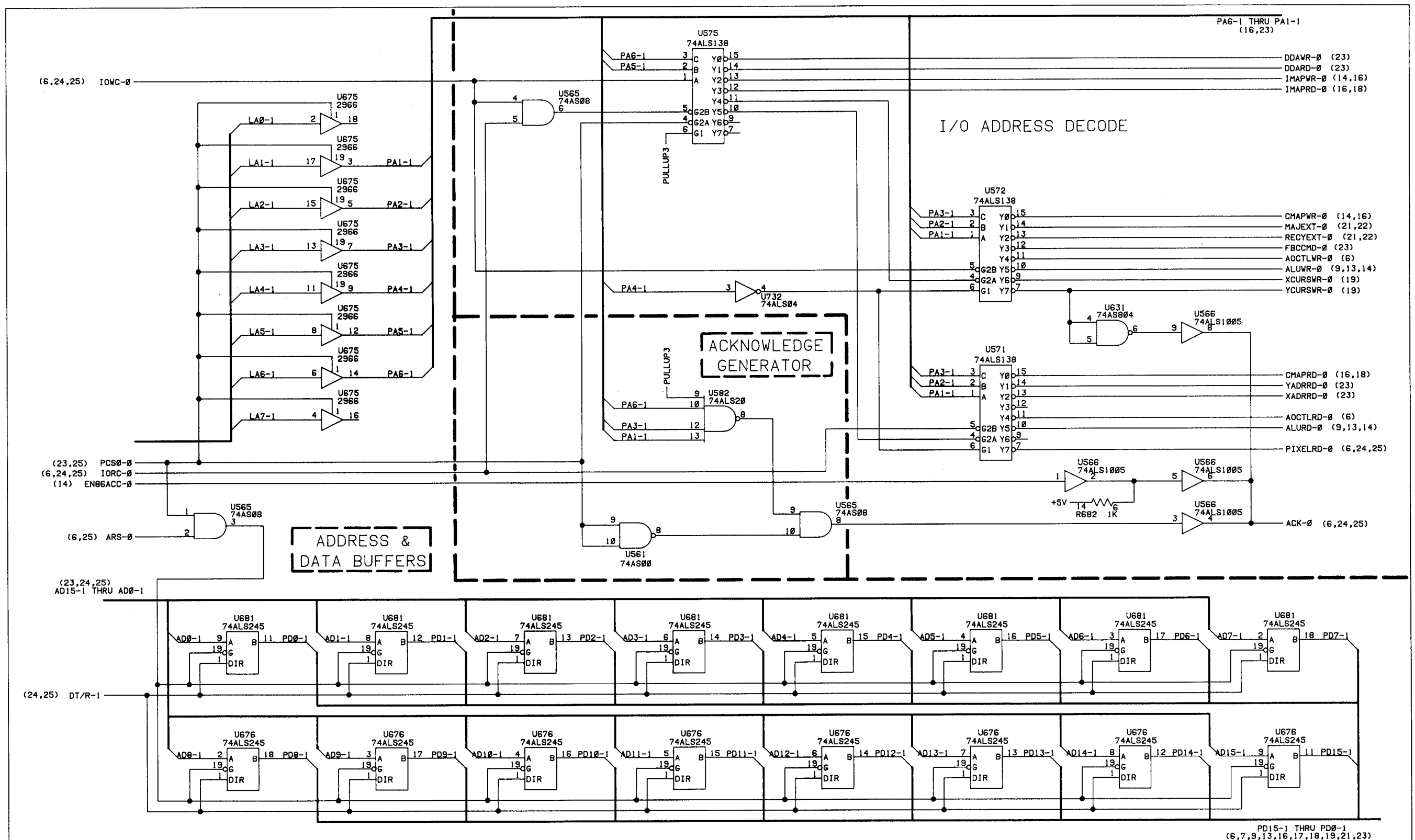


D31-1 THRU DØ-1
(4,7)

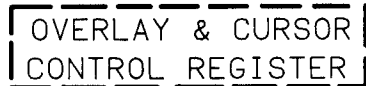
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET: 3 of 26
PLOT DATE: 06-03-86			TITLE:	
ARTWORK NUMBER:			PCB NUMBER: UA923801	



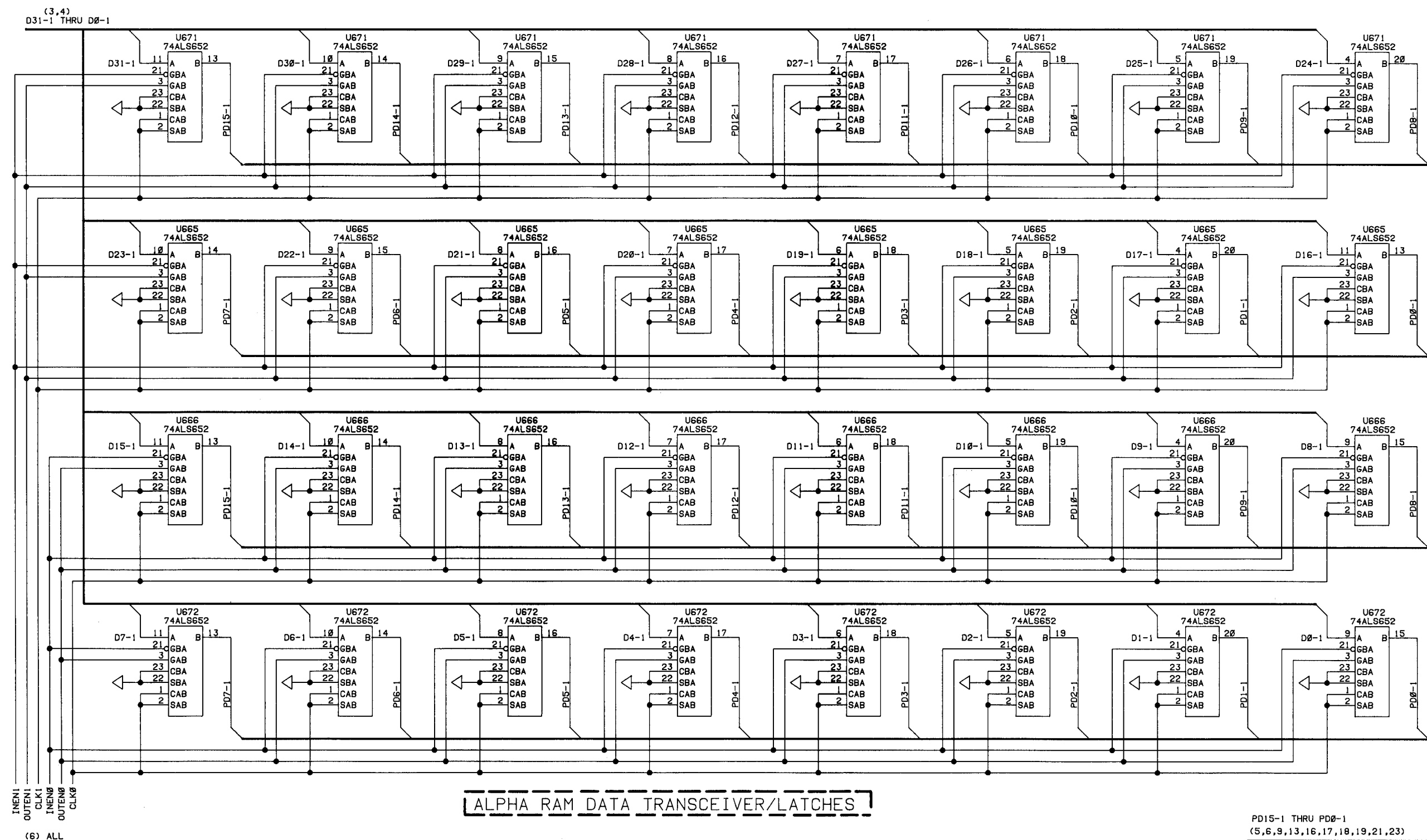
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	4 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



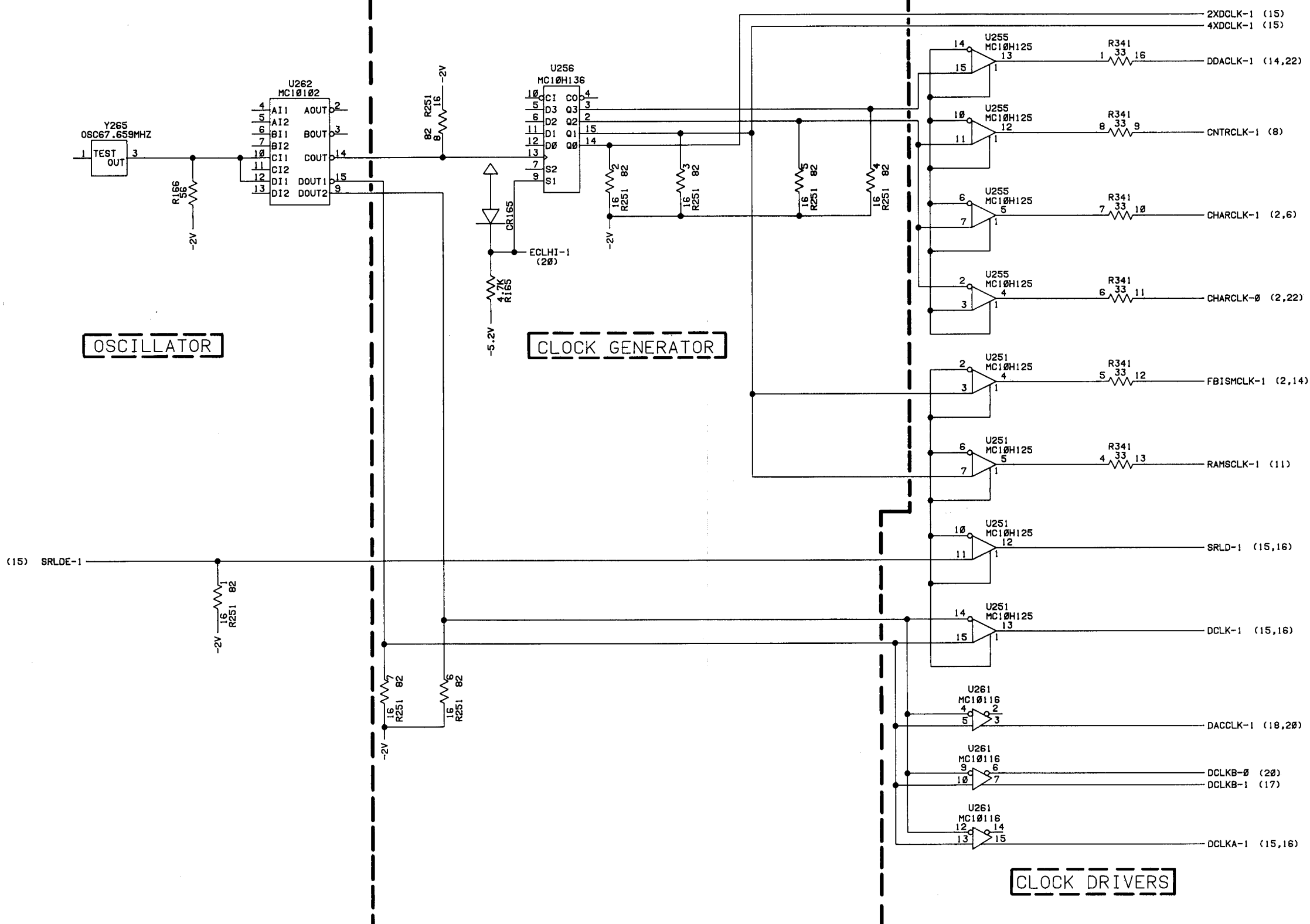
REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHT 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE: DISPLAY CONTROL BOARD	5 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986		



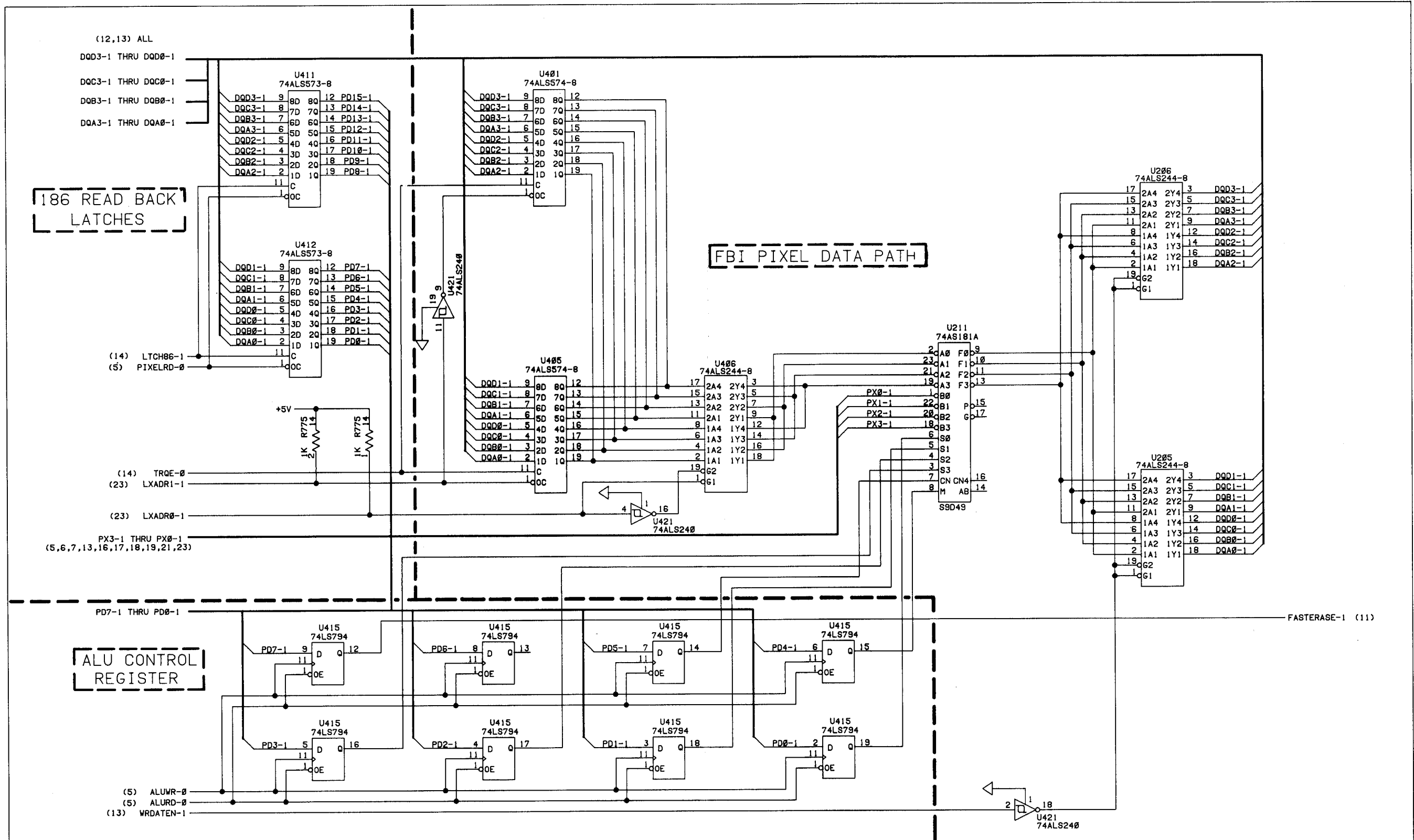
REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	6 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	7 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



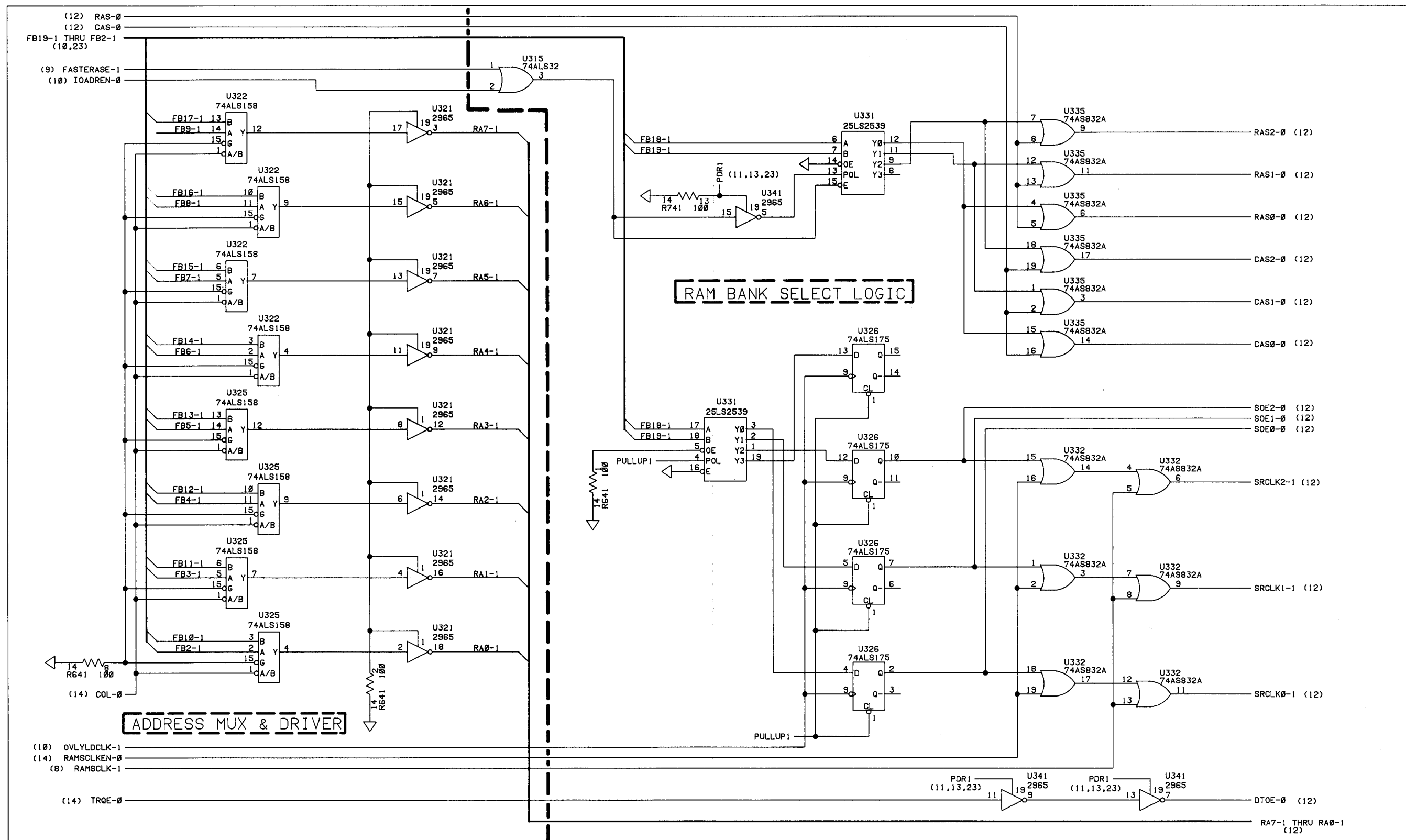
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-16-86			TITLE:	8 of 26
ARTWORK NUMBER:	PCB NUMBER: UB923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



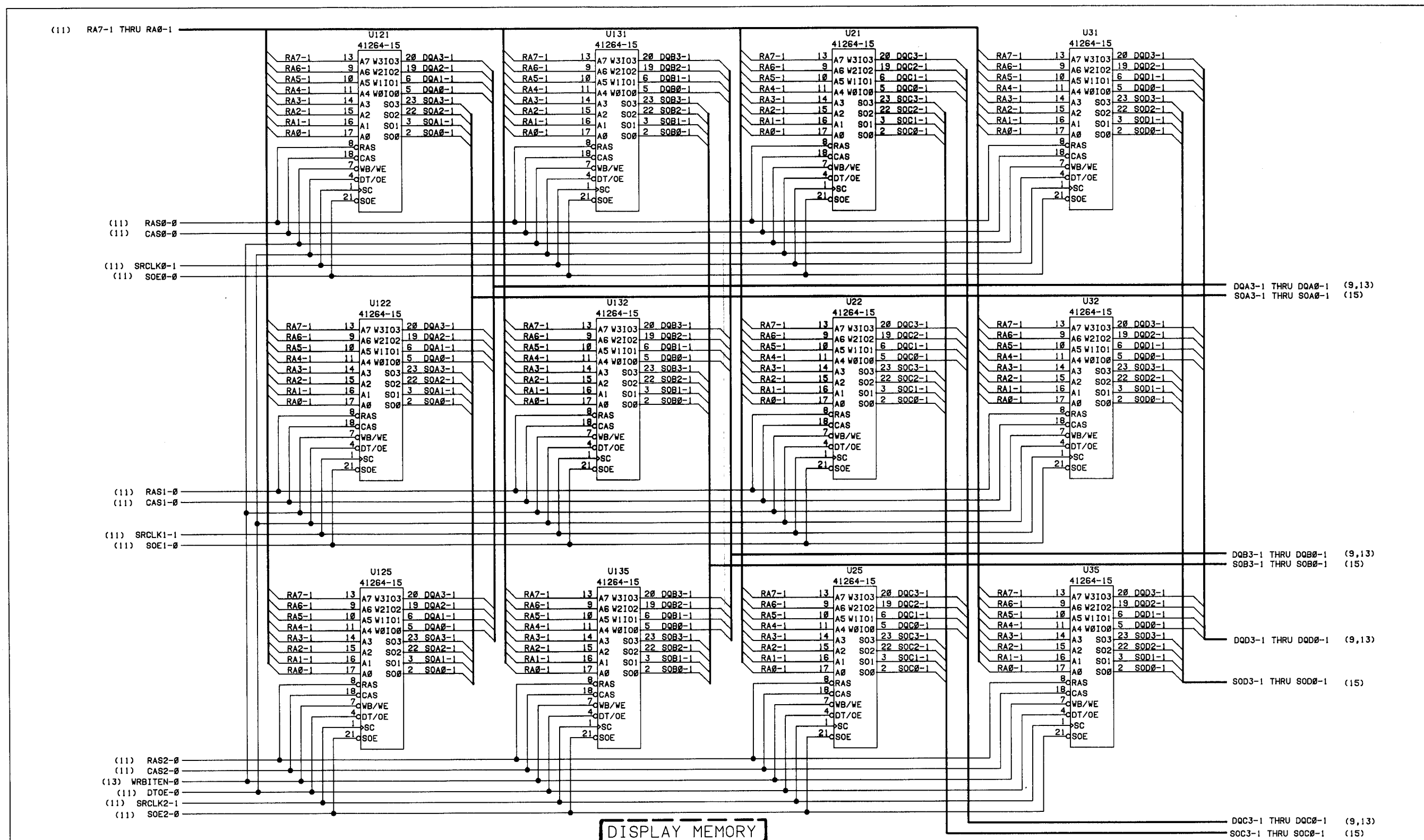
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	9 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



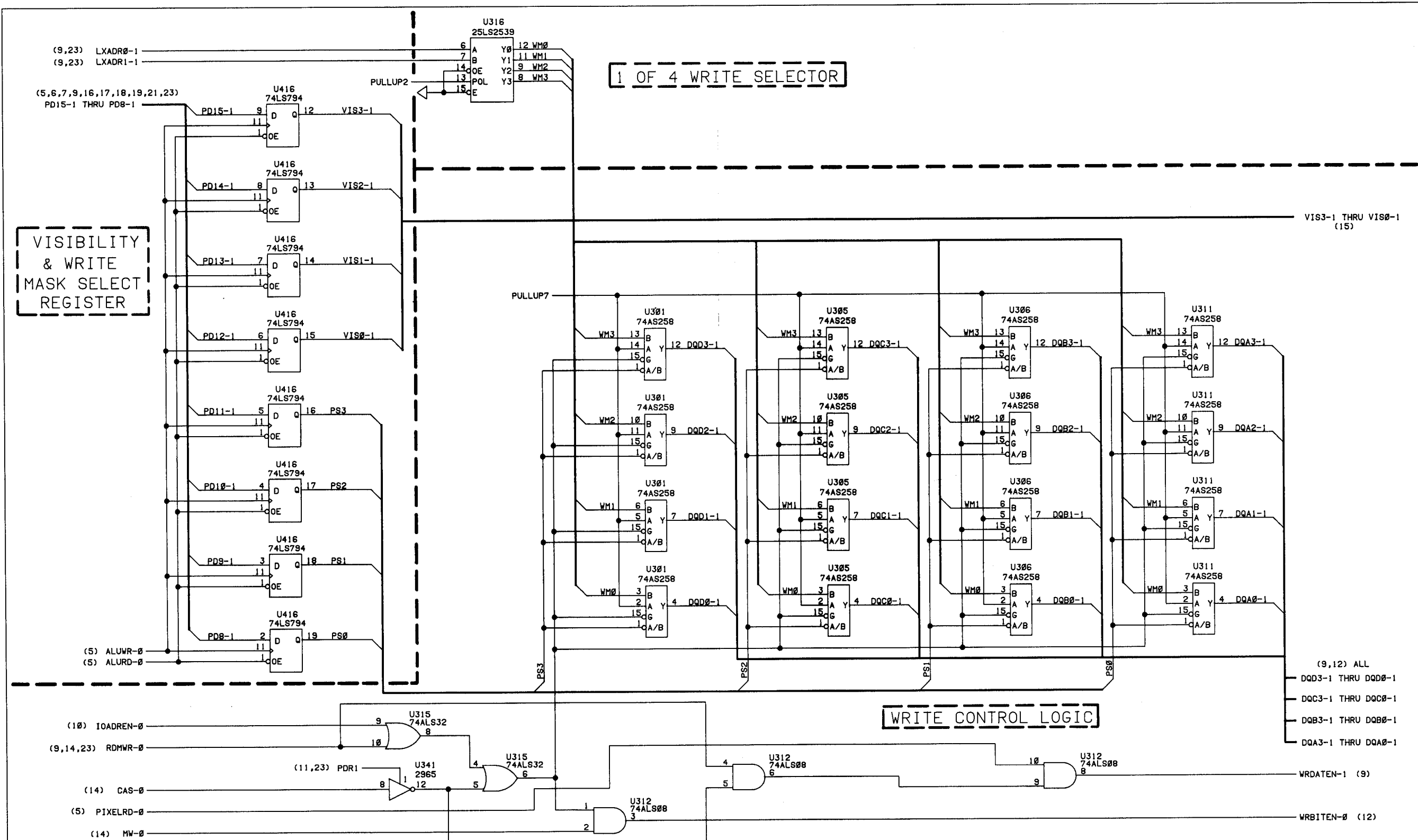
REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET: 10 of 26
PLOT DATE: 06-03-86			TITLE: DISPLAY CONTROL BOARD	
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986		



REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86		TEKTRONIX INC. © 1986	TITLE: DISPLAY CONTROL BOARD	11 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801			

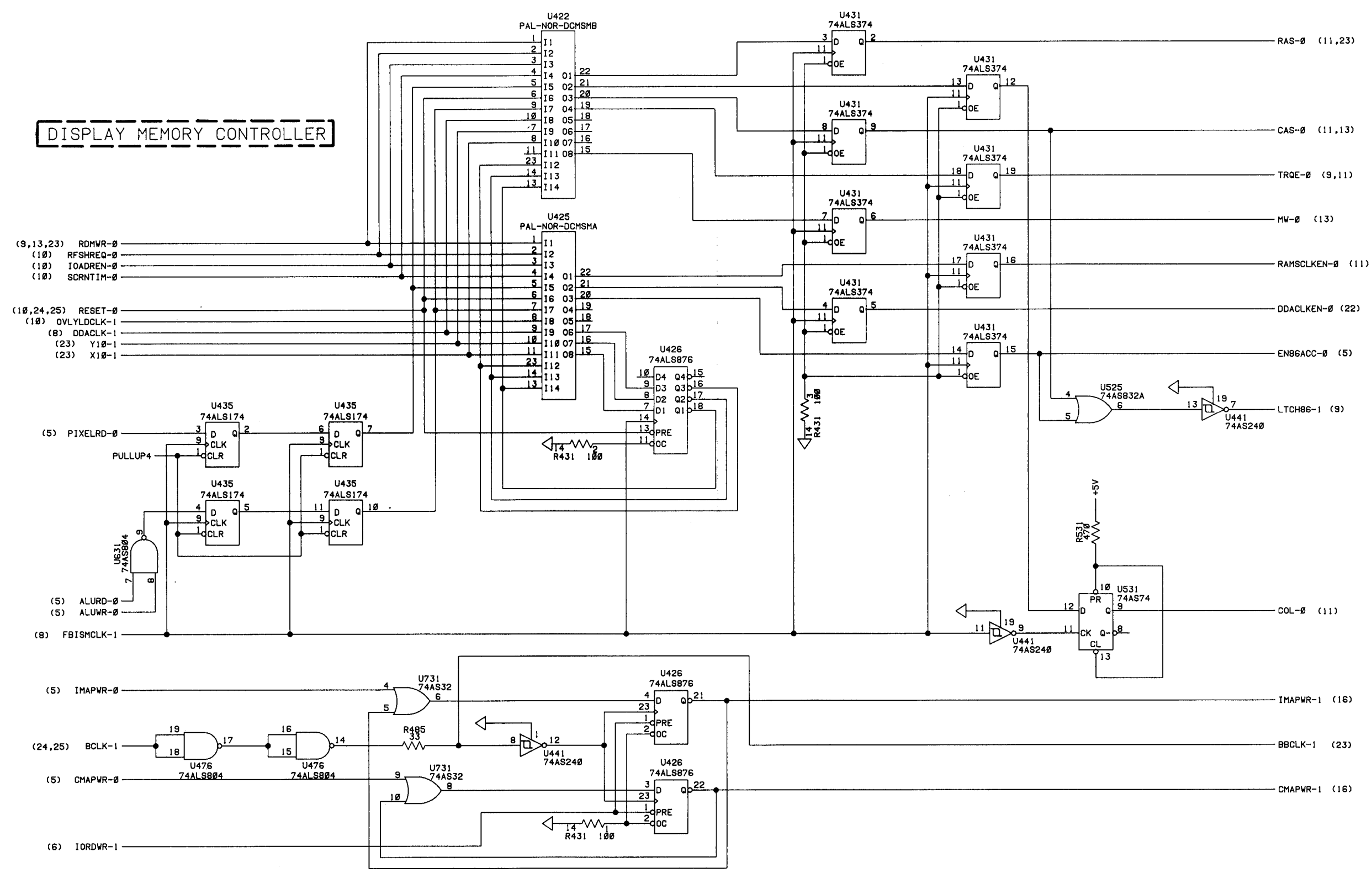


REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86		TEKTRONIX INC. © 1986	TITLE:	12 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801		DISPLAY CONTROL BOARD	

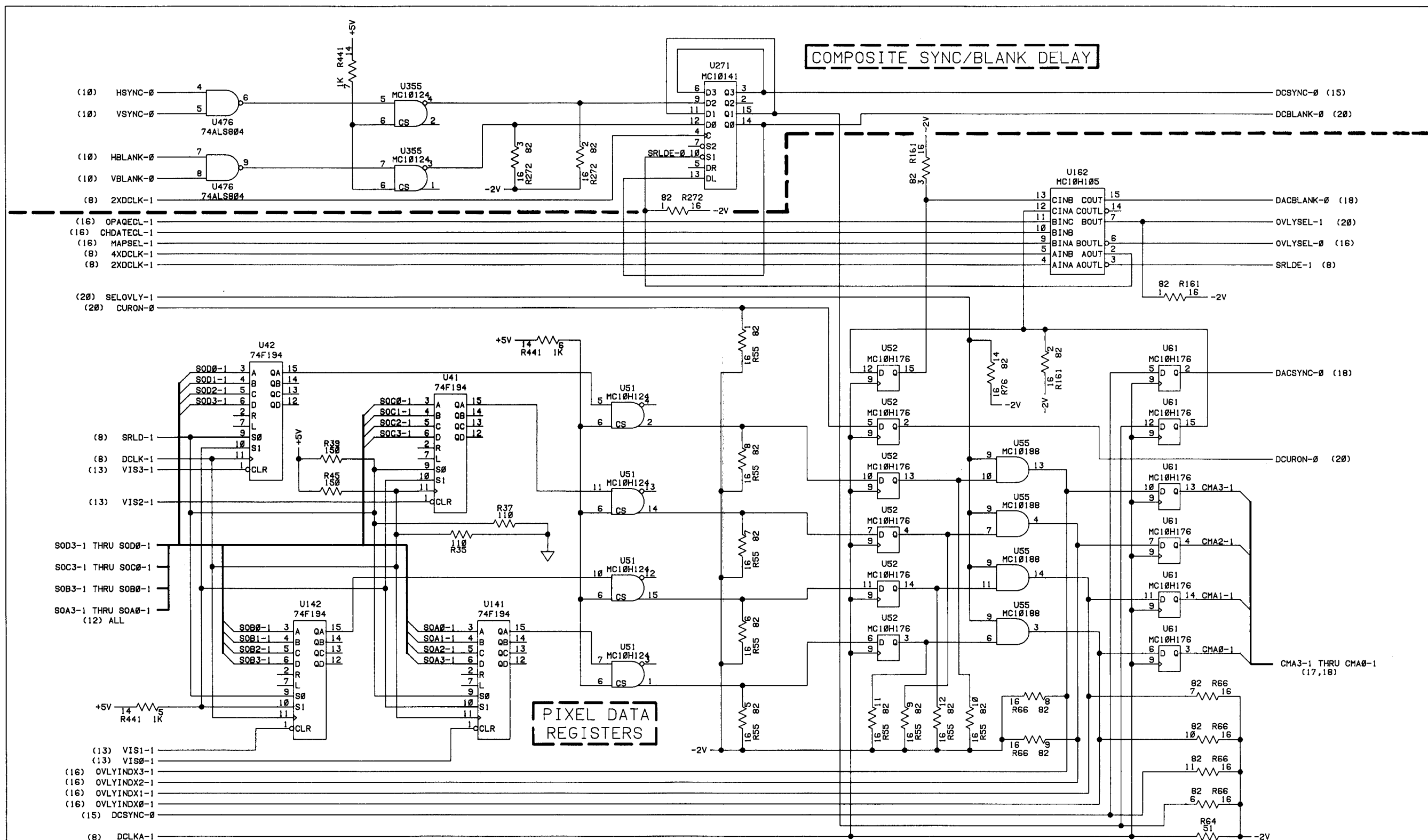


REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	13 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	

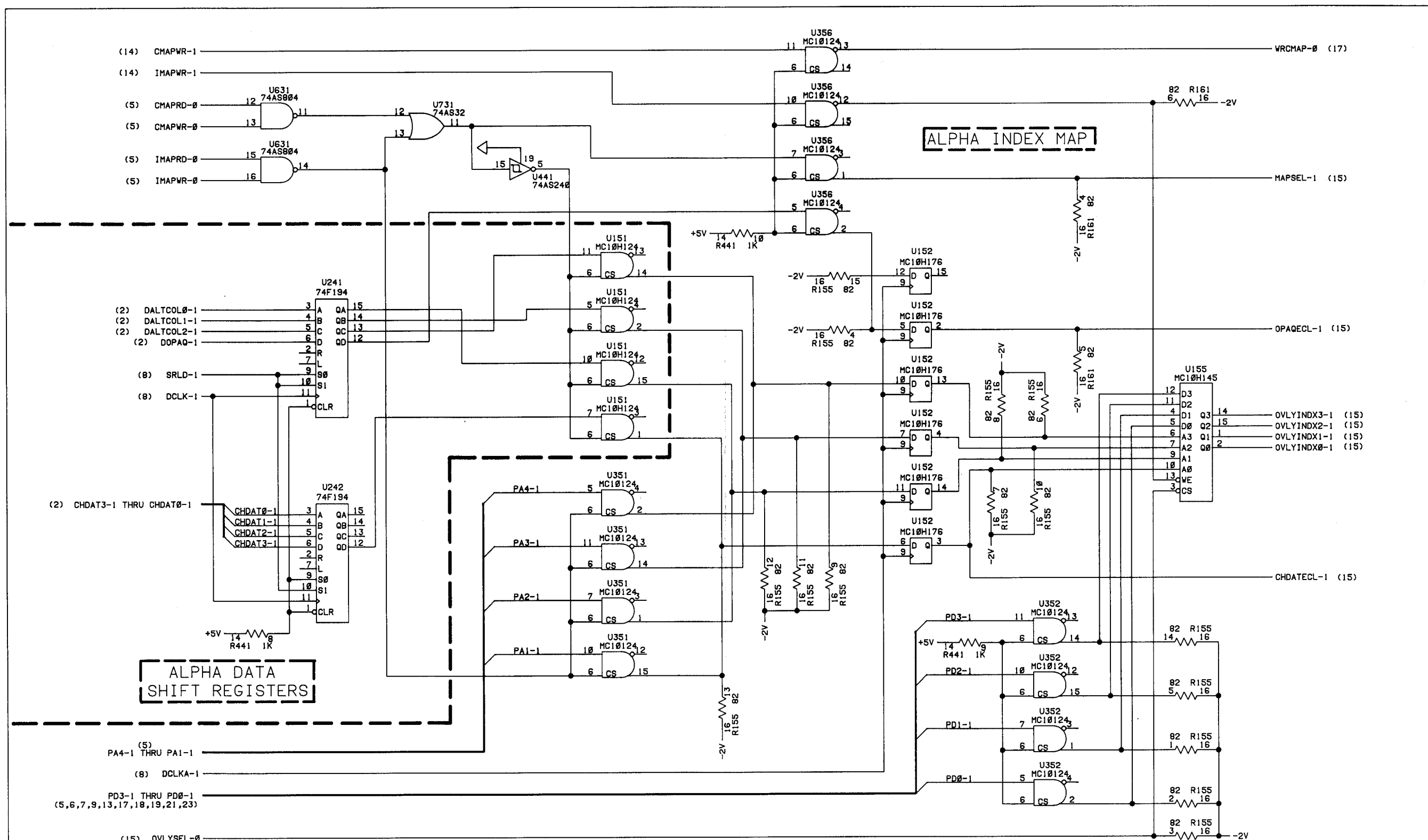
DISPLAY MEMORY CONTROLLER



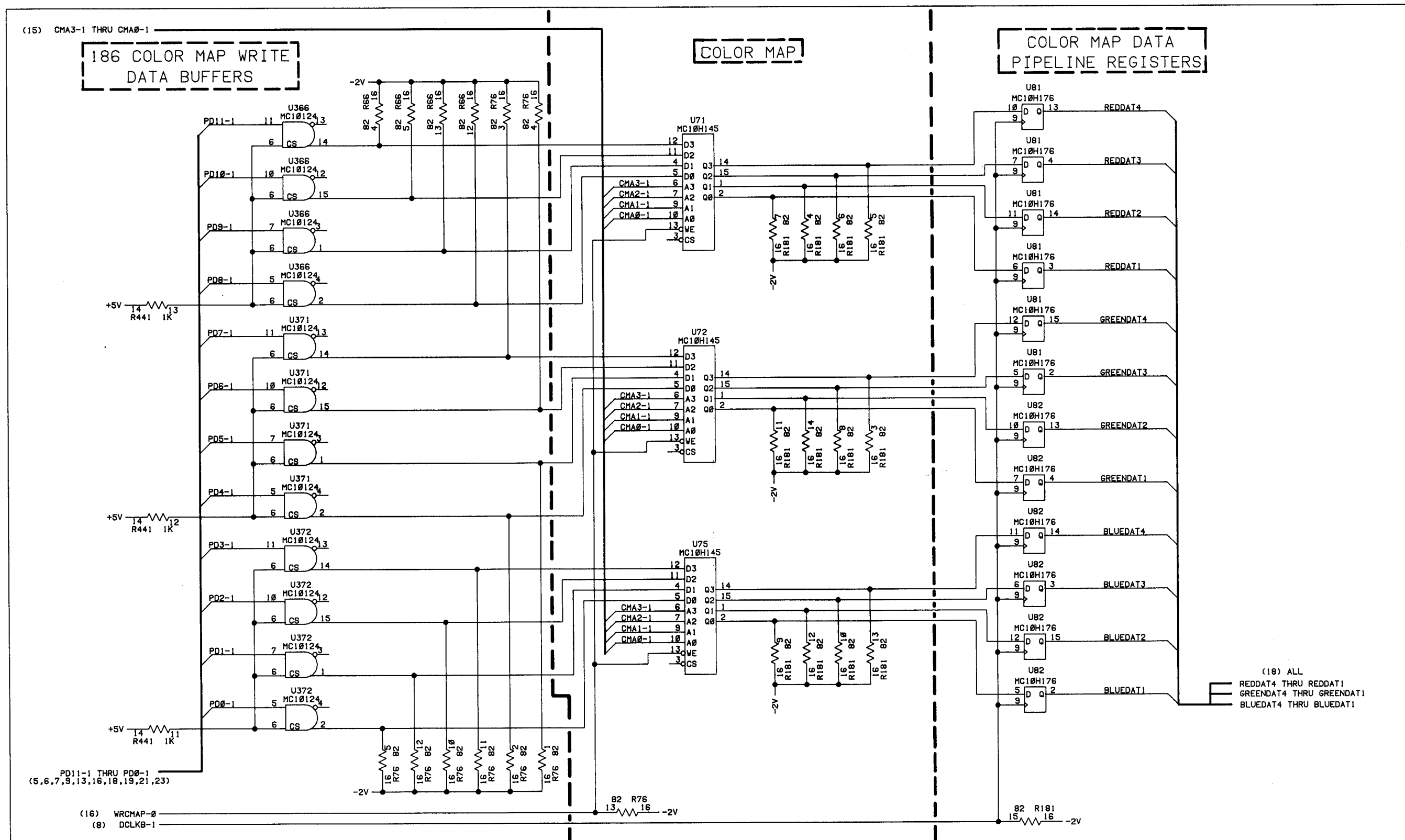
REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE: DISPLAY CONTROL BOARD	14 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986		



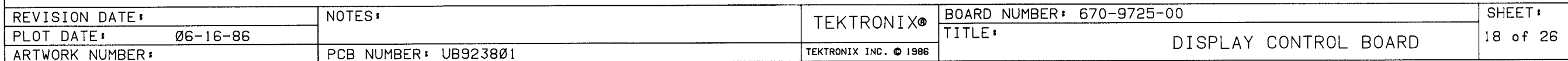
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-16-86			TITLE:	15 of 26
ARTWORK NUMBER:	PCB NUMBER: UB923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	

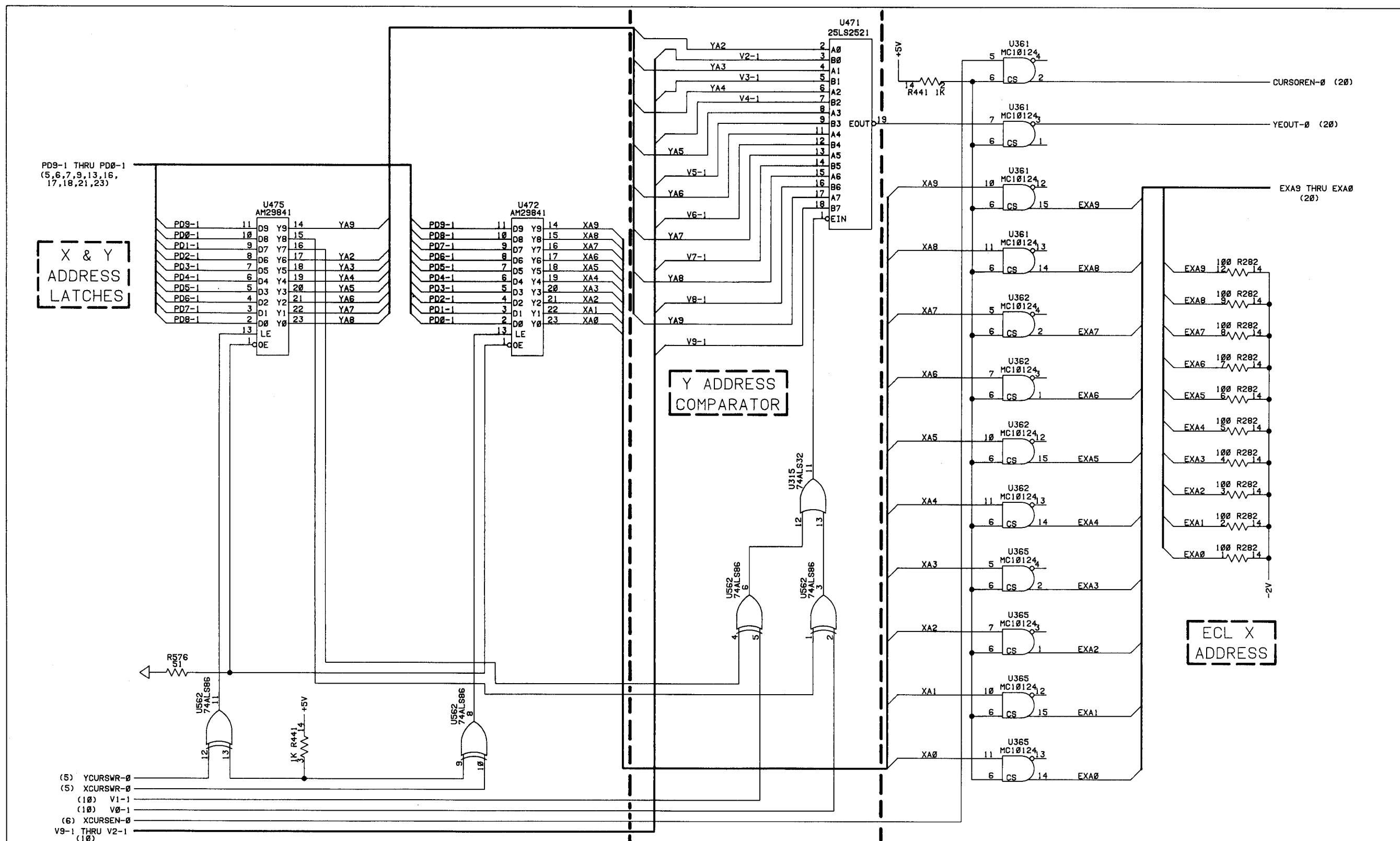


REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-16-86			TITLE:	16 of 26
ARTWORK NUMBER:	PCB NUMBER: UB923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	

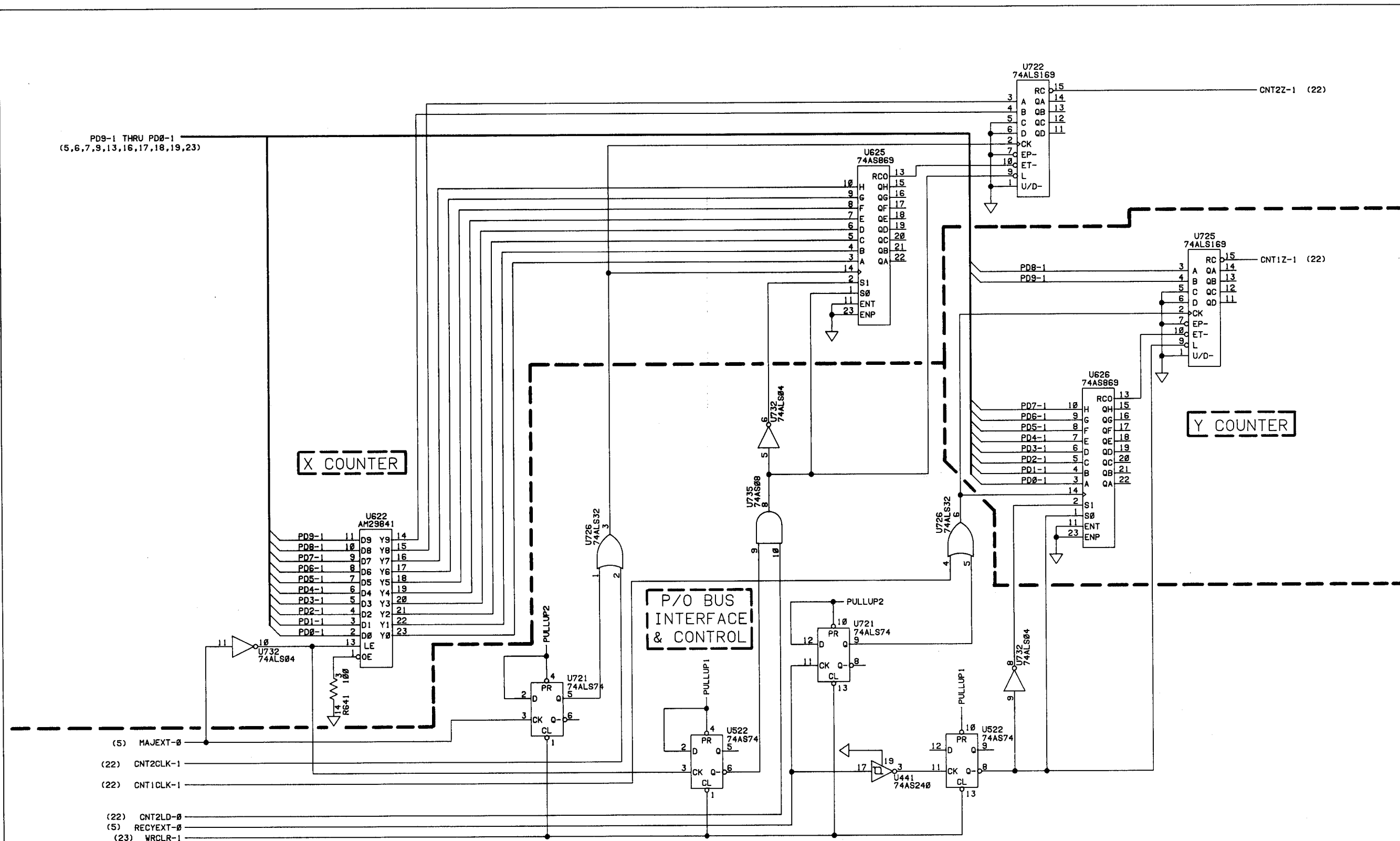


REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-16-86			TITLE: DISPLAY CONTROL BOARD	17 of 26
ARTWORK NUMBER:	PCB NUMBER: UB923801	TEKTRONIX INC. © 1986		

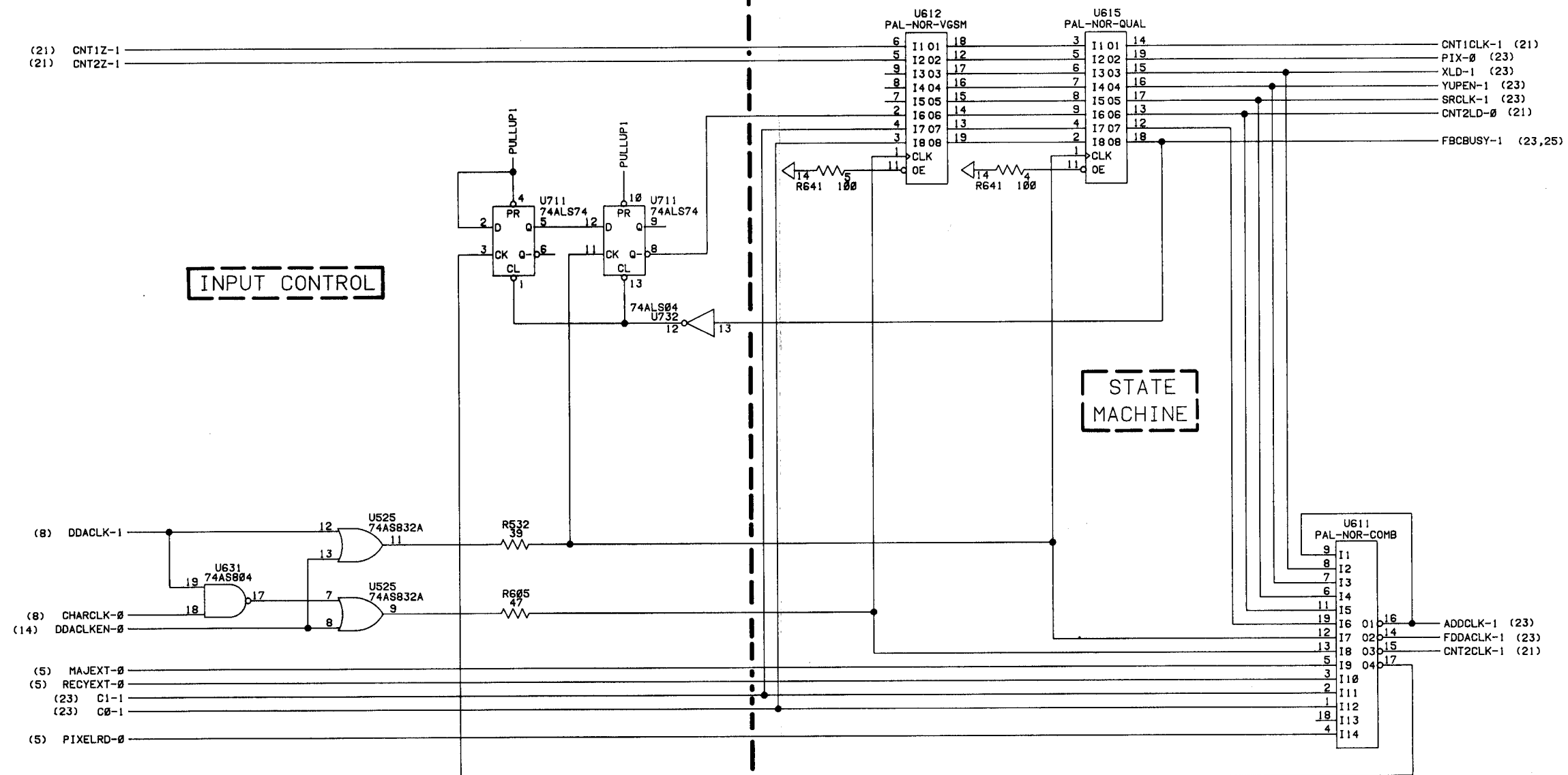




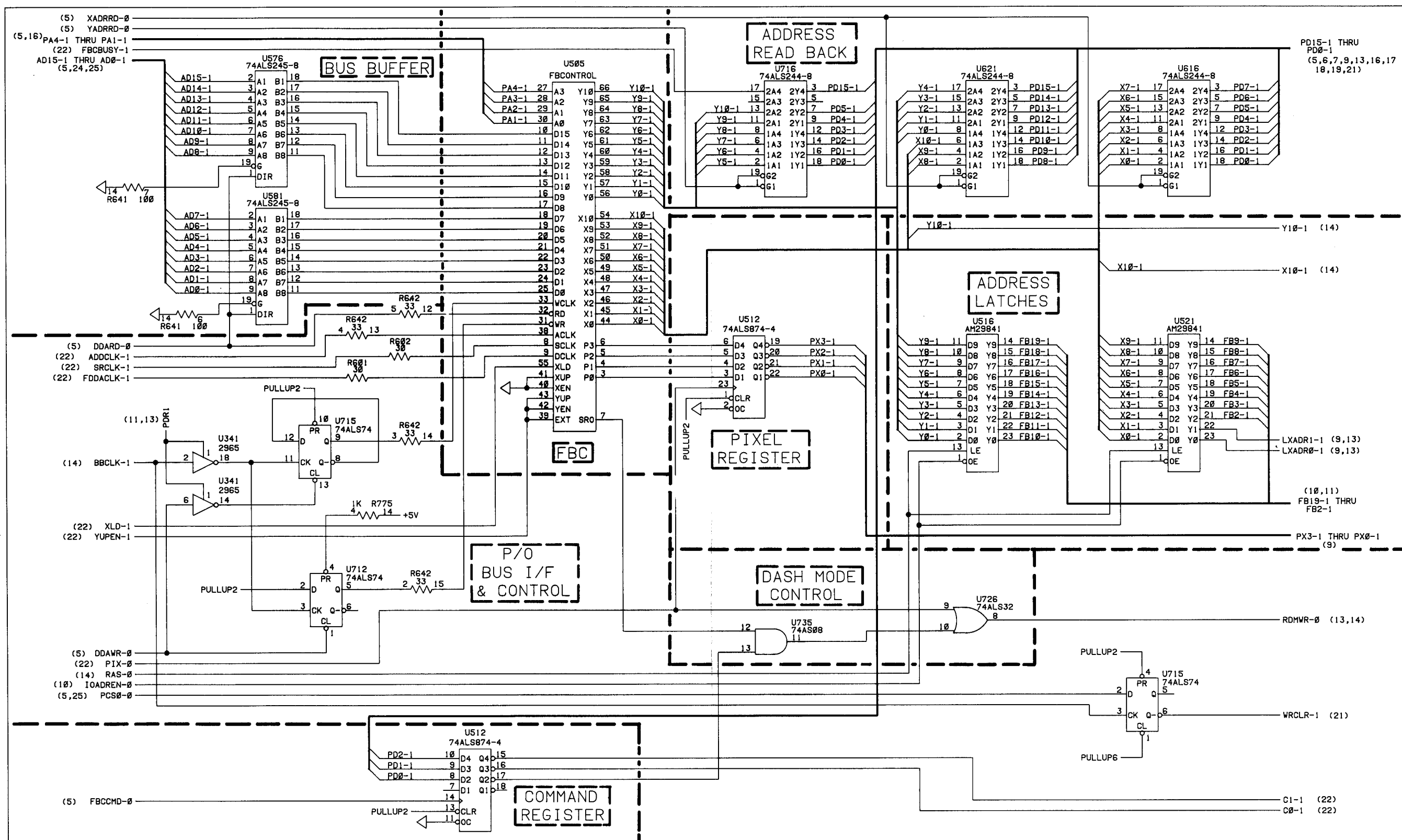
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	19 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	21 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86		TEKTRONIX INC. © 1986	TITLE: DISPLAY CONTROL BOARD	22 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801			



REVISION DATE:	NOTES: PULLUP RESISTORS ARE ON SHEET 26.	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE: DISPLAY CONTROL BOARD	23 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986		

1 ← P35 →
2 ← P35 →
3 ← P35
4 ← P35 — BS2-1 (25)
5 ← P35 →
6 ← P35 →
7 ← P35 — +5V
8 ← P35 — P2-1 (25)
9 ← P35
10 ← P35 — M/I0-1 (25)
11 ← P35
12 ← P35
13 ← P35 — PCS1-0 (25)
14 ← P35 →
15 ← P35 →
16 ← P35 →
17 ← P35 — DT/R-1 (5,25)
18 ← P35 — AD14-1 (5,23,25)
19 ← P35 — AD11-1 (5,23,25)
20 ← P35 — AD8-1 (5,23,25)
21 ← P35 — AD5-1 (5,23,25)
22 ← P35 — AD2-1 (5,23,25)
23 ← P35 — 4PAGE-0 (25)
24 ← P35 — +5V

25 ← P35 — LA19-1 (25)
26 ← P35 — LA16-1 (25)
27 ← P35 — LA13-1 (1,25)
28 ← P35 — LA10-1 (1,25)
29 ← P35 — LA7-1 (1,5,25)
30 ← P35 — LA4-1 (1,5,25)
31 ← P35 — LA1-1 (1,5,25)
32 ← P35 →
33 ← P35 →
34 ← P35
35 ← P35 — RAMACK-1 (25)
36 ← P35 — BS1-1 (25)
37 ← P35 →
38 ← P35 →
39 ← P35 — +5V
40 ← P35 — P1-1 (25)
41 ← P35
42 ← P35 — IORC-0 (5,6,25)
43 ← P35
44 ← P35 — MRDC-0 (25)
45 ← P35
46 ← P35 →
47 ← P35 — BCLK-1 (14,23,25)
48 ← P35 →

49 ← P35 — DEN-0 (25)
50 ← P35 — AD13-1 (5,23,25)
51 ← P35 — AD10-1 (5,23,25)
52 ← P35 — AD7-1 (5,23,25)
53 ← P35 — AD4-1 (5,23,25)
54 ← P35 — AD1-1 (5,23,25)
55 ← P35 — 2PAGE-0 (25)
56 ← P35 — +5V
57 ← P35 — LA18-1 (25)
58 ← P35 — LA15-1 (25)
59 ← P35 — LA12-1 (1,25)
60 ← P35 — LA9-1 (1,25)
61 ← P35 — LA6-1 (1,5,25)
62 ← P35 — LA3-1 (1,5,25)
63 ← P35 — LA0-1 (1,5,25)
64 ← P35 →
65 ← P35 →
66 ← P35
67 ← P35
68 ← P35 — BS0-1 (25)
69 ← P35 →
70 ← P35 — +5V
71 ← P35 — +5V
72 ← P35 — P0-1 (25)

73 ← P35
74 ← P35 — ACK-0 (5,6,25)
75 ← P35
76 ← P35 — IOWC-0 (5,6,25)
77 ← P35 — MWRC-0 (25)
78 ← P35 →
79 ← P35
80 ← P35 →
81 ← P35 — AD15-1 (5,23,25)
82 ← P35 — AD12-1 (5,23,25)
83 ← P35 — AD9-1 (5,23,25)
84 ← P35 — AD6-1 (5,23,25)
85 ← P35 — AD3-1 (5,23,25)
86 ← P35 — AD0-1 (5,23,25)
87 ← P35 — RESET-0 (10,14,25)
88 ← P35 — +5V
89 ← P35 — LA17-1 (25)
90 ← P35 — LA14-1 (1,25)
91 ← P35 — LA11-1 (1,25)
92 ← P35 — LA8-1 (1,25)
93 ← P35 — LA5-1 (1,5,25)
94 ← P35 — LA2-1 (1,5,25)
95 ← P35 — LBHE-0 (25)
96 ← P35 →

P35 96-PIN CONNECTOR

REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86		TEKTRONIX INC. © 1986	TITLE: DISPLAY CONTROL BOARD	24 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801			

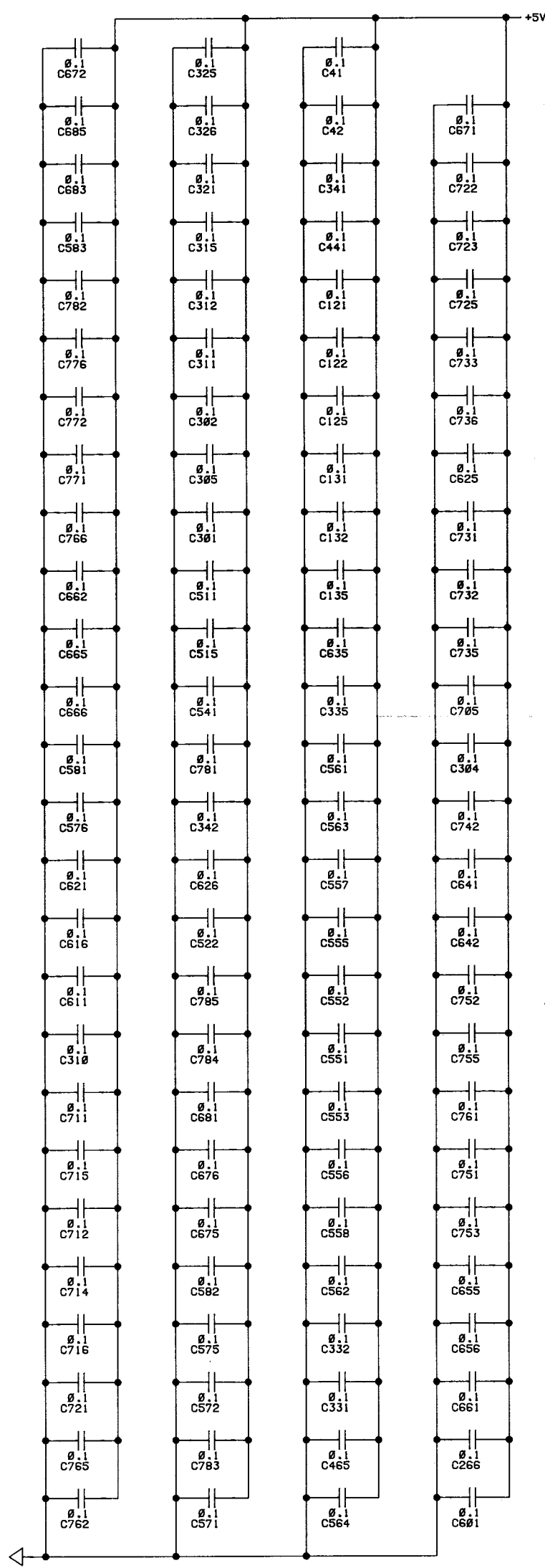
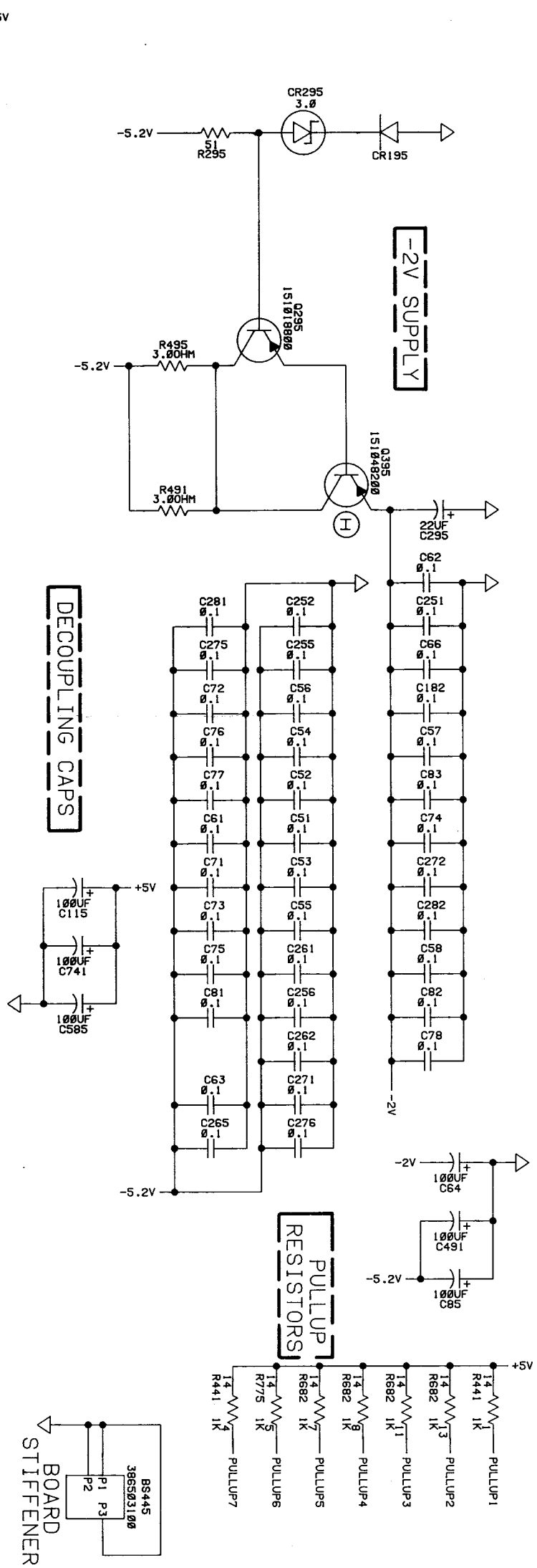
1 ← P39 →	25 ← P39 → PB-1 (24)	49 ← P39 →	73 ← P39 → +5V
2 ← P39 → LBHE-0 (24)	26 ← P39 → +5V	50 ← P39 → BCLK-1 (14,23,24)	74 ← P39 → 4PAGE-0 (24)
3 ← P39 → LA2-1 (1,5,24)	27 ← P39 → +5V	51 ← P39 →	75 ← P39 → AD2-1 (5,23,24)
4 ← P39 → LA5-1 (1,5,24)	28 ← P39 →	52 ← P39 → PCS0-0 (5,23)	76 ← P39 → AD5-1 (5,23,24)
5 ← P39 → LA8-1 (1,24)	29 ← P39 → BS0-1 (24)	53 ← P39 → MRDC-0 (24)	77 ← P39 → AD8-1 (5,23,24)
6 ← P39 → LA11-1 (1,24)	30 ← P39 → FBCBUSY-1 (22)	54 ← P39 → -5.2V	78 ← P39 → AD11-1 (5,23,24)
7 ← P39 → LA14-1 (1,24)	31 ← P39 →	55 ← P39 → IORC-0 (5,6,24)	79 ← P39 → AD14-1 (5,23,24)
8 ← P39 → LA17-1 (24)	32 ← P39 →	56 ← P39 → VBLANK-0 (10,15)	80 ← P39 → DT/R-1 (5,24)
9 ← P39 → +5V	33 ← P39 →	57 ← P39 → P1-1 (24)	81 ← P39 →
10 ← P39 → RESET-0 (10,14,24)	34 ← P39 → LA0-1 (1,5,24)	58 ← P39 → +5V	82 ← P39 →
11 ← P39 → AD0-1 (5,23,24)	35 ← P39 → LA3-1 (1,5,24)	59 ← P39 →	83 ← P39 →
12 ← P39 → AD3-1 (5,23,24)	36 ← P39 → LA6-1 (1,5,24)	60 ← P39 →	84 ← P39 → PCS1-0 (24)
13 ← P39 → AD6-1 (5,23,24)	37 ← P39 → LA9-1 (1,24)	61 ← P39 → BS1-1 (24)	85 ← P39 → ARS-0 (5,6)
14 ← P39 → AD9-1 (5,23,24)	38 ← P39 → LA12-1 (1,24)	62 ← P39 → RAMACK-1 (24)	86 ← P39 → -5.2V
15 ← P39 → AD12-1 (5,23,24)	39 ← P39 → LA15-1 (24)	63 ← P39 →	87 ← P39 → M/10-1 (24)
16 ← P39 → AD15-1 (5,23,24)	40 ← P39 → LA18-1 (24)	64 ← P39 →	88 ← P39 →
17 ← P39 →	41 ← P39 → +5V	65 ← P39 →	89 ← P39 → P2-1 (24)
18 ← P39 →	42 ← P39 → 2PAGE-0 (24)	66 ← P39 → LA1-1 (1,5,24)	90 ← P39 → +5V
19 ← P39 →	43 ← P39 → AD1-1 (5,23,24)	67 ← P39 → LA4-1 (1,5,24)	91 ← P39 →
20 ← P39 → MWRC-0 (24)	44 ← P39 → AD4-1 (5,23,24)	68 ← P39 → LA7-1 (1,5,24)	92 ← P39 →
21 ← P39 → IOWC-0 (5,6,24)	45 ← P39 → AD7-1 (5,23,24)	69 ← P39 → LA10-1 (1,24)	93 ← P39 → BS2-1 (24)
22 ← P39 → -5.2V	46 ← P39 → AD10-1 (5,23,24)	70 ← P39 → LA13-1 (1,24)	94 ← P39 →
23 ← P39 → ACK-0 (5,6,24)	47 ← P39 → AD13-1 (5,23,24)	71 ← P39 → LA16-1 (24)	95 ← P39 →
24 ← P39 →	48 ← P39 → DEN-0 (24)	72 ← P39 → LA19-1 (24)	96 ← P39 →

P39 96-PIN CONNECTOR

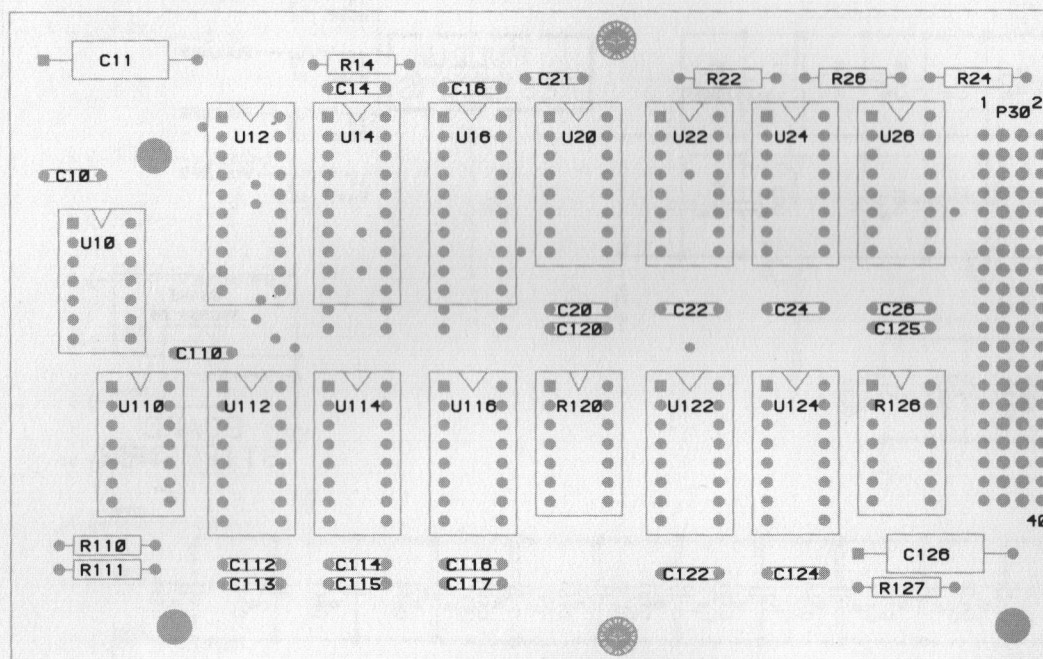
REVISION DATE:	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET:
PLOT DATE: 06-03-86			TITLE:	25 of 26
ARTWORK NUMBER:	PCB NUMBER: UA923801	TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	

VIDEO CONNECTOR

- 1 ← J889 -5.2V
- 2 ← J889 +5V
- 3 ← J889 -5.2V
- 4 ← J889
- 5 ← J889 VSYNC-1
- 6 ← J889
- 7 ← J889 HSYNC-0
- 8 ← J889
- 9 ← J889
- 10 ← J889
- 11 ← J889 BLUE
- 12 ← J889
- 13 ← J889 GREEN
- 14 ← J889
- 15 ← J889 RED
- 16 ← J889
- 17 ← J889 +5V
- 18 ← J889
- 19 ← J889 +5V
- 20 ← J889 -5.2V

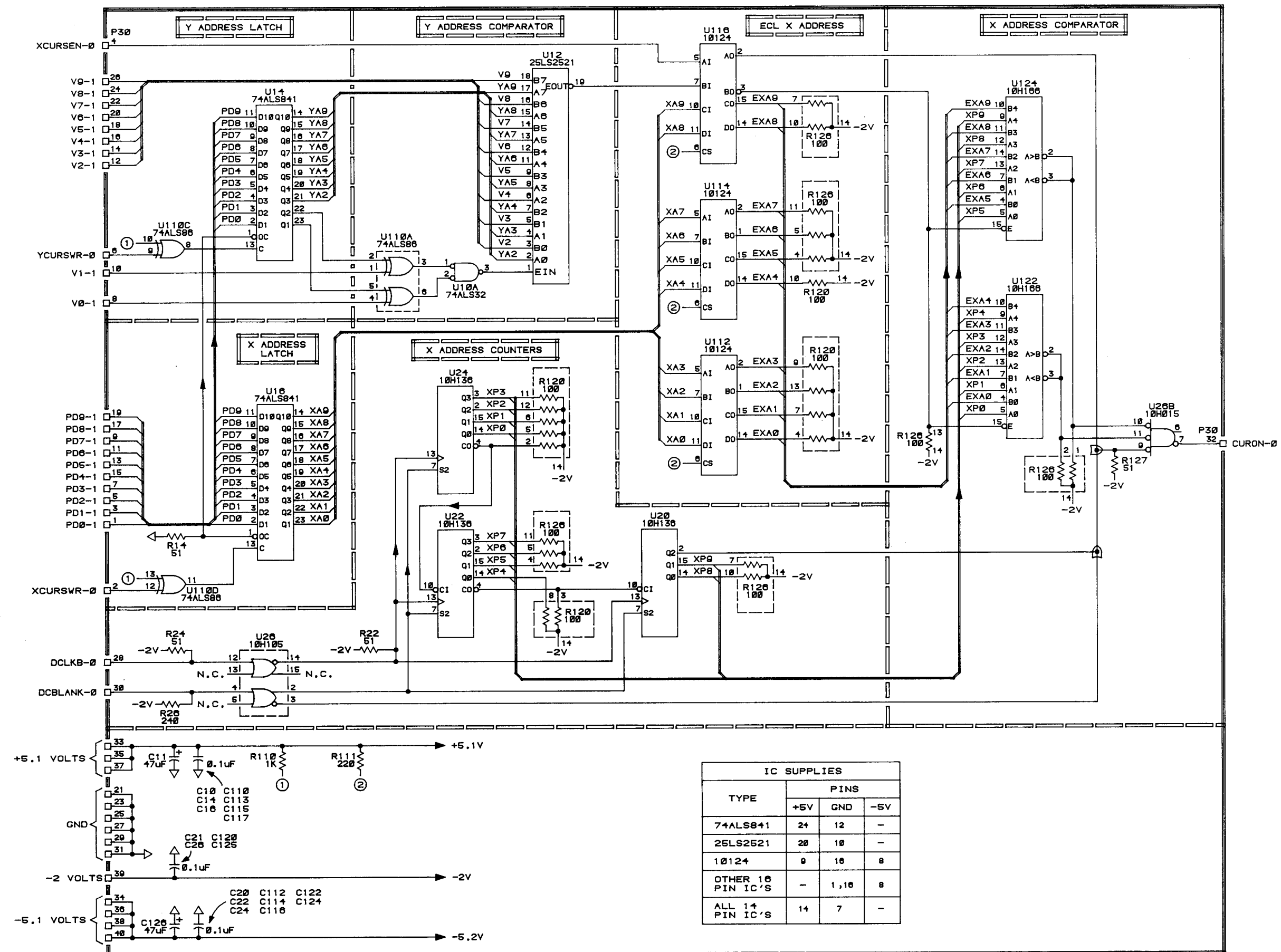


REVISION DATE:	06-03-86	NOTES:	TEKTRONIX®	BOARD NUMBER: 670-9725-00	SHEET: 26 of 26
PLOT DATE:					
ARTWORK NUMBER:			TEKTRONIX INC. © 1986	DISPLAY CONTROL BOARD	



5644-63

Cursor Board Component Locations (670-9181-00).



IC SUPPLIES			
TYPE	PINS		
	+5V	GND	-5V
74ALS841	24	12	-
25LS2521	20	10	-
10124	0	10	8
OTHER 16 PIN IC'S	-	1,10	8
ALL 14 PIN IC'S	14	7	-

FIRST USE: 4111
 DATE: REV, 24 SEPT 1985
 CONTROL NO.: SSA118.000

OTHER USES:

NOTES:

TEKTRONIX, INC. © 1985

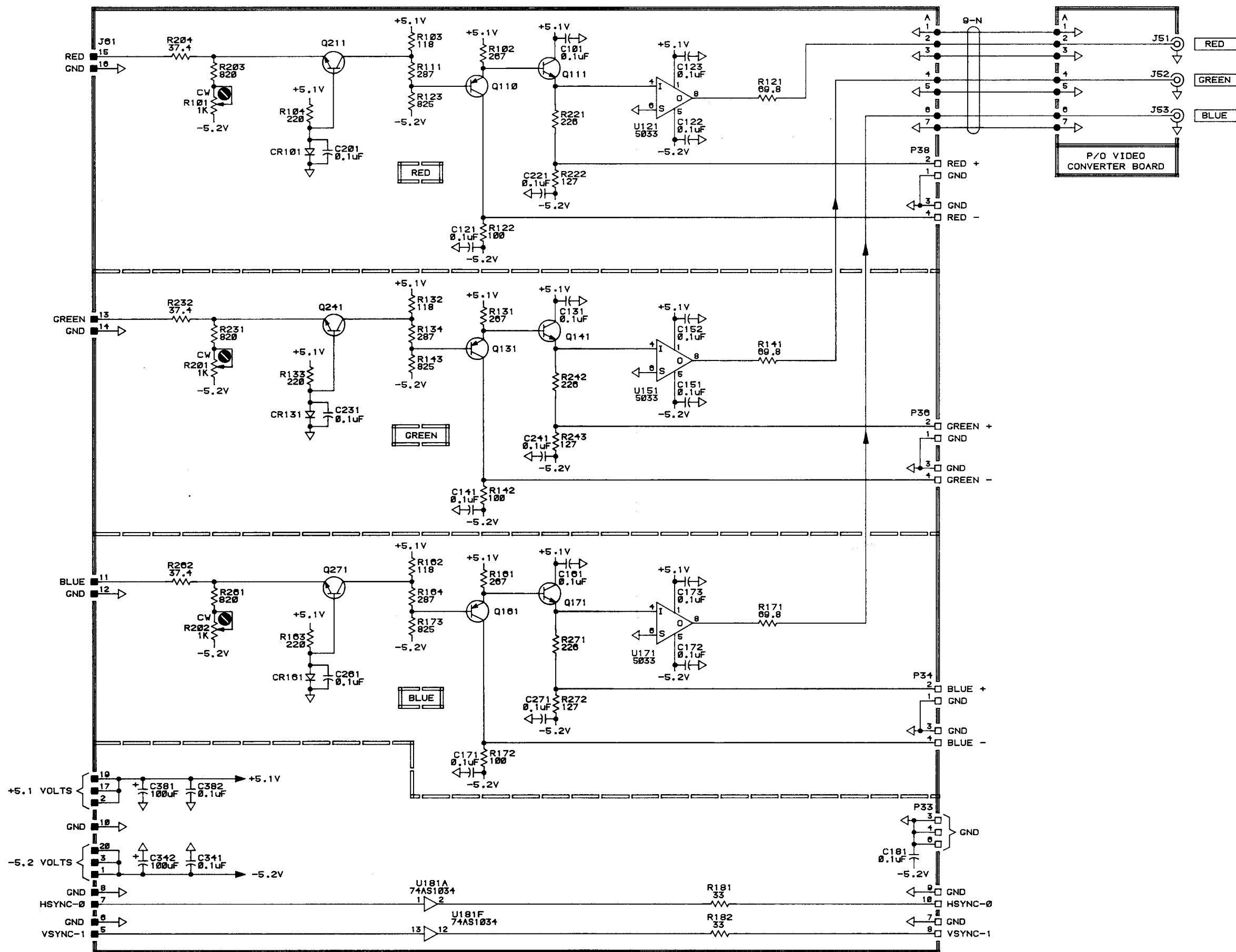
TITLE: 670-9181-00

CURSOR BOARD

Tektronix®

ASSEMBLY:
 CURSOR
 SHEET: 1 OF 1

5644-64



FIRST USE: 4111
 DATE: REV, 24 SEPT 1985
 CONTROL NO.: SSA117.000

OTHER USES:

NOTES:

TEKTRONIX, INC. © 1985

TITLE: 670-9003-00

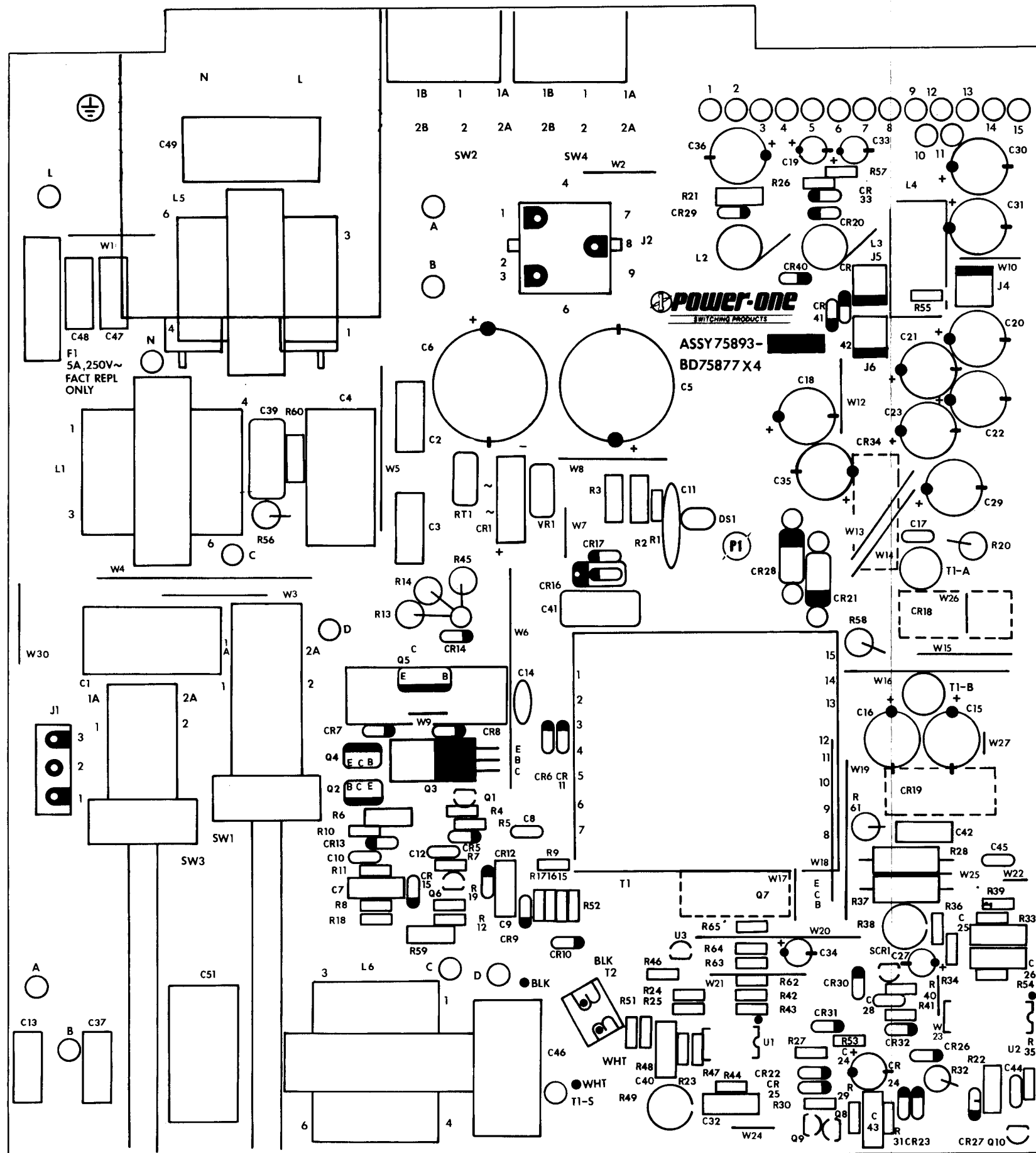
VIDEO CONVERTER BOARD

Tektronix®

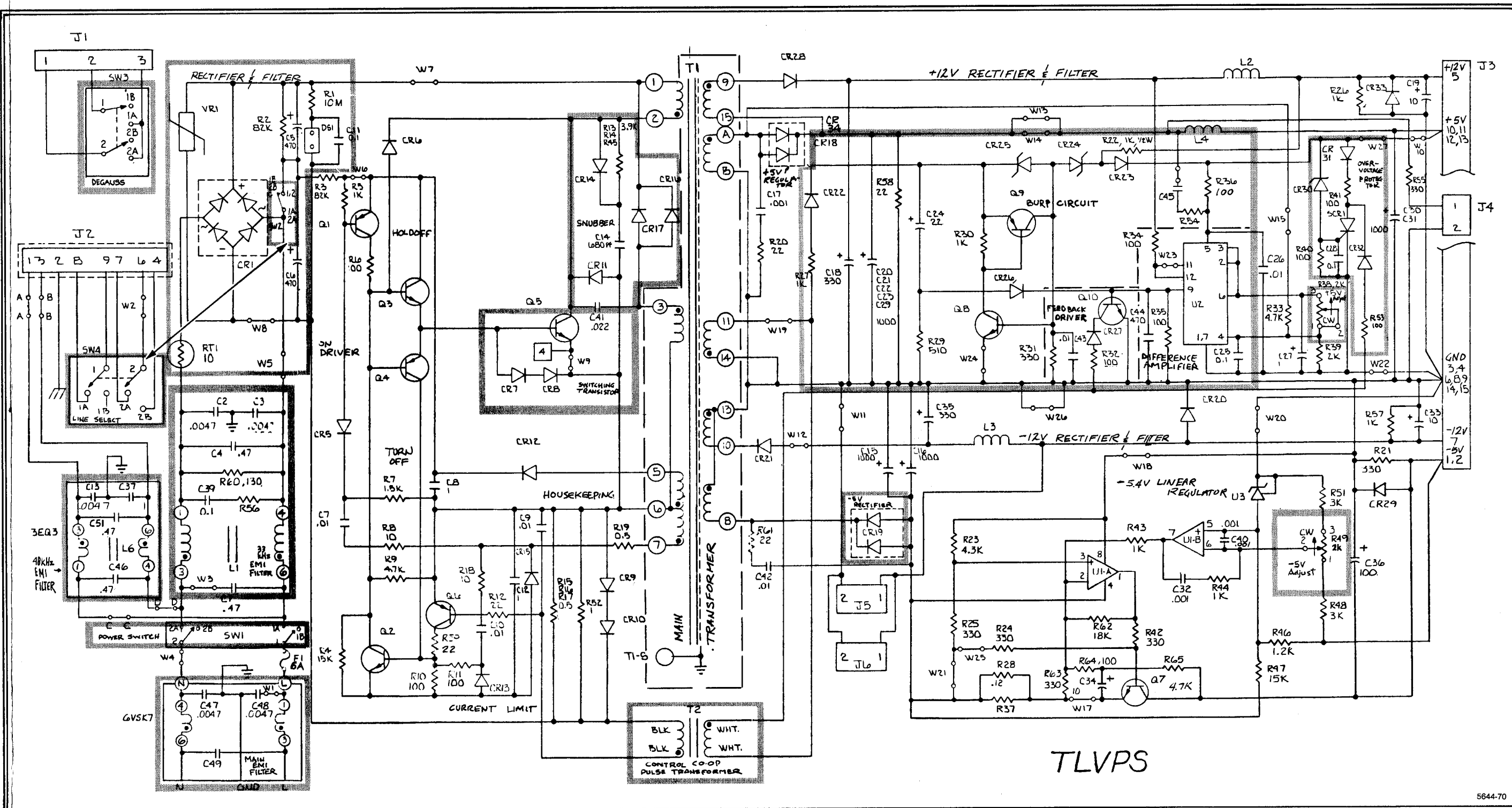
ASSEMBLY:

VIDCONV

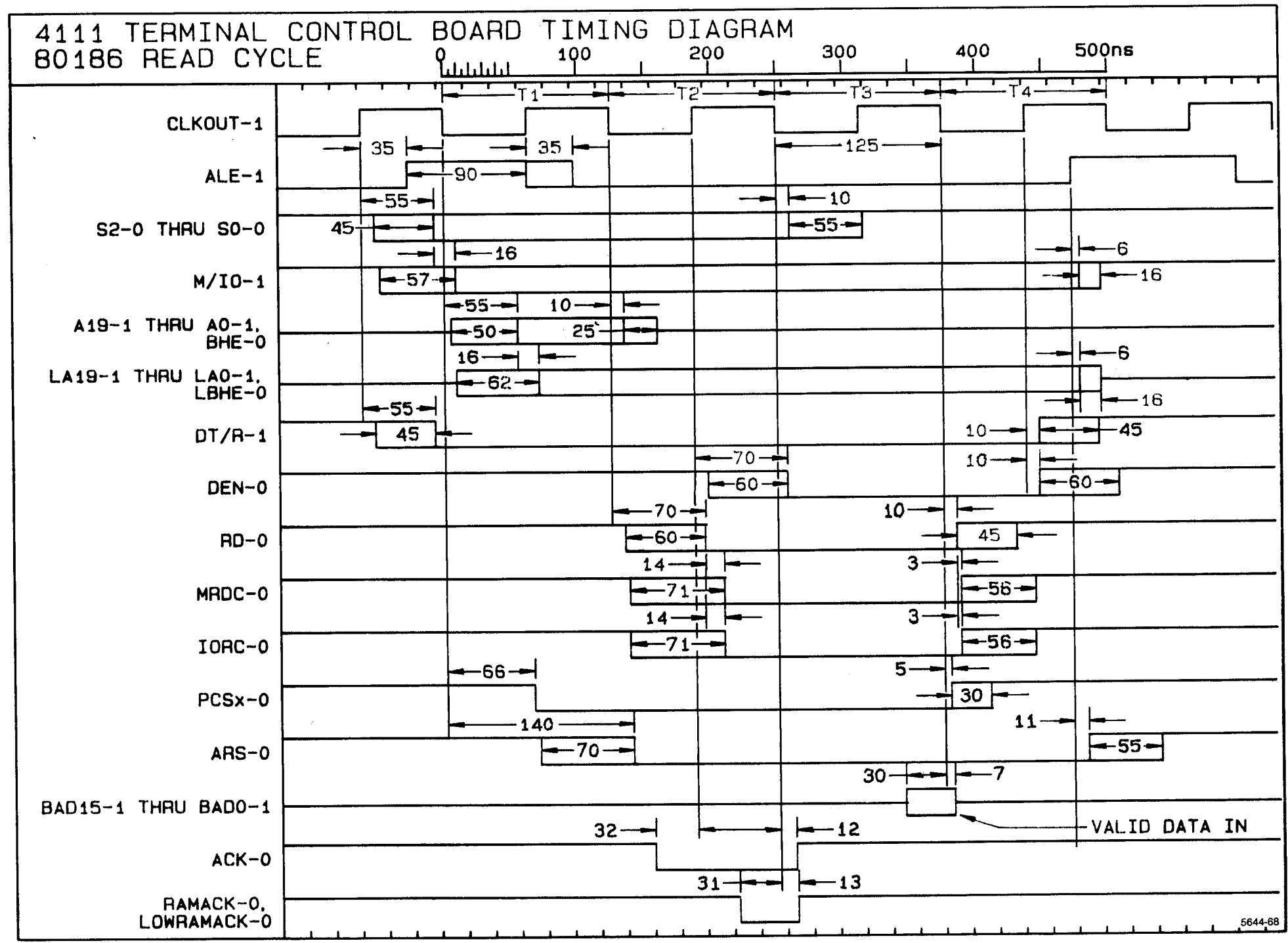
SHEET: 1 OF 1



5644-65

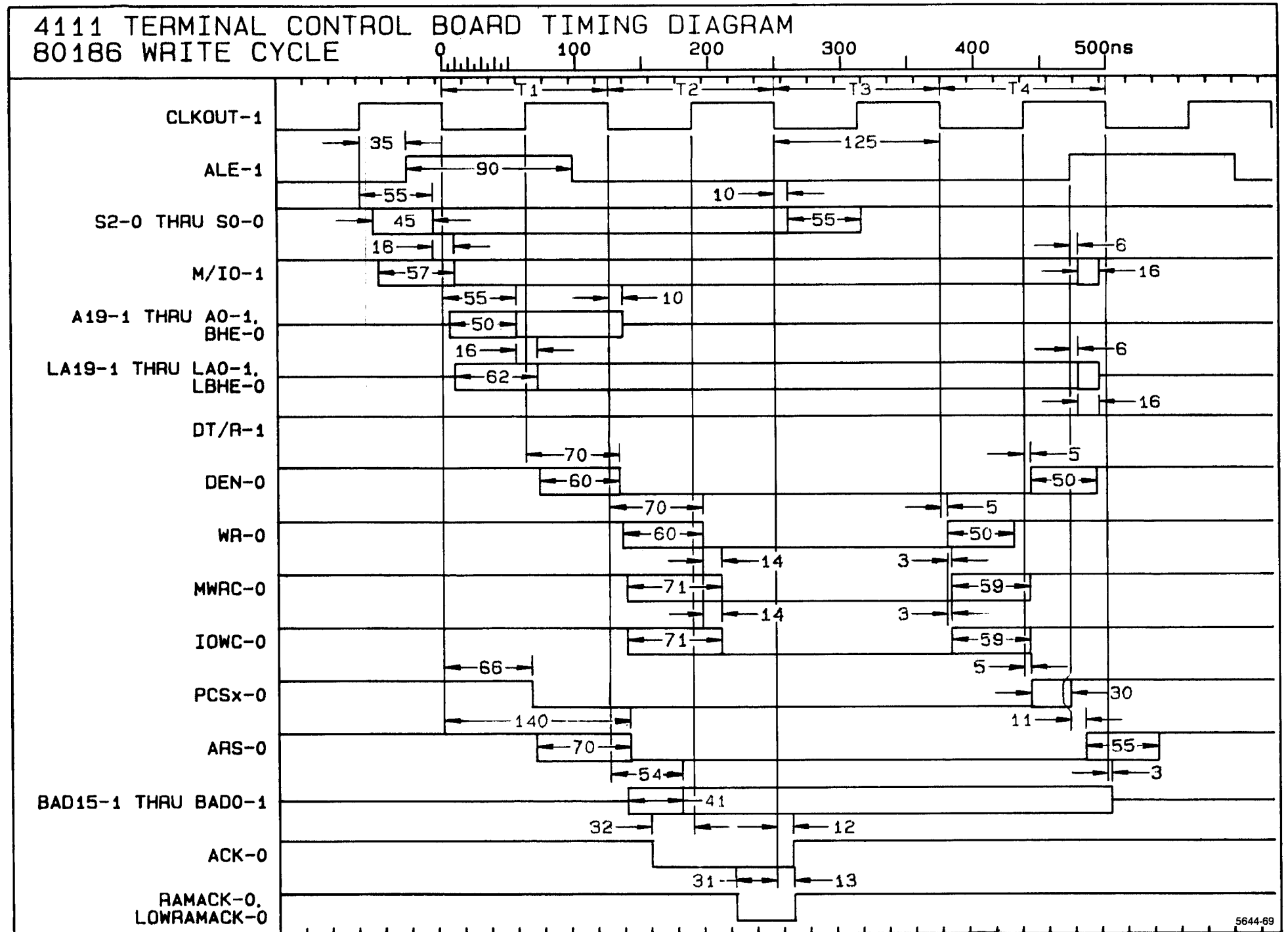


TLVPS

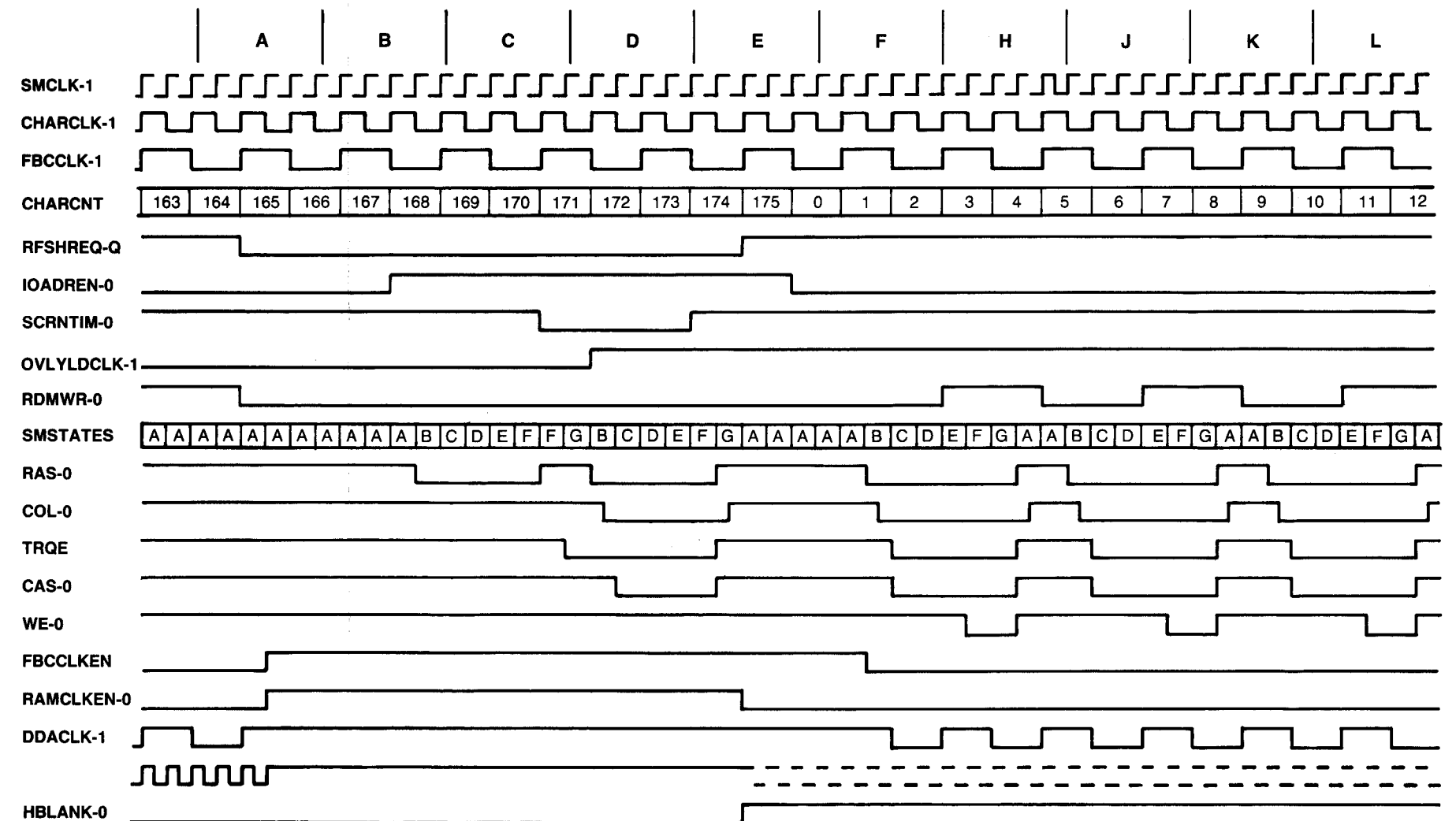


Terminal Control Board Timing.

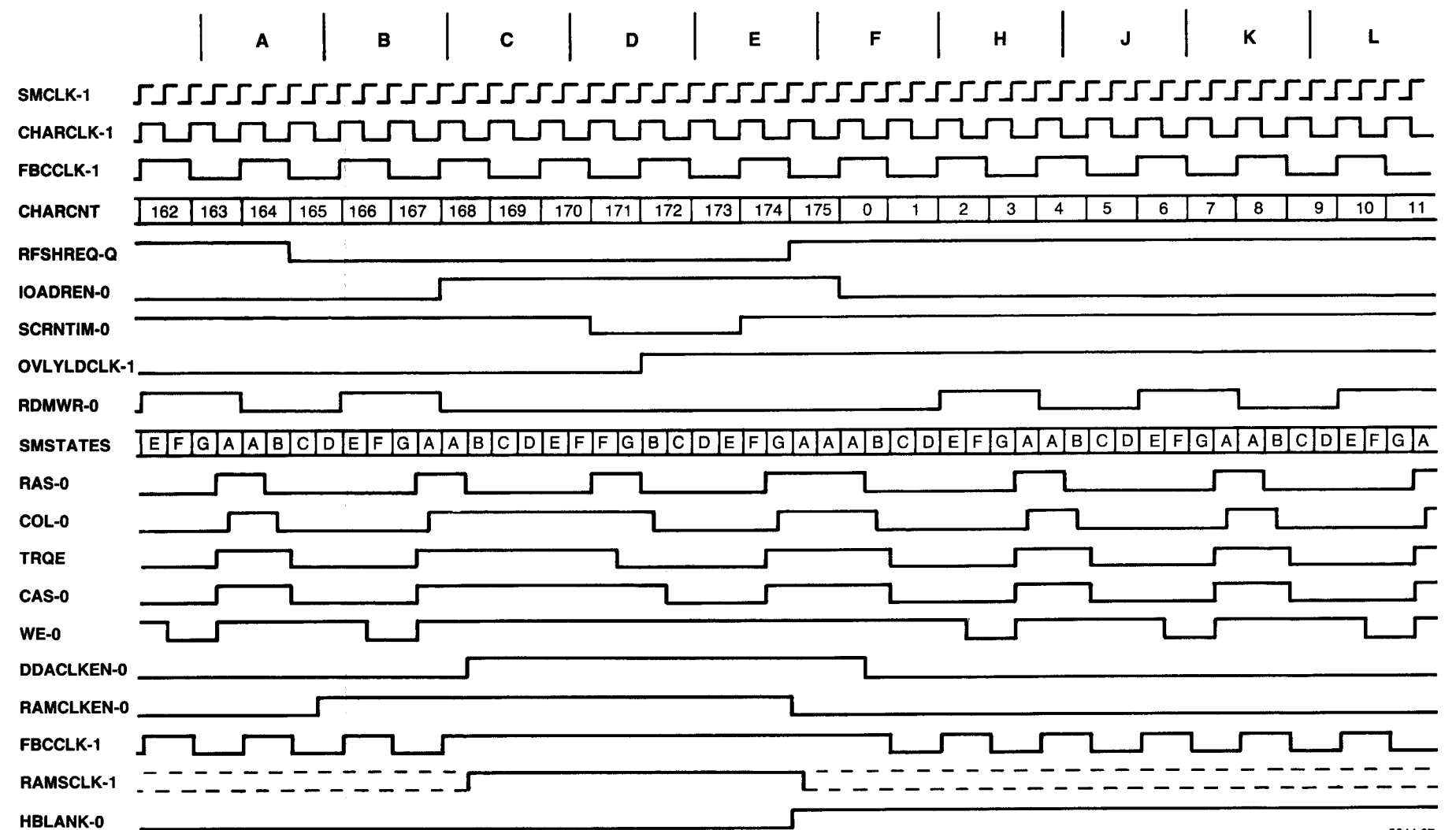
4111 TERMINAL CONTROL BOARD TIMING DIAGRAM 80186 WRITE CYCLE



Terminal Control Board Timing.



Display Control Board Timing.



5844-67

Display Control Board Timing.

Section 10

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 *Name & Description*

Assembly and/or Component

Attaching parts for Assembly and/or Component

---*---

Detail Part of Assembly and/or Component

Attaching parts for Detail Part

---*---

Parts of Detail Part

Attaching parts for Parts of Detail Part

---*---

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol ---*--- indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ABBREVIATIONS

INCH	ELECTRN	IN	INCH	SE	SINGLE END
NUMBER SIZE	ELEC	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ELECTLT	INSUL	INSULATOR	SEMICON	SEMICONDUCTOR
ADPTR	ELEM	INTL	INTERNAL	SHLD	SHIELD
ALIGN	EPL	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	EQPT	MACH	MACHINE	SKT	SOCKET
ASSEM	EXT	MECH	MECHANICAL	SL	SLIDE
ASSY	FIL	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	FLEX	NIP	NIPPLE	SLVG	SLEEVEING
AWG	FLH	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	FLTR	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	FR	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	FSTNR	OVH	OVAL HEAD	STL	STEEL
BRZ	FT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	FXD	PL	PLAIN or PLATE	T	TUBE
CAB	GSKT	PLSTC	PLASTIC	TERM	TERMINAL
CAP	HDL	PN	PART NUMBER	THD	THREAD
CER	HEX	PNH	PAN HEAD	THK	THICK
CHAS	HEX HD	PWR	POWER	TNSN	TENSION
CKT	HEX SOC	RCPT	RECEPTACLE	TPG	TAPPING
COMP	HLCPS	RES	RESISTOR	TRH	TRUSS HEAD
CONN	HLEXT	RGD	RIGID	V	VOLTAGE
COV	HV	RLF	RELIEF	VAR	VARIABLE
CPLG	IC	RTNR	RETAINER	W/	WITH
CRT	ID	SCH	SOCKET HEAD	WSHR	WASHER
DEG	IDNT	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	IMPLR	SCR	SCREW	XSTR	TRANSISTOR

REPLACEABLE MECHANICAL PARTS

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
00779	AMP INC	P O BOX 3608	HARRISBURG PA 17105
01536	TEXTRON INC		ROCKFORD IL 61108
	CAMCAR DIV	1818 CHRISTINA ST	
	SEMS PRODUCTS UNIT		
06383	PANDUIT CORP	17301 RIDGELAND	TINLEY PARK IL 60477
06915	RICHCO PLASTIC CO	5825 N TRIPP AVE	CHICAGO IL 60646
09922	BURNODY CORP	RICHARDS AVE	NORMALK CT 06852
11897	PLASTIGLIDE MFG CORP	2701 N EL SEGUNDO BLVD	HAWTHORNE CA 90250
13511	AMPHENOL CADRE DIV BUNKER RAMO CORP		LOS GATOS CA
16428	BELDEN CORP	2200 US HWY 27 SOUTH	RICHMOND IN 47374
	ELECTRONIC DIV	P O BOX 1980	
19613	MINNESOTA MINING AND MFG CO	1410 E PIONEER DR	IRVING TX 75061
	TEXTOL PRODUCTS DEPT		
	ELECTRONIC PRODUCT DIV		
27264	MOLEX INC	2222 WELLINGTON COURT	LISLE IL 60532
	CORPORATE HQ		
30161	AAVID ENGINEERING INC	30 COOK COURT	LACONIA NH 03246
31918	ITT SCHADON INC	8081 WALLACE RD	EDEN PRAIRIE MN 55343
54407	POWER-ONE INC	740 CALLE PLANO DR	CAMARILLO CA 93010
58361	GENERAL INSTRUMENT CORP	3400 HILLVIEW AVE	PALO ALTO CA 94304
	OPTOELECTRONICS DIV		
70485	ATLANTIC INDIA RUBBER WORKS INC	571 N POLK ST	CHICAGO IL 60607
70903	BELDEN CORP	2000 S BATAVIA AVE	GENEVA IL 60134
73743	FISCHER SPECIAL MFG CO	446 MORGAN ST	CINCINNATI OH 45206
77900	SHAKEPROOF	SAINT CHARLES RD	ELGIN IL 60120
	DIV OF ILLINOIS TOOL WORKS		
78189	ILLINOIS TOOL WORKS INC	ST CHARLES ROAD	ELGIN IL 60120
	SHAKEPROOF DIVISION		
80009	TEKTRONIX INC	4900 S W GRIFFITH DR	BEAVERTON OR 97077
		P O BOX 500	
83385	MICRODOT MANUFACTURING INC	3221 N BIG BEAVER RD	TROY MI 48098
	GREER-CENTRAL DIV		
89663	REESE, J. RAMSEY, INC.	71 MURRAY STREET	NEW YORK, NY 10007
93907	TEXTRON INC	600 18TH AVE	ROCKFORD IL 61101
	CAMCAR DIV		
98978	INTERNATIONAL ELECTRONIC RESEARCH CORP	135 W MAGNOLIA BLVD	BURBANK CA 91502
	SUB OF DYNAMICS CORP OF AMERICA		
53109	FELLER ASA ADOLF AG	355 TESCONI CIRCLE	SANTA ROSA CA 95401
	C/O PANEL COMPONENTS CORP		
TK0435	LEMIS SCREM CO	4114 S PEORIA	CHICAGO IL 60609
TK0648	PRECISION SPRING AND STAMPING	22617 85TH PL SO	KEN WA 98031
TK1099	INSTRUMENT SPECIALTIES CO	BOX A 1	DELAWARE WATERGAP PA 18327
TK1373	PATELEC-CEM (ITALY)	10156 TORINO	VAICENTALLO 62/455 ITALY
TK1504	IMS EQUIPMENT INC	2804 BARRANCA	IRVINE CA 92714
TK6020	DAINICHI-NIPPON CABLES	NEW KOKUSAI BLDG 4-1	TOKYO 100 JAPAN
		MARUNOUCHI 3-CHOME CHIYODA-KU	

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-1	200-2955-02		1	COVER,TERMINAL:TOP (ATTACHING PARTS)	80009	200-2955-02
-2	212-0115-00		3	SCR,ASSEM MSHR:8-32 X 0.75,PNH,STL,POZ	01536	ORDER BY DESCR
-3	212-0674-00		2	SCR,ASSEM MSHR:10-32 X 0.875,PNH,STL (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-4	386-5139-02		1	PANEL,SIDE:LEFT (ATTACHING PARTS)	80009	386-5139-02
-5	212-0122-00		3	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-6	386-5138-02		1	PANEL,SIDE:RIGHT (ATTACHING PARTS)	80009	386-5138-02
-7	212-0122-00		3	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-7.1	348-0836-04		1	SHLD GSKT,ELEX:49.25 L,+/-0.25	80009	348-0836-04
-8	119-2044-00		1	FAN ASSEMBLY:M/BAFFLES (ATTACHING PARTS)	80009	119-2044-00
-9	212-0122-00		1	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-10	-----		1	FAN ASSEMBLY INCLUDES .FAN,TUBEAXIAL:12 VOC,3.6M,57 CEM (SEE REPL CHASSIS PARTS B1001) (ATTACHING PARTS)		
-11	212-0037-00		4	.SCREN,MACHINE:8-32 X 1.75,FILH,STL (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-12	348-0004-00		1	.GROMMET,RUBBER:BLACK,ROUND,0.281 ID	70485	763
-13	255-0249-00		1	.PLASTIC CHANNEL:0.205 X 0.155 X 0.035	80009	255-0249-00
-13.1	348-0901-00		1	.GASKET,SEAL:0.250 THK X 0.50 WIDE X 25 FEE .T PORON 4716-16,M/PRESS	80009	348-0901-00
-14	200-3125-01		1	COVER,CKT BD:	80009	200-3125-01
-15	348-0932-00		2	SHLD GSKT,ELEX:4.5 L,+/- 0.250	80009	348-0932-00
-16	348-0836-01		1	SHLD GSKT,ELEX:32.25 L,+/- 0.250	80009	348-0836-01
-17	333-3206-01		1	PANEL,REAR: (ATTACHING PARTS)	80009	333-3206-01
-18	212-0115-00		2	SCR,ASSEM MSHR:8-32 X 0.75,PNH,STL,POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-19	348-0836-00		3	SHLD GSKT,ELEX:4.5 L	80009	348-0836-00
-19.1	348-0836-03		1	SHLD GSKT,ELEX:19.75 L,+/-0.25	80009	348-0836-03
-20	131-0132-00		1	CONTACT,ELEC:FINGER STRIP	TK1099	97135X3.75INCH
-21	196-3062-00		1	LEAD,ELECTRICAL:10 AWG,8.0 L,BRAID M/BLACK PVC JKT	80009	196-3062-00
-22	175-0371-00		1	.CA ASSY,SP,ELEC:4,30 AWG,108.0 L	80009	175-0371-00
-23	131-1563-00		2	.TERM,QIK DISC.:FEMALE ACCOM 0.25 X 0.037	00779	61198-3
-24	-----		1	POWER SUPPLY: (SEE REPL) (ATTACHING PARTS)		
-25	212-0122-00		2	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-26	118-4920-00		1	POWER SUPPLY INCLUDES .COVER,PMR SPLY: (ATTACHING PARTS)	54407	412-75876
-27	211-0507-00		2	.SCREN,MACHINE:6-32 X 0.312,PNH,STL (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-28	131-1688-00		1	.TERM,QIK DISC:MALE,0.032 X 0.25 BL,45 DEG .BEND	00779	42577-4
-29	255-0334-00		2	.PLASTIC CHANNEL:12.75 X 0.175 X 0.155	11897	122-37-2500
-30	352-0652-00		1	.HLDR,TERM CONN:1 X 15,M/O RAMP,TRIFUCON CO .NTACT	27264	26-03-3151
-31	131-2728-00		15	.CONN,TERMINAL:18-24 AWG,GOLD PLATED BRASS, .TRIFUCON	27264	08-58-0187
-32	343-0549-00		2	.STRAP,TIEDOWN,E:0.091 M X 4.0 L,ZYTEL	06383	PLT1W
-33	131-2214-00		15	.STRAIN RLF,TERM:CIRCUIT BOARD,22-24 AWG	27264	16-02-0037(4811)
-34	118-4921-00		1	.HEAT SINK,PMR: (ATTACHING PARTS)	54407	402-76192
-35	211-0578-00		6	.SCREN,MACHINE:6-32 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
-36	210-0005-00		6	.WASHER,LOCK:#6 EXT,0.02 THK,STL	78189	1106-00
-37	211-0513-00		4	.SCREN,MACHINE:6-32 X 0.625,PNH,STL	93907	880-00032-003
-38	210-0457-00		4	.NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00

REPLACEABLE MECHANICAL PARTS

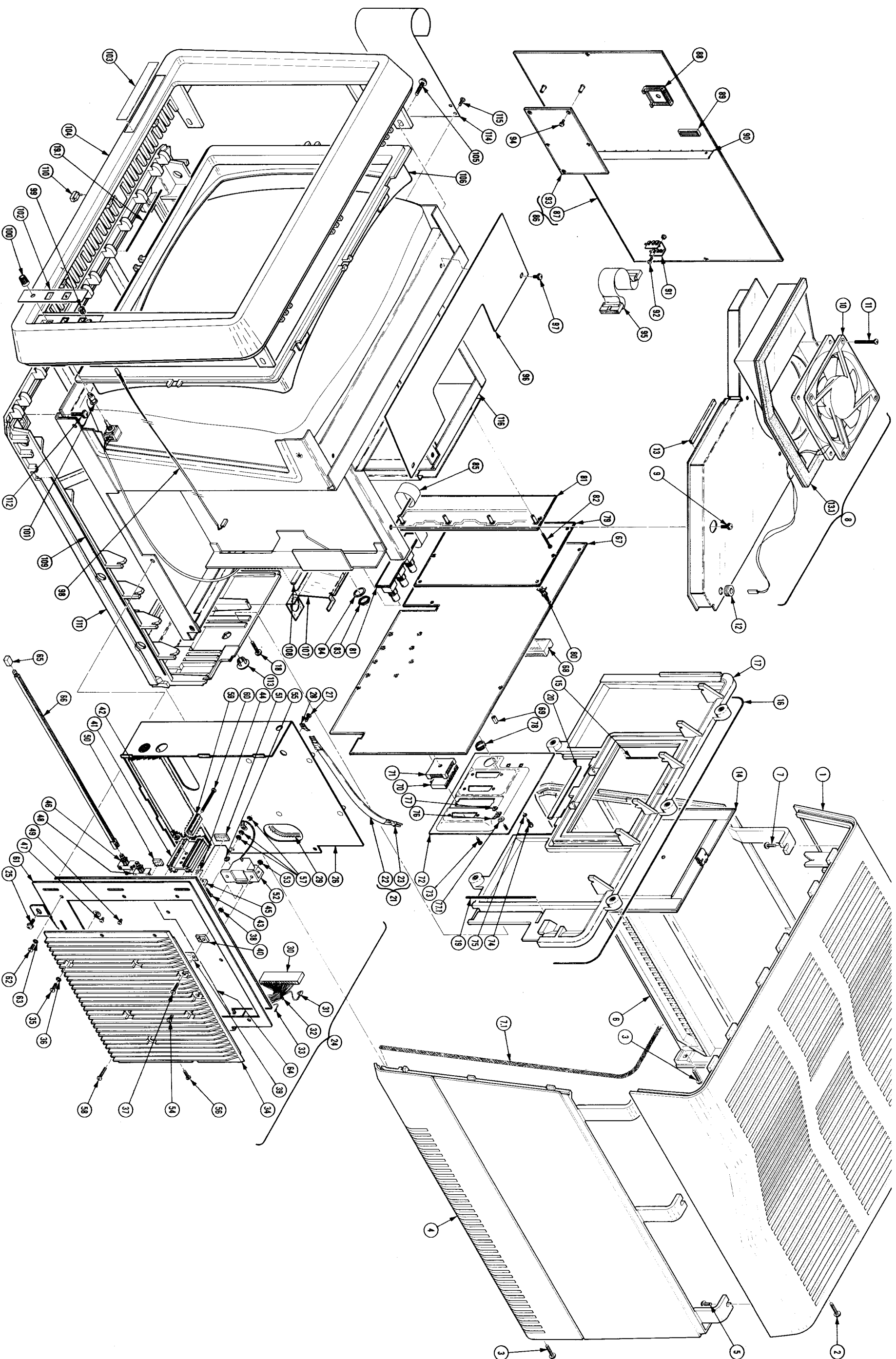
Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont		Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
1-						. (END OF ATTACHING PARTS)		
-39	118-4891-00			4		. INSULATOR:MICA	54407	320-21776
-40	118-4892-00			4		. INSULATOR:	54407	311-21810
-41	118-4889-00			1		. HEAT SINK,ELEC:2.0	54407	402-21345
						. (ATTACHING PARTS)		
-42	210-0586-00			1		. NUT,PL,ASSEM MA:4-40 X 0.25,STL CD PL	78189	211-041800-00
-43	211-0198-00			1		. SCREW,MACHINE:4-40 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-44	118-4891-00			1		. INSULATOR:MICA	54407	320-21776
-45	118-4890-00			1		. INSULATOR:TRANSISTOR	54407	320-21174
-46	118-4887-00			1		. SWITCH,PUSH:MOMENTARY,4A	54407	909-22227
						. (ATTACHING PARTS)		
-47	213-0088-00			2		. SCREW,TPG,TF:4-24 X 0.25,TYPE B,PNH	83385	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-48	260-2259-00			1		. SWITCH,PUSH:DPST,5A,250V	31918	N30X 2A
						. (ATTACHING PARTS)		
-49	213-0088-00			2		. SCREW,TPG,TF:4-24 X 0.25,TYPE B,PNH	83385	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-50	136-0727-00			1		. SKT,PL-IN ELEX:MICROCKT,8 CONTACT	09922	D1LB8P-108
-51	136-0728-00			1		. SKT,PL-IN ELEX:MICROCKT,14 CONTACT	09922	D1LB14P-108
-52	-----			1		. CONN,RCPT,ELEC:AC LINE W/WIRE		
						. (SEE REPL P1)		
						. (ATTACHING PARTS)		
-53	210-0457-00			2		. NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-54	211-0507-00			2		. SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-55	210-0457-00			2		. NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-56	211-0578-00			2		. SCREW,MACHINE:6-32 X 0.438,PNH,STL	TK0435	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-57	210-0457-00			3		. NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-58	211-0514-00			1		. SCREW,MACHINE:6-32 X 0.750,PNH,STL	TK0435	ORDER BY DESCR
-59	118-4888-00			1		. HEAT SINK,ELEC:1.25	54407	402-21412
						. (ATTACHING PARTS)		
-60	211-0553-00			1		. SCREW,MACHINE:6-32 X 1.5,PNH,STL	TK0435	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-61	118-4919-00			1		. CHAS,PMR SUPPLY:	54407	412-75875
						. (ATTACHING PARTS)		
-62	211-0507-00			3		. SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-63	210-0005-00			3		. WASHER,LOCK:#6 EXT,0.02 THK,STL	78189	1106-00
						. (END OF ATTACHING PARTS)		
-64	118-4922-00			1		. INSULATOR:POWER SUPPLY	54407	320-75895
-65	366-0554-00			2		PUSH BUTTON:SMOKE TAN,0.326 X 0.253 X 0.43	80009	366-0554-00
-66	384-0991-00			2		EXTENSION SHAFT:13.271 L X 0.244 OD,GREY PC	80009	384-0991-00
-67	-----			1		CIRCUIT BD ASSY:TERMINAL CONTROL		
						(SEE REPL)		
						TERMINAL CONTROL BOARD INCLUDES		
-68	136-0797-01			12		. SKT,PL-IN ELEX:MICROCKT,28 CONTACT	80009	136-0797-01
-69	366-1559-01			2		. PUSH BUTTON:GRAY,0.18 SQ X 0.43	80009	366-1559-01
-70	214-3803-00	8010100	8010687	1		. HEAT SINK,ELEC:FINNED,68 PIN SKT	30161	58328
-71	136-0813-00	8010100	8010687	1		. SKT,PL-IN ELEX:CHIP CARRIER,68 CONTACTS	19613	268-5400-00-1102
-72	386-5104-00			1		. PLATE,CONN MTG:ALUMINUM	80009	386-5104-00
						. (ATTACHING PARTS)		
-73	211-0008-00			2		. SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-74	131-0890-01			6		. LOCK,CONNECTOR:4-40 X 0.312 L,HEX HD,STL C	00779	205818-2
						. D PL W/O WASHERS & HEX NUT		
-75	210-0054-00			6		. WASHER,LOCK:#4 SPLIT,0.025 THK STL	78189	ORDER BY DESCR
						. (END OF ATTACHING PARTS)		
-76	131-1369-00			1		. TERM,QIK DISC.:0.615 L X 0.25 M BLADE	80009	131-1369-00
						. (ATTACHING PARTS)		
-77	210-0406-00			1		. NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
-77.1	210-0004-00			1		. WASHER,LOCK:#4 INTL,0.015 THK,STL	77900	1204-00-00-0541C
						. (END OF ATTACHING PARTS)		
-78	131-3090-00			1		. CONTACT,ELEC:FINGER STRIP,CU-8E	TK0648	ORDER BY DESCR
-79	-----			1		CIRCUIT BD ASSY:RAM OPTION		
						(SEE REPL)		
						RAM OPTION BOARD INCLUDES		
-80	361-0801-00			1		. SPACER,CKT BD:0.415 NOM L,NYLON	06915	CBS-6M
-82	211-0018-00			2		. SCREW,MACHINE:4-40 X 0.875,PNH,STL	TK0435	ORDER BY DESCR

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont		Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
1-83	220-0497-00			3	NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
-84	210-0845-00			3	NASHER,FLAT:0.5 ID X 0.625 OD X 0.02,STL (END OF ATTACHING PARTS)	89663	634-R
					EXTERNAL VIDEO BOARD INCLUDES		
-85	175-9258-00			1	.CA ASSY,SP,ELEC:7 COND,6.0 L	80009	175-9258-00
-86	-----			1	CIRCUIT BD ASSY:DISPLAY CONTROLLER (SEE REPL)		
-87	670-8524-00			1	.CIRCUIT BD ASSY:DISPLAY CONTROLLER (SEE REPL)	80009	670-8524-00
	-----			1	.DISPLAY CONTROLLER BOARD INCLUDES		
-88	136-0871-00			1	..SKT,PL-IN ELEK:QUAD,68 PIN,M/SOLDER TAIL ..MOUNT	00779	821543-1
-89	136-0657-00			1	..SKT,PL-IN ELEK:MICROCKT,24 CONTACT	80009	136-0657-00
-90	124-0436-00			1	..BUS CONDUCTOR:CKT BD,14 TAB,9.1 L	80009	124-0436-00
-91	214-3036-00			1	..HEAT SINK,XSTR:TO-220,ALUMINUM ..(ATTACHING PARTS)	98978	7363-8A
-92	211-0008-00			1	..SCREEN,MACHINE:4-40 X 0.25,PNH,STL ..(END OF ATTACHING PARTS)	93907	ORDER BY DESCR
-93	-----			1	.CIRCUIT BD ASSY:CROSS HAIR CURSOR (SEE REPL)		
					..(ATTACHING PARTS)		
-94	211-0008-00			3	.SCREEN,MACHINE:4-40 X 0.25,PNH,STL ..(END OF ATTACHING PARTS)	93907	ORDER BY DESCR
-95	175-9830-00			1	CA ASSY,SP,ELEC:20,28 AWG,6.0 L,RIBBON	80009	175-9830-00
-96	337-3183-00			1	SHIELD,ELEC:EMI, TOP (ATTACHING PARTS)	80009	337-3183-00
-97	212-0122-00			2	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-98	198-5372-01	8010100	8010100	1	WIRE SET,ELEC:LED POWER INDICATOR,22.0 L (THROW RETAINING RING AWAY)	80009	198-5372-01
-99	352-0700-00	8010100	8010100	1	HOLDER,LED:PLASTIC,2 PIECE	58361	CWP52
-100	366-1833-00			1	KNOB:GRAY,0.25 ID X 0.392 OD X 0.466 H	80009	366-1833-00
-101	377-0512-01			1	INSERT,KNOB:0.172 ID X 0.28 OD X 0.64,NYL	80009	377-0512-01
-102	334-5430-00	8010100	8010100	1	MARKER,IDENT:MKO POWER OFF/ON	80009	334-5430-00
	334-5430-01	8010100		1	MARKER,IDENT:MKO POWER ON/OFF	80009	334-5430-01
-103	334-6312-00			1	MARKER,IDENT:MKO TEKTRONIX 4111 MOLDED M/AD HESIVE BACK	80009	334-6312-00
-104	333-3106-02			1	PANEL,FRONT: (ATTACHING PARTS)	80009	333-3106-02
-105	212-0115-00			4	SCR,ASSEM MSHR:8-32 X 0.75,PNH,STL,POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-106	331-0384-12			1	MASKS,CRT ASSY:COMBINED INNER & OUTER MASK	80009	331-0384-12
-107	378-0266-00			1	BAFFLE,AIR:INLET,REAR,BOTTOM	80009	378-0266-00
-108	131-0132-00			1	CONTACT,ELEC:FINGER STRIP	TK1099	97135X3.75INCH
-109	348-0836-02			2	SHLD GSKT,ELEC:14.75 L,+/- 0.250	80009	348-0836-02
-110	348-0513-00			2	FOOT,CABINET:BLACK POLYURETHANE	80009	348-0513-00
-111	200-2957-05			1	COVER,TERMINAL:BOTTOM (ATTACHING PARTS)	80009	200-2957-05
-112	212-0674-00			4	SCR,ASSEM MSHR:10-32 X 0.875,PNH,STL (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
					BOTTOM PAN INCLUDES		
-113	134-0180-00			1	.PLUG,BUTTON:0.812 X 0.328	80009	134-0180-00
-114	337-3306-01			2	SHIELD,ELEC:EMI (ATTACHING PARTS)	80009	337-3306-01
-115	212-0122-00			4	SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-116	-----			1	MONITOR:COLOR RASTER,19 INCH (SEE GMA303 MANUAL)		



FIG. 1 4111 OLD VERSION



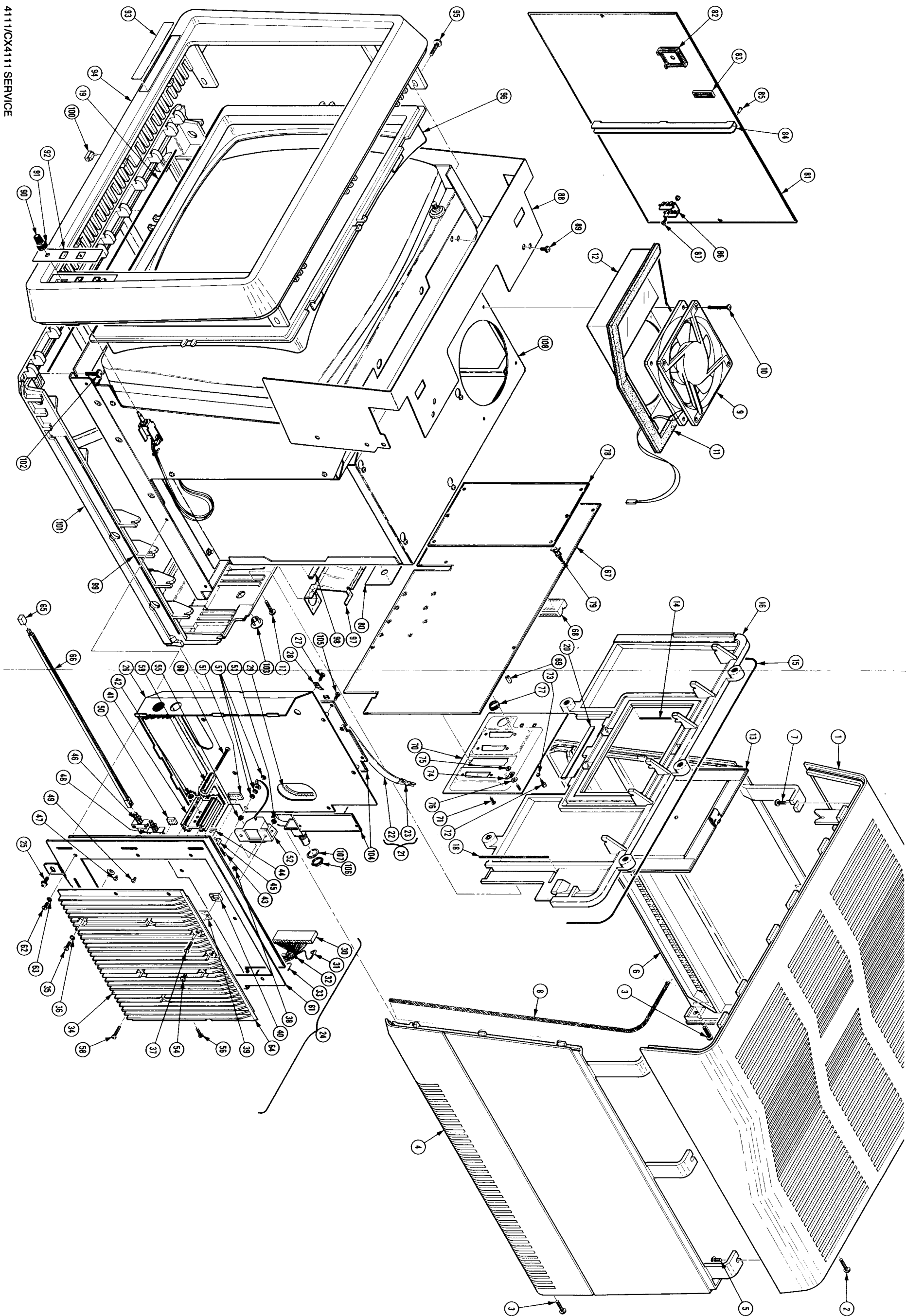


Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Qty	12345 Name & Description	Mfr. Code	Mfr. Part No.
2-1	200-2955-02		1	COVER, TERMINAL: TOP (ATTACHING PARTS)	80009	200-2955-02
-2	212-0115-00		3	SCR, ASSEM MSHR: 8-32 X 0.75, PNH, STL, POZ	01536	ORDER BY DESCR
-3	212-0674-00		2	SCR, ASSEM MSHR: 10-32 X 0.875, PNH, STL (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-4	386-5139-02		1	PANEL, SIDE: LEFT (ATTACHING PARTS)	80009	386-5139-02
-5	212-0122-00		3	SCR, ASSEM MSHR: 8-32 X 0.5, PNH, STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-6	386-5138-02		1	PANEL, SIDE: RIGHT (ATTACHING PARTS)	80009	386-5138-02
-7	212-0122-00		3	SCR, ASSEM MSHR: 8-32 X 0.5, PNH, STL POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-8	348-0836-04		1	SHLD GSKT, ELEK: 49.25 L, +/- 0.25	80009	348-0836-04
-9	-----		1	FAN, TUBE AXIAL: 12 VDC, 3.6W, 57 CEM (SEE CHASSIS PARTS 81001) (ATTACHING PARTS)		
-10	212-0037-00		4	SCREW, MACHINE: 8-32 X 1.75, FILH, STL (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-11	348-0901-00		1	GASKET, SEAL: 0.250 THK X 0.50 WIDE X 25 FEET PORON 4716-16, M/PRESS	80009	348-0901-00
-12	378-0264-01		1	BAFFLE, AIR: EXIT, FAN M/ADH SEAL GASKET	80009	378-0264-01
-13	200-3125-01		1	COVER, CKT 80:	80009	200-3125-01
-14	348-0932-00		2	SHLD GSKT, ELEK: 4.5 L, +/- 0.250	80009	348-0932-00
-15	348-0836-01		1	SHLD GSKT, ELEK: 32.25 L, +/- 0.250	80009	348-0836-01
-16	333-3206-01		1	PANEL, REAR: (ATTACHING PARTS)	80009	333-3206-01
-17	212-0115-00		2	SCR, ASSEM MSHR: 8-32 X 0.75, PNH, STL, POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-18	348-0836-00		3	SHLD GSKT, ELEK: 4.5 L	80009	348-0836-00
-19	348-0836-03		1	SHLD GSKT, ELEK: 19.75 L, +/- 0.25	80009	348-0836-03
-20	131-0132-00		1	CONTACT, ELEC: FINGER STRIP	TK1099	97135X3.75INCH
-21	196-3062-00		1	LEAD, ELECTRICAL: 10 AWG, 8.0 L, BRAID N/BLACK PVC JKT	80009	196-3062-00
-22	175-0371-00		1	.CA ASSY, SP, ELEC: 4.30 AWG, 108.0 L	80009	175-0371-00
-23	131-1563-00		2	.TERM, QIK DISC.: FEMALE ACCOM 0.25 X 0.037	00779	61198-3
-24	-----		1	POWER SUPPLY: 4406/4111 (SEE REPL) (ATTACHING PARTS)		
-25	212-0122-00		2	SCR, ASSEM MSHR: 8-32 X 0.5, PNH, STL POZ (END OF ATTACHING PARTS) POWER SUPPLY INCLUDES	01536	ORDER BY DESCR
-26	337-3346-00		1	.SHIELD, ELEC: PMR SPLY (ATTACHING PARTS)	80009	337-3346-00
-27	211-0507-00		2	.SCREW, MACHINE: 6-32 X 0.312, PNH, STL (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-28	131-1688-00		1	.TERM, QIK DISC: MALE, 0.032 X 0.25 BL, 45 DEG .BEND	00779	42577-4
-29	255-0334-00		2	.PLASTIC CHANNEL: 12.75 X 0.175 X 0.155	11897	122-37-2500
-30	352-0652-00		1	.HLDR, TERM CONN: 1 X 15, N/O RAMP, TRIFUCON CO .NTACT	27264	26-03-3151
-31	131-2728-00		15	.CONN, TERMINAL: 18-24 AWG, GOLD PLATED BRASS, .TRIFUCON	27264	08-58-0187
-32	343-0549-00		2	.STRAP, TIEDOWN, E: 0.091 M X 4.0 L, ZYTEL	06383	PLT1M
-33	131-2214-00		15	.STRAIN RLF, TERM: CIRCUIT BOARD, 22-24 AWG	27264	16-02-0037(4811)
-34	118-4921-00		1	.HEAT SINK, PMR: (ATTACHING PARTS)	54407	402-76192
-35	211-0578-00		6	.SCREW, MACHINE: 6-32 X 0.438, PNH, STL	TK0435	ORDER BY DESCR
-36	210-0005-00		6	.WASHER, LOCK: #6 EXT, 0.02 THK, STL	78189	1106-00
-37	211-0513-00		4	.SCREW, MACHINE: 6-32 X 0.625, PNH, STL	93907	880-00032-003
-38	210-0457-00		4	.NUT, PL, ASSEM MA: 6-32 X 0.312, STL CO PL (END OF ATTACHING PARTS)	78189	511-061800-00
-39	118-4891-00		4	.INSULATOR: WICA	54407	320-21776
-40	118-4892-00		4	.INSULATOR:	54407	311-21810
-41	118-4889-00		1	.HEAT SINK, ELEC: 2.0 (ATTACHING PARTS)	54407	402-21345
-42	210-0586-00		1	.NUT, PL, ASSEM MA: 4-40 X 0.25, STL CO PL	78189	211-041800-00

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
2-43	211-0198-00		1		.SCREW,MACHINE:4-40 X 0.438,PNH,STL (END OF ATTACHING PARTS)	TK0435	ORDER BY DESCR
-44	118-4891-00		1		.INSULATOR:MICA	54407	320-21776
-45	118-4890-00		1		.INSULATOR:TRANSISTOR	54407	320-21174
-46	118-4887-00		1		.SWITCH,PUSH:MOMENTARY,4A (ATTACHING PARTS)	54407	909-22227
-47	213-0088-00		2		.SCREW,TPG,TF:4-24 X 0.25,TYPE B,PNH (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-48	260-2259-00		1		.SWITCH,PUSH:DPST,5A,250V (ATTACHING PARTS)	31918	N30X 2A
-49	213-0088-00		2		.SCREW,TPG,TF:4-24 X 0.25,TYPE B,PNH (END OF ATTACHING PARTS)	83385	ORDER BY DESCR
-50	136-0727-00		1		.SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
-51	136-0728-00		1		.SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-52	-----		1		.CONN,RCPT,ELEC:AC LINE N/MIRE (SEE REPL P1) (ATTACHING PARTS)		
-53	210-0457-00		2		.NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-54	211-0507-00		2		.SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-55	210-0457-00		2		.NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-56	211-0578-00		2		.SCREW,MACHINE:6-32 X 0.438,PNH,STL (END OF ATTACHING PARTS)	TK0435	ORDER BY DESCR
-57	210-0457-00		3		.NUT,PL,ASSEM MA:6-32 X 0.312,STL CD PL	78189	511-061800-00
-58	211-0514-00		1		.SCREW,MACHINE:6-32 X 0.750,PNH,STL	TK0435	ORDER BY DESCR
-59	118-4888-00		1		.HEAT SINK,ELEC:1.25 (ATTACHING PARTS)	54407	402-21412
-60	211-0553-00		1		.SCREW,MACHINE:6-32 X 1.5,PNH,STL (END OF ATTACHING PARTS)	TK0435	ORDER BY DESCR
-61	118-4919-00		1		.CHAS,PMR SUPPLY: (ATTACHING PARTS)	54407	412-75875
-62	211-0507-00		3		.SCREW,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-63	210-0005-00		3		.WASHER,LOCK:#6 EXT,0.02 THK,STL (END OF ATTACHING PARTS)	78189	1106-00
-64	118-4922-00		1		.INSULATOR:POWER SUPPLY	54407	320-75895
-65	366-0554-00		2		PUSH BUTTON:SMOKE TAN,0.326 X 0.253 X 0.43	80009	366-0554-00
-66	384-0991-00		2		EXTENSION SHAFT:13.271 L X 0.244 OD,GREY PC	80009	384-0991-00
-67	-----		1		CIRCUIT BD ASSY:TERMINAL CONTROL (SEE REPL)		
-68	136-0797-01		12		TERMINAL CONTROL BOARD INCLUDES .SKT,PL-IN ELEK:MICROCKT,28 CONTACT	80009	136-0797-01
-69	366-1559-01		2		.PUSH BUTTON:GRAY,0.18 SQ X 0.43	80009	366-1559-01
-70	386-5104-00		1		.PLATE,CONN MTG:ALUMINUM (ATTACHING PARTS)	80009	386-5104-00
-71	211-0008-00		2		.SCREW,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-72	131-0890-01		6		.LOCK,CONNECTOR:4-40 X 0.312 L,HEX HD,STL C .D PL W/O WASHERS & HEX NUT	00779	205818-2
-73	210-0054-00		6		.WASHER,LOCK:#4 SPLIT,0.025 THK STL (END OF ATTACHING PARTS)	78189	ORDER BY DESCR
-74	131-1369-00		1		.TERM,QIK DISC.:0.615 L X 0.25 M BLADE (ATTACHING PARTS)	80009	131-1369-00
-75	210-0406-00		1		.NUT,PLAIN,HEX:4-40 X 0.188,BRS CD PL	73743	12161-50
-76	210-0004-00		1		.WASHER,LOCK:#4 INTL,0.015 THK,STL (END OF ATTACHING PARTS)	77900	1204-00-00-0541C
-77	131-3090-00		1		.CONTACT,ELEC:FINGER STRIP,CU-8E	TK0648	ORDER BY DESCR
-78	-----		1		CIRCUIT BD ASSY:RAM OPTION (SEE REPL) RAM OPTION BOARD INCLUDES		
-79	361-0801-00		1		.SPACER,CKT BD:0.415 NOM L,NYLON	06915	CBS-6M
-80	386-5482-00		1		.WASHER,PLATE:STL,SMOKE TAN	80009	386-5482-00
-81	-----		1		CIRCUIT BD ASSY:DISPLAY CONTROL (SEE REPL) (DISPLAY CONTROLLER BOARD INCLUDES)		
-82	136-0871-00		1		.SKT,PL-IN ELEK:QUAD,68 PIN,M/SOLDER TAIL M .OUNT	00779	821543-1
-83	136-0657-00		1		.SKT,PL-IN ELEK:MICROCKT,24 CONTACT	80009	136-0657-00
-84	386-5031-00		1		.STIF,CIRCUIT BD:9.1 L,ALUMINUM (ATTACHING PARTS)	80009	386-5031-00

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
2-85	210-3099-00		3		.RIVET,SOLID:0.187 L X 0.116 OD,DOME HD,ALU .MINUM	19738	75021-0406
-86	214-3036-00		1		.(END OF ATTACHING PARTS) .HEAT SINK,XSTR:T0-220,ALUMINUM	98978	7363-8A
-87	211-0008-00		1		.(ATTACHING PARTS) .SCREEN,MACHINE:4-40 X 0.25,PNH,STL	93907	ORDER BY DESCR
-88	337-3361-00		1		.(END OF ATTACHING PARTS) SHIELD,ELEC:EMI 4111	80009	337-3361-00
-89	212-0122-00		6		(ATTACHING PARTS) SCR,ASSEM MSHR:8-32 X 0.5,PNH,STL POZ	01536	ORDER BY DESCR
-90	366-0632-00		1		(END OF ATTACHING PARTS) KNOB:SMOKE TAN	80009	366-0632-00
-91	366-0633-00		1		KNOB:SMOKE TAN	80009	366-0633-00
-92	334-6730-00		1		MARKER,IDENT:MKD POKER ON/OFF	80009	334-6730-00
-93	334-6567-00		1		MARKER,IDENT:MKD TEKTRONIX CX4111	80009	334-6567-00
-94	333-3106-02		1		PANEL,FRONT: (ATTACHING PARTS)	80009	333-3106-02
-95	212-0115-00		4		SCR,ASSEM MSHR:8-32 X 0.75,PNH,STL,POZ (END OF ATTACHING PARTS)	01536	ORDER BY DESCR
-96	331-0384-12		1		MASKS,CRT ASSY:COMBINED INNER & OUTER MASK	80009	331-0384-12
-97	378-0266-00		1		BAFFLE,AIR:INLET,REAR,BOTTOM	80009	378-0266-00
-98	131-0132-00		1		CONTACT,ELEC:FINGER STRIP	TK1099	97135X3.75INCH
-99	348-0836-02		2		SHLD GSKT,ELEK:14.75 L,+/- 0.250	80009	348-0836-02
-100	348-0513-00		2		FOOT,CABINET:BLACK POLYURETHANE	80009	348-0513-00
-101	200-2957-05		1		COVER,TERMINAL:BOTTOM (ATTACHING PARTS)	80009	200-2957-05
-102	212-0674-00		4		SCR,ASSEM MSHR:10-32 X 0.875,PNH,STL (END OF ATTACHING PARTS) BOTTOM PAN INCLUDES	01536	ORDER BY DESCR
-103	134-0180-00		1		.PLUG,BUTTON:0.812 X 0.328	80009	134-0180-00
-104	670-9553-00		1		CIRCUIT BD ASSY:CX INTFC (ATTACHING PARTS)	80009	670-9553-00
-105	211-0507-00		4		SCREEN,MACHINE:6-32 X 0.312,PNH,STL	83385	ORDER BY DESCR
-106	220-0497-00		1		NUT,PLAIN,HEX:0.5-28 X 0.562 HEX,BRS CD PL	80009	220-0497-00
-107	210-0845-00		1		WASHER,FLAT:0.5 ID X 0.625 OD X 0.02,STL (END OF ATTACHING PARTS)	89663	634-R
-108	-----		1		MON,CLR DISPLAY: (SEE 119-2387-XX MANUAL)		

REPLACEABLE MECHANICAL PARTS

Fig. & Index No.	Tektronix Part No.	Serial/Assembly No. Effective Dscont	Qty	12345	Name & Description	Mfr. Code	Mfr. Part No.
3-					STANDARD ACCESSORIES		
-1	161-0066-00		1		CABLE ASSY,PMR,:3,18AWG,115V,96.0 L (STANDARD)	16428	CH8481, FH8481
-2	161-0066-09		1		CABLE ASSY,PMR,:3,0.75MM SQ,220V,99.0 L (OPTION A1 EUROPEAN)	53109	86511000
-3	161-0066-10		1		CABLE ASSY,PMR,:3,0.75MM SQ,240V,96.0 L (OPTION A2 UNITED KINGDOM)	TK1373	24230
-4	161-0066-11		1		CABLE ASSY,PMR,:3,0.75MM,240V,96.0 L (OPTION A3 AUSTRALIAN)	53109	ORDER BY DESCR
-5	334-3995-00		1		MARKER,IDENT:MARKED CAUTION (OPTION A3 ONLY)	80009	334-3995-00
-6	161-0066-12		1		CABLE ASSY,PMR,:3,18 AWG,250V,99.0 L (OPTION A4 NORTH AMERICAN)	70903	CH-77893
-7	161-0154-00		1		CABLE ASSY,PMR,:3,0.75MM SQ,240V,6A,2.5M L (OPTION A5 SWISS)	53109	86515000
	012-0911-00		1		CABLE,INTCON:144.0 L, RS 232	TK6020	ESF-85249
	062-7235-01		1		MANUAL,TECH:TO THE USER SURVEY CARD	80009	062-7235-01
	070-5142-02		1		MANUAL,TECH:REF,4115B	80009	070-5142-02
	070-5239-00		1		BOOK:INTRODUCTION TO COMPUTER COLOR GRAPHIC S	80009	070-5239-00
	070-5683-01		1		MANUAL,TECH:OPERATORS,4111	80009	070-5683-01
	070-5809-00		1		SHEET,TECHNICAL:INSTL,4111F2C (OPTION F2C ONLY)	80009	070-5809-00
	070-6084-00		1		MANUAL,TECH:USERS,CX4111	80009	070-6084-00
	070-6092-00		1		MANUAL,TECH:INSTL,4111F05	80009	070-6092-00
	334-3290-02		1		OVERLAY,KYBD:BLANK,SMOKE TAN	80009	334-3290-02
					OPTIONAL ACCESSORIES		
	012-1136-00		1		CABLE,INTCON:14,24 AWG,121.0 L	80009	012-1136-00
	013-0214-01		1		ADAPTER ASSY:COPIER LOOPBACK TEST FIXTURE F OR 410X 84111	80009	013-0214-01
	013-0218-00		1		ADAPTER ASSY:SELF TEST,25/15 PIN	80009	013-0218-00
	067-1043-00		1		FIXTURE,CAL:HOST PORT LOOP BACK CONN	80009	067-1043-00
	067-1221-00		1		FIXTURE,CAL:GENERATOR	80009	067-1221-00
	067-1244-00		1		FIXTURE,CAL:4111,GRATICULE	80009	067-1244-00
	067-1252-00		1		FIXTURE,CAL:4111,EXTENDER 80 AND CABLES	80009	067-1252-00
	070-4664-03		1		MANUAL,TECH:PROGRAMMERS,4110/4120 SERIES	80009	070-4664-03
	070-5141-01		1		MANUAL,TECH:REF,4110/4120 SERIES	80009	070-5141-01
	070-5215-00		1		MANUAL,TECH:SVCE,GMA302	80009	070-5215-00
	070-5276-00		1		MANUAL,TECH:4115/4120 SERIES SERIAL KEYBOAR D	80009	070-5276-00
	070-5644-01		1		MANUAL,TECH:SERVICE,4111/CX4111	80009	070-5644-01
	131-3371-00		1		CONN,RCPT,ELEC:D-SUBMIN,9 PIN,830PS	13511	FCC17E9AD-240

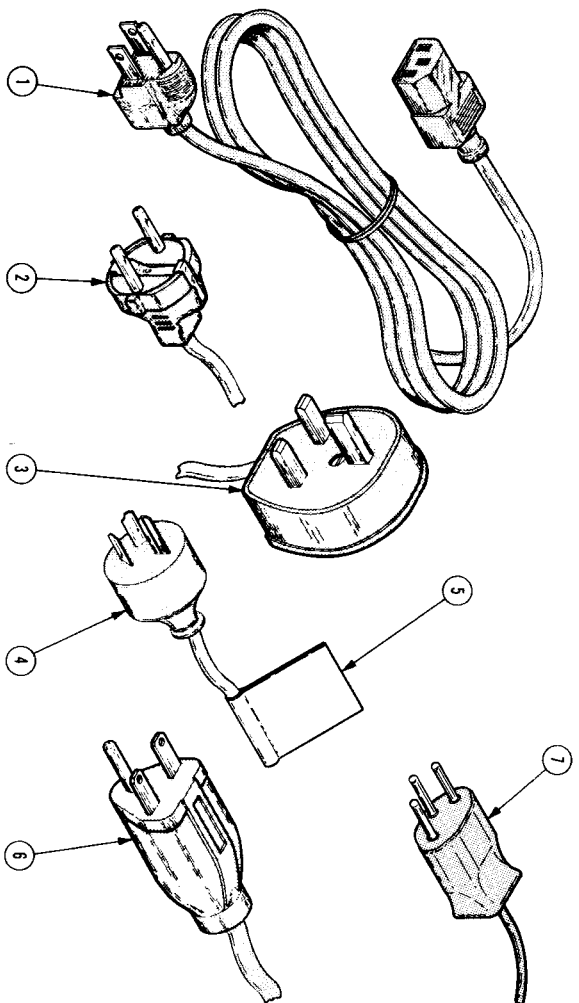


FIG. 3 ACCESSORIES



Appendix A

SIGNAL LIST

Table A-1 contains a list of all signals in the terminal, with the exception of signals unique to your specific Display module. Display module signals can be found in

either the *GMA302 Display Monitor Service Manual* or the *119-2387-00 Display Module Service Manual*.

Table A-1
SIGNAL LIST

Name	Description
1BNK-1	(One Bank) — Output of RAM Initialization circuitry on Terminal Control board. Held in a low state at all times.
256K-1	(256 K Memory) — Output of RAM Initialization circuitry on Terminal Control board. Held in a low state at all times.
2PAGE-0	(2 Pages of RAM Memory Present).
2XDCLK-1	(2 Times D Clock) — 33.8295 MHz, used by the blanking and sync delay registers (one half the frequency or twice the time of DCLK-1)
4PAGE-0	(4 Pages of RAM Memory Present).
ACK-0	(Acknowledge) — Processor acknowledge signal.
AD0-1 through AD19-1	(Processor Address/Data Bus) — AD0-1 through AD19-1 become LA0-1 through LA19-1 (Latched Address 0 through 19). These signals convey address information to all peripheral devices.
ADDCLK-1	(Address Clock) — Clock output of the State Machine, used by the FBC.
AH8-0	(Address High Byte, Bit 8) — The high bit of the low address byte.
AL8-0	(Address Low Byte, Bit 8) — The high bit of the low address byte.
ALE/QS0-1	(Address Latch Enable/Queue Status 0) — The bus timeout counter is held cleared when this signal is true (when the Address Latches are enabled).
ALPHAON-1	(Alpha On) — Enables character visibility.
ALTCOL0-1 through ALTCOL2-1	(Alternate Color 0 through 2) — Used to select one of eight Dialog area foreground/background color pairs.
ALURD-0	(ALU Read) — When true, signifies that the Processor wants to read the ALU Control Register.
ALUWR-0	(ALU Write) — When true, signifies that the Processor wants to write to the ALU Control Register.
AO0-1 through AO8-1	(Address Out, Bits 0 through 8) — The current RAM address.
AOCTLRD-0	(Alpha Overlay Read) — Enables alpha overlay control register.
AOCTLWR-0	(Alpha Overlay Write) — Enables alpha overlay control register.
ARS-0	(Alpha RAM Select) — When true, enables Alpha RAM.
BAD0-1 through BAD15-1	(Buffered Address/Data Bus) — The Buffered Address/Data Bus is the System Data Bus from the peripheral devices.
BCLK-1	(Buffered Clock) — System clock signal.
BDEN-0	(Buffered Data Enable) — Goes true when the Data Buffers on the Terminal Control board are enabled.
BDT/R-1	(Buffered Data Transmit/Receive) — Determines direction of data flow on RAM Option board data bus.
BELL-1	(Bell Tone) — Keyboard bell.

continued

SIGNAL LIST

Table A-1 (cont)
SIGNAL LIST

Name	Description
BEN-0	(Buffer Enable) — Enables the Data Buffers on the RAM Option board.
BHE-0	(Byte High Enable). BHE-0 becomes LBHE-0 (Latched Byte High Enable), which tells the Write Enable Logic on the Terminal Control board to enable the high byte of RAM for a write cycle.
BLINK-1	(Blink) — One of the character attributes.
BLUE	(Blue Input) — Blue input to Video Converter board.
BLUE + and BLUE-	(Blue Output) — Blue differential output of Video Converter board.
BPCS0-0	(Buffered Peripheral Chip Select 0) — Buffered PCS0-0.
BRD-0	(Buffered Read) — Buffered RD/QSMD-0.
BS-0	(Bank Select) — selects the RAM bank.
BS0-0 through BS2-0 and BS0-1 through BS2-1	(Buffered Status 0 through 2) — BS0 is true during write memory requests and BS1 is true during read memory requests. BS2 is false after a RESET to configure U380 to accept the STATUS inputs from the Processor as valid (as opposed to bus commands).
BUSY-1	(Copier Busy) — Color Copier is busy. Used in conjunction with FAULT-0.
BWR-0	(Buffered Write) — Buffered WR/QS1-0.
C0-1 and C1-1	(Command 0 and 1) — Outputs of the Command Register that set the mode of the State Machine (Vector mode, Rectangle mode, etc.)
CAACK-0	(Copier Acknowledge) — Color Copier acknowledges that it has received a COPY command.
CAS-0	(Column Address Strobe) — The column select signal for RAM access latching.
CAS0-0 through CAS2-0	(Column Address Strobe 0 through 2) — The column select signal for RAM access latching.
CHARCLK-0	(Character Clock).
CHARLTCH-0	(Character Latch).
CHDAT0-1 through CHDAT3-1	(Character Data 0 through 3).
CLKOUT-1	(Clock Output) — becomes BCLK-1 (Buffered Clock) and RAMCLK-1 (RAM Clock).
CMA0-1 through CMA3-1	(Color Map Address) — Color Map color intensity information inputs.
CMAPRD-0	(Color Map Read) — Enables the Color Map for a Processor read.
CMAWR-0 and CMAWR-1	(Color Map Write) — Enables the Color Map for a Processor write.
CNTRCLK-1	(Counter Clock) — 8.4574 MHz, used by the horizontal and vertical counters.
COL-0	(Column) — Selects the Address Multiplexer.
COMCLK-1	(Communications Clock) — 3.6864 MHz clock signal from the Communications Clock Circuit on the Terminal Control board.
COPINT-1	(Copier Interrupt) — A INT 3 level interrupt to the Processor from a Color Copier.
CTS	(Clear To Send) — RS-232 signal.
CURBLNK-0	(Cursor Blink) — Enables cursor blinking.
CURON-0	(Cursor On) — Turns cursor on.
CURSOR-1	(Cursor) — Character attribute (signifies that a character is actually a cursor).
D0-1 through D7-1	(Data 0 through 7) — Data inputs to the ALU Control Register.
DACBLANK-0	(Digital-Analog-Conversion Blanking) — The blanking control signal to the DAC.
DACCLK-1	(Digital-Analog-Conversion Clock) — DAC clock signal.
DACCUR-0	(Digital-Analog-Conversion Cursor) — Signals a cursor for the DAC.
DACSYNC-0	(Digital-Analog-Conversion Synchronization) — The sync signal for the DAC.

continued

Table A-1 (cont)

SIGNAL LIST

Name	Description
DCBLANK-0	(Display Control Blank) — Used with DCLKB-0 by the X Address Counters to provide the count for the X crosshair address.
DCD	(Data Carrier Detect) — RS-232 signal.
DCLK-1	(Data Clock) — 67.659 MHz, used by the Pixel Data Shift Register.
DCLKA-1	(Data Clock A) — 67.659 MHz, used by the Pixel Data Pipe Line Registers.
DCLKB-0 and DCLKB-1	(Display Clock B) — Used with DCBLANK-0 by the X Address Counters to provide the count for the X crosshair address.
DCSYNC-0	(Display Control Synchronization) — Composite sync signal.
DDACLK-1	(DDA Clock) — 4.2287 MHz, used by the Vector Generator circuitry.
DDACLKEN-0	(DDA Clock Enable) — State Machine clock.
DDARD-0	(DDA Read) — Enables internal read registers of the FBC.
DDAWR-0	(DDA Write) — Enables internal write registers of the FBC.
DEN-0	(Data Enable) — becomes BDEN-0 (Buffered Data Enable).
DIALON-1	(Dialog On) — Enables the Dialog area.
DMARRQ-1	(Direct Memory Access Read Request) — Notifies the Processor internal DMA controller when a DMA read is to occur.
DMAWRQ-1	(Direct Memory Access Write Request) — Notifies the Processor internal DMA controller when a DMA write is to occur.
DSR	(Data Set Ready) — RS-232 signal.
DT/R-0 and DT/R-1	(Data Transmit/Receive) — becomes BDT/R-0 and BDT/R-1 (Buffered Data Transmit/Receive).
DTR	(Data Terminal Ready) — RS-232 signal.
E2RDY-1	(EEROM Ready)
EN86ACC-0	(Enable 80186 Access) — Pixel Read Registers acknowledge signal.
ENBLNK-0	(Enable Blink) — Enables the characters blink function.
FAN	(Fan) — 12 Vdc fan output.
FAULT-0	(Fault) — when true, indicates a Color Copier error. Used in conjunction with BUSY-1.
FBCBUSY-1	(Frame Buffer Controller Busy) — Frame Buffer Controller IC (U226) busy.
FBCCMD-0	(Frame Buffer Control Command) — Enables mode control and FBC command register.
FBISMCLK-1	(Frame Buffer Interface State Machine Clock) — 16.9148 MHz, used by the Display Memory Control State Machine.
GREEN	(Green Input) — Green input to Video Converter board.
GREEN + and GREEN-	(Green Output) — Green differential output of Video Converter board.
HSTINT-1	(Host Interrupt) — A Level 0 interrupt from the host communications circuitry.
HSYNC-0	(Horizontal Synchronization)
IMAPRD-0	(Index Map Read) — Enable Index Map read register.
IMAPWR-0 and IMAPWR-1	(Index Map Write) — Enables Index Map write register.
INPRIME-0	(Input Prime) — Notification to a Color Copier that the terminal is ready to copy.
INV-1	(Inverse) — Character attribute.

continued

SIGNAL LIST

Table A-1 (cont)

SIGNAL LIST

Name	Description
INT0-1 through INT3-1	(Interrupt Levels 0 through 3) — Processor interrupts.
IOADREN-0	(I/O Address Enable) — Enables the output of the Address Latches when true.
IORC-0	(I/O Read Command) — When RD/QSMD-0 (Read/Queue Status Memory Data) is true and M/I/O-1 is false, IORC-0 is true (an I/O read cycle is in progress).
IORDWR-1	(I/O Read/Write) — Signals an I/O read or write cycle.
IOWC-0	(I/O Write Command) — When WR/QS1-0 (Write Strobe/Queue Status 1) is true and M/I/O-1 (Memory or I/O) is false, IOWC-0 is true (an I/O write cycle is in progress).
IR/S0-1	(Image Relationship/Serial Output) — Specifies image/medium relationship of color copier. In response to a STATUS command, sends a serial copier status report.
KBDINT-1	(Keyboard Interrupt) — A Level 1 interrupt from the Keyboard Controller.
KBRDATA-1	(Keyboard Read Data) — Data from keyboard to the Keyboard Controller.
KBRESET-0	(Keyboard Reset) — Resets Keyboard Processor.
KBTDATA-1	(Keyboard Transmit Data) — Keyboard data from the Keyboard Controller to the Keyboard.
KEYTST-1	(Key Test) — A Self-test signal that allows the keyboard circuitry to test character transmission and reception without using the actual keyboard key circuitry.
LA0-1 through LA19-1	(Latched Address Bus) — Become PA0-1 — PA7-1 (Processor Address 0 through 7). Carry the lower half of the address information from the Processor.
LBHE-0	(Latched Byte High Enable) — Tells the Write Enable Logic on the Terminal Control board to enable the high byte of RAM for a write cycle.
LOWRAMACK-0	(Low RAM Acknowledge) — Clocks the qualifying signals from the Write Enable Logic for the low RAM.
LS0-0 and LS1-0	(Latched Status 0 & 1) — During Processor HALTS and when no bus cycles are in process, these signals are both false, holding the counter cleared. During memory /I/O write cycles, S0-0 is true, and during memory /I/O read cycles, S1-0 is true. A Processor instruction fetch causes both signals to go true. Either or both signals becoming true enables the bus timeout counter.
LTCH86-1	(Latch 80186) — Latches data into the 186 Pixel Read Back Latches.
M/I/O-1	(Memory or I/O) — Notifies all peripheral devices whether a memory or I/O cycle is in progress.
MAJEXT-0	(Major Extent) — Enables major extent/rectangle X extent register.
MPCS-0	(Multiplier Chip Select) — Enables multipliers.
MRDC-0	(Memory Read Command) — When RD/QSMD-0 and M/I/O-1 are both true, MRDC-0 is true (a memory read cycle is in progress).
MW-0	(Memory Write) — Strokes data into Display Memory.
MWRC-0	(Memory Write Command) — When WR/QS1-0 and M/I/O-1 are both true, MWRC-0 is true (a memory write cycle is in progress).
OPAQ-1	(Opaque) — Character attribute.
OVLYLDCLK-1	(Overlay Load Clock) latches the row address (V9-1 through V4-1 — Vertical 9 through 4) into the Alpha RAM Address Generator at the beginning of each line refresh.
P0-1 through P3-1	(Page 0 through Page 3) — RAM page numbers.
PA0-1 through PA7-1	(Processor Address Bus) — Buffered LA0-1 — LA7-1.
PCS0-0 through PCS4-0 and PCS6-0	(Peripheral Chip Selects 0 through 4, and 6) — Processor generated chip selects.
PD0-1 through PD15-1	(Processor Data Bus) — Buffered AD0-1 — AD15-1.
PDI	(Program Data Input) — The nine serial data bits from the RAM Initialization Logic on the Terminal Control board.
PE-0	(Peripheral Enable) — Enables the RAM Controller on the RAM Option board.

continued

Table A-1 (cont)
SIGNAL LIST

Name	Description
PIX-0	(Pixel) — Enables the Pixel Register when true.
PIXELRD-0	(Pixel Read) — Enables pixel data register.
PPIINT-1	(Peripheral Port Interrupt) — A Level 2 interrupt from the 2PP1 interface.
RAMACK-0 and RAMACK-1	(RAM Acknowledge) — Clocks the flip-flops in the Write Enable Logic.
RAMCLK-1	(RAM Clock) — Clocks the register in the Wait State Generator.
RAMSCLKEN-0	(RAM Shift Clock Enable) — Enables strobe for RAMSCLK-1.
RAS-0	(Row Address Strobe) — The row select signal for RAM refreshing and access latching.
RAS0-0 through RAS2-0	(Row Address Strobe 0 through 2) — The row select signal for RAM refreshing and access latching.
RCK-0	(Register Clock) — Clocks the Page Register on the RAM Option board and creates ACK-0.
RDATA	(Receive Data) — RS-232 signal.
RDMWR-0	(Read/Modify/Write) — When true, causes the state machine to perform a read/modify/write to Display Memory.
RD/QSMD-0	(Read/Queue Status Memory Data) — becomes BRD-0 (Buffered Read).
RECYEXT-0	(Rectangle Y Extent) — Enables rectangle Y extent register.
RED	(Red Input) — Red input to Video Converter board.
RED + and RED-	(Red Output) — Red differential output of Video Converter board.
RESET-0 and RESET-1	(System Reset) — Resets circuitry to default (power-up) conditions.
RFSHREQ-0	(Refresh Request) — Requests a refresh cycle.
RSTOUT-0	(Reset Out) — Asynchronous reset signal.
RTS	(Request To Send) — RS-232 signal.
S0-0 through S2-0	(Status 0 through 2) — S0-0 and S1-0 become LS0-0 and LS1-0 (Latched Status 0 & 1), which clear the Wait State Generator and the Bus Timeout Circuit. S2-0 becomes M/IO-1 (Memory or I/O), which tells all peripheral devices whether a memory or I/O cycle is in progress.
SCRNTIM-0	(Screen Timing) — Output of the Horizontal & Vertical Counters and Control Logic.
SDCD	(Secondary Data Carrier Detect) — RS-232 signal.
SELECT-1	(Select) — When true, indicates a Color Copier is present.
SOE0-0 through SOE2-0	(Shift Output Enable) — Enables the output of the shift registers of the Display Memory.
SRCLK0-1 through SRCLK3-1	(Shift Register Clock) — Clocks the Display Memory shift registers.
SRLD-0 and SRLD-1	(Shift Register Load) — 16.9148 MHz, used by the Pixel Data Shift Registers.
SRTS(A)	(Secondary Request To Send) — RS-232/A signal.
SRTS(C)	(Secondary Request To Send) — RS-232/C signal.
STAT0-1, STAT3-1, and STAT5-1	(Status) — Outputs of the Status Register.
STEST-0	(Self-test) — Notifies circuitry that the Self-test program is in process.

continued

SIGNAL LIST

Table A-1 (cont)

SIGNAL LIST

Name	Description
STROBE-0	(Strobe) — Strokes output data to a color copier, if present.
TDATA	(Transmit Data) — RS-232 signal.
TMROUT0-1	(Processor Timer Output 0) — Becomes BELL-1 (Bell Tone).
TRQE-0	(Transfer/Queue Enable) — When true, signifies a read/modify/write cycle; when false, a refresh cycle.
UDL-1	(Underline) — Character attribute.
V0-1 through V9-1	(Vertical 0 through 9) — Character Row Address bus.
VBLANK-0	(Vertical Blanking) — Blanking for vertical retrace.
VSYNC-0	(Vertical Synchronization) — Vertical sync signal for the Display Module.
WAIT3-1	(Wait 3) — Insert 3 wait states.
WE-0	(Write Enable) — Output of the RAM Controller that combines with outputs from the Write Enable Logic to create WEH-0 (Write Enable High Byte) and WEL-0 (Write Enable Low Byte).
WEA0-0 through WEA3-0	(Write Enable A) — Write enable for the RAMs in memory Plane 0.
WEB0-0 through WEB3-0	(Write Enable B) — Write enable for the RAMs in memory Plane 1.
WEC0-0 through WEC3-0	(Write Enable C) — Write enable for the RAMs in memory Plane 2.
WED0-0 through WED3-0	(Write Enable D) — Write enable for the RAMs in memory Plane 3.
WEH-0	(Write Enable High Byte) — Enables high byte of RAM for a write.
WEL-0	(Write Enable Low Byte) — Enables low byte of RAM for a write.
WRCLR-1	(Write Clear) — Clears the flip-flops that load the X and Y Counters.
WR/QS1-0	(Write/Queue Status 1) — becomes BWR-0 (Buffered Write).
X0-1 through X10-1	(X Address 0 through 10).
XADDRD-0	(X Address Read) — Enables the X0-1 — X10-1 and Y0-1 — Y4-1 Address Read Back Latches when true.
XCURSEN-0	(X Cursor Enable) — Enable for the Cursor board.
XCURSWR-0	(X Cursor Write) — Enables crosshair cursor X address register.
XLD-1	(X Load) — Loads the X registers in the FBC.
Y0-1 through Y10-1	(Y Address 0 through 10).
YADDRD-0	(Y Address Read) — Enables pixel address read register for Self-test.
YCURSWR-0	(Y Cursor Write) — Enables crosshair cursor Y address register.
YEP-0	(Yes, an Option is Present) — Held true when an option is connected to the Option Interface Bus.
YUPEN-1	(Y Up Enable) — Enables the Y registers in the FBC.

Appendix B

PAL INFORMATION

INTRODUCTION

This section contains the following information on Programmed Logic Array (PAL) ICs used in the 4111 and CX4111:

- Location
- Pin-out
- Input and output signals
- Equations

Note that the newer circuit layout of the Display Control board (670-9725-nn) uses the same PALs as the older version Display Control Board (670-8524-nn). The only exception is that “U” numbers of ICs on the newer board have changed. The following cross reference lists the equivalent circuit numbers for the two versions of the Display Control board (schematic pages are listed for each PAL).

In the following PAL equations, a “*” (asterisk) is used to denote a logic AND function. The equations are given so that the named signal is true when the input signals are in the state given.

As an example:

$$XXX \text{ (true)} = A1 \text{ (true)} * B1 \text{ (false)} * C1 \text{ (true)}$$

XXX is the name of the signal being described. For XXX to be true, input signals A1 and C1 must be true and input signal B1 must be false.

EQUIVALENT PAL ICs FOR DISPLAY CONTROL BOARDS

670-8524-nn Board (old version)	670-9725-nn Board (newer version)
U212 (DSPLCTL-3)	U611 (NEWDC-22)
U214 (DSPLCTL-3)	U612 (NEWDC-22)
U220 (DSPLCTL-3)	U615 (NEWDC-22)
U286 (DSPLCTL-10)	U555 (NEWDC-6)
U348 (DSPLCTL-11)	U535 (NEWDC-2)
U464 (DSPLCTL-6)	U422 (NEWDC-14)
U467 (DSPLCTL-6)	U425 (NEWDC-14)
U470 (DSPLCTL-5)	U465 (NEWDC-10)
U478 (DSPLCTL-5)	U461 (NEWDC-10)

TERMINAL CONTROL BOARD

U292

Table B-1
U292 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	256K-1
2	1BNK-1
3	LA19-1
4	LA18-1
5	LA15-1
6	LA14-1
7	LA6-1
8	LA5-1
9	LA1-1
10	P2-1
11	P1-1
13	P0-1
14	PCS1-0
16	STAT5-1
23	M/IO-1

Table B-2
U292 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	ECS-0
17	SCS-0
18	MCS-0
19	PE-0
20	BS-0
21	AL8-0
22	AH8-0

Pin 12 is ground; Pin 24 is Vcc.

Equations

$$\text{ECS-0 (true)} = \text{M/IO-1 (false)} * \text{LA15-1 (false)} * \text{LA14-1 (true)}$$

$$\text{SCS-0 (true)} = \text{PCS1-0 (true)} * \text{LA6-1 (true)} * \text{LA5-1 (false)}$$

$$\text{MCS-0 (true)} = \text{PCS1-0 (true)} * \text{LA6-1 (false)}$$

$$\begin{aligned} \text{PE-0 (true)} &= \text{STAT5-1 (true)} * \text{M/IO-1 (true)} * \text{LA19-1 (true)} * \\ &\quad \text{LA18-1 (true)} * \text{256K-1 (true)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (true)} * \text{M/IO-1 (true)} * \text{LA19-1 (true)} * \\ &\quad \text{LA18-1 (false)} * \text{256K-1 (true)} * \text{1BNK-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (true)} * \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \\ &\quad \text{LA18-1 (true)} * \text{256K-1 (true)} * \text{1BNK-1 (false)} * \\ &\quad \text{P2-1 (false)} * \text{P1-1 (false)} * \text{P0-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \\ &\quad \text{LA18-1 (true)} * \text{256K-1 (true)} * \text{P2-1 (false)} * \text{P1-1} \\ &\quad \text{(false)} * \text{P0-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \\ &\quad \text{LA18-1 (true)} * \text{256K-1 (true)} * \text{1BNK-1 (false)} * \\ &\quad \text{P2-1 (false)} * \text{P1-1 (false)} * \text{P0-1 (true)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \\ &\quad \text{LA18-1 (true)} * \text{256K-1 (true)} * \text{1BNK-1 (false)} * \\ &\quad \text{P2-1 (false)} * \text{P1-1 (true)} * \text{P0-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (false)} \\ \text{AL8-0 (true)} &= \text{LA18-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ &\quad \text{256K-1 (true)} * \text{1BNK-1 (false)} * \text{P2-1 (false)} * \\ &\quad \text{P1-1 (false)} * \text{P0-1 (true)} \\ \\ \text{AH8-0 (true)} &= \text{1BNK-1 (true)} * \text{LA1-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (true)} * \text{LA19-1 (false)} * \text{1BNK-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{LA19-1 (false)} * \text{LA18-1 (false)} \\ &\quad * \text{1BNK-1 (false)} \\ &\quad \text{OR} \\ &\quad \text{STAT5-1 (false)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ &\quad \text{1BNK-1 (false)} * \text{P2-1 (false)} * \text{P1-1 (false)} * \\ &\quad \text{P0-1 (false)} \\ \\ \text{BS-0 (true)} &= \text{1BNK-1 (true)} \\ &\quad \text{OR} \\ &\quad \text{1BNK-1 (false)} * \text{LA1-1 (false)} \end{aligned}$$

U322

Table B-3
U322 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	LA19-1
2	LA18-1
3	LA17-1
4	LA16-1
5	LA15-1
6	LA14-1
7	LA13-1
8	M/IO-1
9	STAT5-1
10	DEN-0
11	PCS3-0

Table B-4
U322 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	ARS-0
16	DEO-0
17	A-0
18	B-0
19	C-0
20	D-0
21	E-0
22	F-0

Pin 12 is ground; Pin 24 is Vcc; Pins 13, 14, and 23 are not connected.

Equations

$$\text{DEO-0 (true)} = \text{LA19-1 (false)} * \text{DEN-0 (true)} * \text{PCS3-0 (false)}$$

OR

$$\text{LA18-1 (true)} * \text{DEN-0 (true)} * \text{PCS3-0 (false)}$$

OR

$$\text{LA17-1 (true)} * \text{DEN-0 (true)} * \text{PCS3-0 (false)}$$

$$\text{ARS-0 (true)} = \text{M/IO-1 (false)} * \text{LA15-1 (true)} * \text{LA14-1 (true)} * \text{LA13-1 (false)}$$

OR

$$\text{M/IO-1 (false)} * \text{LA15-1 (true)} * \text{LA14-1 (false)}$$

$$\text{A-0 (true)} = \text{STAT5-1 (false)} * \text{M/IO-1 (true)} * \text{LA19-1 (true)} * \text{LA18-1 (false)} * \text{LA17-1 (true)} * \text{LA16-1 (false)}$$

B-0 (true) = STAT5-1 (false) * M/IO-1 (true) * LA19-1 (true) *
LA18-1 (false) * LA17-1 (true) * LA16-1 (true)

C-0 (true) = STAT5-1 (false) * M/IO-1 (true) * LA19-1 (true) *
LA18-1 (true) * LA17-1 (false) * LA16-1 (false)

D-0 (true) = STAT5-1 (false) * M/IO-1 (true) * LA19-1 (true) *
LA18-1 (true) * LA17-1 (false) * LA16-1 (true)

E-0 (true) = STAT5-1 (false) * M/IO-1 (true) * LA19-1 (true) *
LA18-1 (true) * LA17-1 (true) * LA16-1 (false)

F-0 (true) = STAT5-1 (false) * M/IO-1 (true) * LA19-1 (true) *
LA18-1 (true) * LA17-1 (true) * LA16-1 (true)

RAM OPTION BOARD

U110

Table B-5
U110 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	LA2-1
2	LA3-1
3	LA4-1
4	LA5-1
5	LA6-1
6	LA19-1
7	LA18-1
8	LA1-1
9	BDEN-0
10	IOWC-1
11	M/IO-1
13	P2-1
14	P1-1
16	PCS1-0
17	1BNK-1
23	P0-1

Table B-6
U110 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	RCK-0
18	BEN-0
19	PE-0
20	BS-0
21	AL8-0
22	AH8-0

Pin 12 is ground; Pin 24 is Vcc.

Equations

$$\text{RCK-0 (true)} = \text{IOWC-0 (true)} * \text{PCS1-0 (true)} * \text{LA6-1 (true)} * \\ \text{LA5-1 (true)} * \text{LA4-1 (false)} * \text{LA3-1 (false)} * \\ \text{LA2-1 (false)} * \text{LA1-1 (false)}$$

$$\text{PE-0 (true)} = \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (false)} * \text{P1-1 (true)} * \text{P0-1 (true)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (false)} * \text{P0-1 (false)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (false)} * \text{P0-1 (true)} * \text{1BNK-1} \\ \text{(false)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (true)} * \text{P0-1 (false)} * \text{1BNK-1} \\ \text{(false)}$$

$$\text{BEN-0 (true)} = \text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (false)} * \text{P1-1 (true)} * \text{P0-1 (true)} * \text{BDEN-0} \\ \text{(true)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (false)} * \text{P0-1 (false)} * \text{BDEN-0} \\ \text{(true)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (false)} * \text{P0-1 (true)} * \text{1BNK-1} \\ \text{(false)} * \text{BDEN-0 (true)}$$

OR

$$\text{M/IO-1 (true)} * \text{LA19-1 (false)} * \text{LA18-1 (true)} * \\ \text{P2-1 (true)} * \text{P1-1 (true)} * \text{P0-1 (false)} * \text{1BNK-1} \\ \text{(false)} * \text{BDEN-0 (true)}$$

PAL INFORMATION

BS-0 (true) = 1BNK-1 (false) * LA1-1 (false)

OR

1BNK-1 (true)

AH8-0 (true) = LA19-1 (false) * LA18-1 (true) * P2-1 (false) *
P1-1 (true) * PO-1 (true) * 1BNK-1 (true) *
LA1-1 (false)

OR

LA19-1 (false) * LA18-1 (true) * P2-1 (true) *
P1-1 (false) * PO-1 (false) * 1BNK-1 (true) *
LA1-1 (false)

OR

LA19-1 (false) * LA18-1 (true) * P2-1 (false) *
P1-1 (true) * PO-1 (true) * 1BNK-1 (false)

OR

LA19-1 (false) * LA18-1 (true) * P2-1 (true) *
P1-1 (false) * PO-1 (false) * 1BNK-1 (false)

AL8-0 (true) = LA19-1 (false) * LA18-1 (true) * P2-1 (false) *
P1-1 (true) * PO-1 (true)

OR

LA19-1 (false) * LA18-1 (true) * P2-1 (true) *
P1-1 (false) * PO-1 (true) * 1BNK-1 (false)

DISPLAY CONTROL BOARD

U212

Table B-7

**U212 PIN-OUT AND
SIGNAL NAMES
(INPUTS)**

Pin Number	Signal Name
1	C0-1
2	C1-1
3	RECYEXT-1
4	PIXELRD-1
5	MAJEXT-1
6	SRCLK-1
7	YUPEN-1
8	XLD-1
9	ADDCLK-1
11	CNT2LD-1
12	GDDACLK-1
13	GDDASMCLK-1
19	RD-1

NOTE

The PALs of the newer Display Control board (670-9725-nn) use different IC "U" numbers than the PALs of the older version Display Control board (670-8524-nn). Refer to the cross reference at the beginning of this appendix to find equivalent circuit numbers for the newer version Display Control board.

Table B-8

**U212 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)**

Pin Number	Signal Name
14	DDACLK-0
15	CNT2CLK-0
16	ADDCLK-0
17	GO-0

Pin 10 is ground; Pin 20 is Vcc; Pin 18 is not connected.

Equations

$$GO-0 \text{ (false)} = C1-1 \text{ (false)} * MAJEXT-1 \text{ (false)}$$

OR

$$C1-1 \text{ (true)} * C0-1 \text{ (false)} * RECYEXT-1 \text{ (false)}$$

OR

$$C1-1 \text{ (true)} * C0-1 \text{ (true)} * PIXELRD-1 \text{ (false)}$$

$$ADDCLK-0 \text{ (false)} = SRCLK-1 \text{ (false)} * RD-1 \text{ (true)} * XLD-1 \text{ (false)} * YUPEN-1 \text{ (false)}$$

OR

$$SRCLK-1 \text{ (false)} * GDDACLK-1 \text{ (true)}$$

OR

$$RD-1 \text{ (false)} * GDDACLK-1 \text{ (true)}$$

$$DDACLK-0 \text{ (false)} = SRCLK-1 \text{ (false)} * GDDACLK-1 \text{ (true)}$$

$$CNT2CLK-0 \text{ (false)} = CNT2LD-1 \text{ (true)} * ADDCLK-1 \text{ (false)}$$

OR

$$GDDASMCLK-1 \text{ (true)} * ADDCLK-1 \text{ (false)}$$

U214

Table B-9
U214 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	CLK-1
2	GO-1
3	CO-1
4	C1-1
5	CNT2Z-1
6	CNT1Z-1

Table B-10
U214 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
12	C2LI-0
13	YUEI-0
14	AA-0
15	BB-0
16	CC-0
17	DD-0
18	RMW-0
19	DCI-0

Pins 10 and 11 are ground; Pin 20 is Vcc; Pins 7, 8, and 9 are not connected.

Equations

$$\begin{aligned}
 \text{DD-0 (true)} &= \text{GO-1 (false)} * \text{CO (true)} * \text{CC-0 (true)} * \text{BB-0 (true)} * \text{AA-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{DD-0 (true)} * \text{CC-0 (false)} * \text{BB-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{DD-0 (false)} * \text{CC-0 (true)} * \text{BB-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{CNT2Z-1 (true)} * \text{DD-0 (false)} * \text{CC-0 (true)} * \text{BB-0 (true)} \\
 \text{CC-0 (true)} &= \text{GO-1 (false)} * \text{C1-1 (true)} * \text{CO-1 (false)} * \text{DD-0 (true)} * \text{BB-0 (true)} * \text{AA-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{DD-0 (true)} * \text{CC-0 (true)} * \text{BB-0 (false)} * \text{AA-0 (false)} \\
 &\quad \text{OR} \\
 &\quad \text{DD-0 (true)} * \text{CC-0 (false)} * \text{BB-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{CNT2Z-1 (false)} * \text{DD-0 (false)} * \text{CC-0 (false)} * \text{BB-0 (true)} * \text{AA-0 (true)} \\
 &\quad \text{OR} \\
 &\quad \text{CNT2Z-1 (true)} * \text{DD-0 (false)} * \text{CC-0 (false)} * \text{BB-0 (true)} * \text{AA-0 (true)}
 \end{aligned}$$

BB-0 (true) = GO-1 (false) * C1-1 (false) * C0-1 (false) * DD-0 (true) * BB-0 (true) * AA-0 (true)

OR

DD-0 (true) * CC-0 (false) * BB-0 (false) * AA-0 (false)

OR

CNT2Z-1 (false) * DD-0 (false) * CC-0 (false) * BB-0 (true) * AA-0 (true)

OR

CNT2Z-1 (true) * DD-0 (true) * CC-0 (true) * BB-0 (true) * AA-0 (false)

OR

CNT2Z-1 (true) * DD-0 (false) * CC-0 (true) * BB-0 (false) * AA-0 (true)

AA-0 (true) = GO-1 (false) * C1-1 (false) * C0-1 (false) * CC-0 (true) * BB-0 (true) * AA-0 (true)

OR

DD-0 (true) * CC-0 (true) * BB-0 (false) * AA-0 (true)

OR

DD-0 (true) * CC-0 (false) * BB-0 (false) * AA-0 (false)

OR

DD-0 (false) * CC-0 (true) * BB-0 (true) * AA-0 (true)

OR

CNT1Z-1 (true) * DD-0 (false) * BB-0 (true) * AA-0 (true)

OR

CNT2Z-1 (true) * DD-0 (false) * CC-0 (true) * BB-0 (true)

OR

CNT2Z-1 (true) * DD-0 (false) * CC-0 (false) * BB-0 (true) * AA-0 (true)

PAL INFORMATION

C2LI-0 (true) = DD-0 (true) * CC-0 (true)
OR
DD-0 (false) * CC-0 (false)
OR
BB-0 (false)
OR
AA-0 (false)
DCI-0 (true) = DD-0 (true) * CC-0 (true) * AA-0 (false)
OR
BB-0 (true) * AA-0 (true)
OR
DD-0 (false) * CC-0 (false)
OR
CC-0 (false) * AA-0 (true)
OR
DD-0 (false) * BB-0 (false)
RMW-0 (true) = DD-0 (true) * AA-0 (true)
OR
CC-0 (true) * AA-0 (true)
OR
DD-0 (false) * AA-0 (false)
OR
CC-0 (false) * AA-0 (false)
OR
BB-0 (false)
YUEI-0 (true) = CC-0 (true) * AA-0 (true)
OR
DD-0 (false)
OR
BB-0 (true)
OR
CC-0 (false) * AA-0 (false)

U220

Table B-11
U220 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	GDDACLK-1
2	DCI-1
3	RMW-1
4	YUEI-1
5	C2LI-1
6	DD-1
7	CC-1
8	BB-1
9	AA-1

Table B-12
U220 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
12	RD-0
13	CNT2LD-0
14	CNT1CLK-0
15	XLD-1
16	YUPEN-0
17	SRCLK-0
18	FBCBUSY-0
19	PIX-0

Pin 10 is ground; Pin 20 is Vcc.

Equations

$$\text{PIX-0 (false)} = \text{RMW-1 (true)}$$

$$\text{FBCBUSY-0 (false)} = \text{DD-1 (true)} * \text{CC-1 (true)} * \text{BB-1 (true)} * \text{AA-1 (true)}$$

$$\text{CNT1CLK-0 (false)} = \text{DD-1 (false)}$$

OR

$$\text{CC-1 (false)}$$

OR

$$\text{BB-1 (true)}$$

OR

$$\text{AA-1 (true)}$$

$$\text{SRCLK-0 (false)} = \text{DCI-1 (false)}$$

$$\text{XLD-0 (false)} = \text{CC-1 (true)}$$

OR

$$\text{DD-1 (false)}$$

OR

$$\text{BB-1 (false)}$$

OR

$$\text{AA-1 (false)}$$

$$\text{YUPEN-0 (false)} = \text{YUEI-1 (false)}$$

$$\text{CNT2LD-0 (false)} = \text{C2LI-1 (true)}$$

$$\text{RD-0 (false)} = \text{DD-1 (false)} * \text{CC-1 (true)} * \text{BB-1 (true)} * \text{AA-1 (false)}$$

PAL INFORMATION

U286

Table B-13
U286 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	CHARCLKD-1
2	IORC-1
3	IOWC-1
4	ARS-1
5	DIALON-1
6	CAD0-1
7	OACK-1

Table B-14
U286 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
12	X-0
13	Y-0
14	CHARLTCH-0
15	REFRESH-0
16	ACK-0
17	CTL0-0
18	PWE-0
19	CTL1-0

Equations

Pins 10 and 11 are ground; Pin 20 is Vcc; Pins 8 and 9 are not connected.

$$Y-0 \text{ (false)} = \text{ARS-1 (false)} * \text{DIALON-1 (false)} * \text{IORC-1 (false)} * \\ \text{OACK-1 (false)} * Y-0 \text{ (true)} * X-0 \text{ (false)}$$

OR

$$\text{ARS-1 (false)} * \text{DIALON-1 (false)} * \text{IOWC-1 (false)} * \\ \text{OACK-1 (false)} * Y-0 \text{ (true)} * X-0 \text{ (false)}$$

OR

$$\text{ARS-1 (false)} * \text{CAD0-1 (false)} * \text{IORC-1 (false)} * \\ \text{OACK-1 (false)} * Y-0 \text{ (true)} * X-0 \text{ (false)}$$

OR

$$\text{ARS-1 (false)} * \text{CAD0-1 (false)} * \text{IOWC-1 (false)} * \\ \text{OACK-1 (false)} * Y-0 \text{ (true)} * X-0 \text{ (false)}$$

$$X-0 \text{ (false)} = \text{ARS-1 (false)} * \text{IORC-1 (false)} * \text{OACK-1 (false)} \\ * Y-0 \text{ (true)} * X-0 \text{ (true)}$$

OR

$$\text{ARS-1 (false)} * \text{IOWC-1 (false)} * \text{OACK-1 (false)} * \\ Y-0 \text{ (true)}$$

OR

$$\text{ARS-1 (false)} * \text{DIALON-1 (true)} * \text{CAD0-1 (true)} * \\ Y-0 \text{ (true)} * X-0 \text{ (false)}$$

$$\text{REFRESH-0 (false)} = \text{DIALON-1 (true)} * \text{CAD0-1 (true)}$$

$$\text{CHARLTCH-0 (false)} = \text{DIALON-1 (true)} * \text{CAD0-1 (true)}$$

CTL0-0 (false) = ARS-1 (false) * DIALON-1 (false) * OACK-1
(false) * IORC-1 (false) * Y-0 (true) * X-0
(false)

OR

ARS-1 (false) * DIALON-1 (false) * OACK-1
(false) * IOWC-1 (false) * Y-0 (true) * X-0
(false)

OR

ARS-1 (false) * CAD0-1 (false) * OACK-1 (false)
* IORC-1 (false) * Y-0 (true) * X-0 (false)

OR

ARS-1 (false) * CAD0-1 (false) * OACK-1 (false)
* IOWC-1 (false) * Y-0 (true) * X-0 (false)

OR

Y-0 (false) * X-0 (true)

CTL1-0 (false) = ARS-1 (false) * DIALON-1 (false) * OACK-1
(false) * IORC-1 (false) * Y-0 (true) * X-0
(false)

OR

ARS-1 (false) * DIALON-1 (false) * OACK-1
(false) * IOWC-1 (false) * Y-0 (true) * X-0
(false)

OR

ARS-1 (false) * CAD0-1 (false) * OACK-1 (false)
* IORC-1 (false) * Y-0 (true) * X-0 (false)

OR

ARS-1 (false) * CAD0-1 (false) * OACK-1 (false)
* IOWC-1 (false) * Y-0 (true) * X-0 (false)

PWE-0 (false) = ARS-1 (false) * DIALON-1 (false) * OACK-1 (false)
* IOWC-1 (false) * Y-0 (true) * X-0 (false)

OR

ARS-1 (false) * CAD0-1 (false) * OACK-1 (false) *
IOWC-1 (false) * Y-0 (true) * X-0 (false)

ACK-0 (false) = Y-0 (false)

U348

Table B-15
U348 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	FBISMCLK-1
2	UDL-1
3	BLINK-1
4	CURSOR-1
5	CURBLNK-1
6	BLINKON-1
7	DIALON-1
8	ENBLNK-1
9	CHARCLK-1
12	CL0-1
13	CL1-1
18	CL2-1
19	CL3-1

Table B-16
U348 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
14	CURUDL-0
15	CHAROFF-0
16	HORBLNK-0

Pins 10 and 11 are ground; Pin 20 is Vcc; Pin 17 is not connected.

Equations

$\text{CURUDL-0 (false)} = \text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CLO-1 (true)} * \text{UDL-1 (true)} * \text{BLINKON-1} \\
\text{(false)} * \text{ENBLNK-1 (false)} * \text{BLINK-1 (false)} \\
* \text{CHARCLK-1 (false)}$

OR

$\text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CLO-1 (true)} * \text{UDL-1 (true)} * \text{BLINK-1 (false)} \\
* \text{CHARCLK-1 (false)}$

OR

$\text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CLO-1 (true)} * \text{UDL-1 (true)} * \text{ENBLNK-1 (true)} \\
* \text{CHARCLK-1 (false)}$

OR

$\text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CURSOR-1 (true)} * \text{CURBLNK-1 (false)} * \\
\text{BLINKON-1 (false)} * \text{ENBLNK-1 (false)} * \\
\text{CHARCLK-1 (false)}$

OR

$\text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CURSOR-1 (true)} * \text{ENBLNK-1 (true)} * \text{CHARCLK-1} \\
\text{(false)}$

OR

$\text{CL3-1 (true)} * \text{CL2-1 (true)} * \text{CL1-1 (false)} * \\
\text{CURSOR-1 (true)} * \text{CURBLNK-1 (true)} * \text{CHARCLK-1} \\
\text{(false)}$

$\text{CHAROFF-0 (false)} = \text{DIALON-1 (true)} * \text{CHARCLK-1 (false)}$

OR

$\text{BLINKON-1 (true)} * \text{BLINK-1 (true)} * \text{ENBLNK-1} \\
\text{(false)} * \text{CHARCLK-1 (false)}$

OR

$\text{CHARCLK-1 (true)} * \text{CHAROFF-0 (false)}$

$\text{HORBLNK-0 (false)} = \text{DIALON-1 (true)} * \text{CHARCLK-1 (false)}$

OR

$\text{CHARCLK-1 (true)} * \text{HORBLNK-0 (false)}$

U464

Table B-17
U464 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	RDMWR-1
2	RFSHREQ-1
3	IOADREN-1
4	SCRNTIM-1
5	PIXELRD-1
6	RESET-1
7	Y10-1
8	X10-1
9	ALUACC-1
10	DDACLK-1
13	QX-1
14	QY-1
23	QZ-1

Table B-18
U464 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	WE-0
17	XS3-0
19	TRQE-0
20	CAS-0
21	COL-0
22	RAS-0

Pin 12 is ground; Pin 24 is Vcc; Pins 11, 16, and 18 are not connected.

Equations

$$\text{RAS-0 (false)} = \text{XS3-0 (false)}$$

OR

$$\text{RFSHREQ-1 (false)} * \text{IOADREN-1 (true)} * \text{QZ-1 (false)}$$

OR

$$\begin{aligned} &\text{RFSHREQ-1 (true)} * \text{ALUACC-1 (false)} * \text{RDMWR-1} \\ &\text{(false)} * \text{IOADREN-1 (false)} * \text{X10-1 (false)} * \\ &\text{Y10-1 (false)} * \text{DDACLK-1 (true)} * \text{QZ-1 (false)} * \\ &\text{QY-1 (false)} * \text{QX-1 (false)} \end{aligned}$$

OR

$$\begin{aligned} &\text{RFSHREQ-1 (true)} * \text{ALUACC-1 (false)} * \text{RDMWR-1} \\ &\text{(true)} * \text{PIXELRD-1 (false)} * \text{IOADREN-1 (false)} * \\ &\text{QZ-1 (false)} * \text{QY-1 (false)} * \text{QX-1 (false)} \end{aligned}$$

OR

$$\text{QZ-1 (false)} * \text{QX-1 (true)}$$

OR

$$\text{QY-1 (true)} * \text{QX-1 (false)}$$

XS3-0 (false) = PIXELRD-1 (true) * IOADREN-1 (false) * QZ-1 (true)
 * QY-1 (true) * QX-1 (true)

OR

RFSHREQ-1 (false) * IOADREN-1 (true) * SCRNTIM-1
 (false) * QZ-1 (true) * QY-1 (false) * QX-1
 (true)

OR

RFSHREQ-1 (true) * QY-1 (true)

COL-0 (false) = RFSHREQ-1 (false) * IOADREN-1 (true) * SCRNTIM-1
 (false) * QZ-1 (true) * QY-1 (false) * QX-1 (true)

OR

RFSHREQ-1 (true) * ALUACC-1 (false) * RDMWR-1
 (false) * IOADREN-1 (false) * X10-1 (false) *
 Y10-1 (false) * DDACLK-1 (true) * QZ-1 (false) *
 QY-1 (false) * QX-1 (false)

OR

RFSHREQ-1 (true) * ALUACC-1 (false) * RDMWR-1
 (true) * PIXELRD-1 (false) * IOADREN-1 (false) *
 QZ-1 (false) * QY-1 (false) * QX-1 (false)

OR

CAS-0 (false)

PAL INFORMATION

TRQE-0 (false) = XS3-0 (false)

OR

IOADREN-1 (false) * QZ-1 (false) * QX-1 (true)

OR

IOADREN-1 (false) * QY-1 (true) * QX-1 (false)

OR

SCRNTIM-1 (false) * QZ-1 (false) * QX-1 (true)

OR

IOADREN-1 (true) * SCRNTIM-1 (true) * QY-1 (true)

OR

RFSHREQ-1 (true) * QZ-1 (false) * QX-1 (true)

CAS-0 (false) = PIXELRD-1 (true) * IOADREN-1 (false) * QZ-1 (true)
* QY-1 (true) * QX-1 (true)

OR

IOADREN-1 (false) * QZ-1 (false) * QX-1 (true)

OR

IOADREN-1 (false) * QY-1 (true) * QX-1 (false)

OR

SCRNTIM-1 (false) * QZ-1 (false) * QX-1 (true)

OR

SCRNTIM-1 (false) * QY-1 (true) * QX-1 (false)

OR

RFSHREQ-1 (true) * QZ-1 (false) * QX-1 (true)

OR

RFSHREQ-1 (true) * QY-1 (true)

WE-0 (false) = PIXELRD-1 (true) * IOADREN-1 (false) * QZ-1 (true)
* QY-1 (true)

OR

RFSHREQ-1 (true) * PIXELRD-1 (true) * QZ-1 (true)
* QY-1 (true)

U467

Table B-19
U467 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	RDMWR-1
2	RFSHREQ-1
3	IOADREN-0
4	SCRNTIM-1
5	PIXELRD-1
6	RESET-1
7	ALUACC-1
8	OVLYLDCLK-1
9	DDACLK-1
10	Y10-1
11	X10-1
13	QX-1
14	QY-1
23	QZ-1

Table B-20
U467 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	DX-0
16	DY-0
17	XSX-0
18	DDAXS-0
19	EN86ACC-0
20	DDACLKEN-0
21	RAMCLKEN-0

Equations

$$DZ-0 \text{ (true)} = \text{PIXELRD-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QY-1 (true)}$$

OR

$$\text{IOADREN-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QY-1 (true)}$$

OR

$$\text{RFSHREQ-1 (true)} * \text{PIXELRD-1 (false)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QX-1 (true)}$$

OR

$$\text{RESET-1 (true)} * \text{QY-1 (true)} * \text{QX-1 (false)}$$

$$DY-0 \text{ (true)} = \text{RFSHREQ-1 (false)} * \text{IOADREN-1 (true)} * \text{RESET-1 (true)} * \text{SCRNTIM-1 (true)} * \text{OVLYLDCLK-1 (false)} * \text{QY-1 (true)}$$

OR

$$\text{RESET-1 (true)} * \text{QY-1 (true)} * \text{QX-1 (false)}$$

OR

$$\text{RESET-1 (true)} * \text{QZ-1 (false)} * \text{QX-1 (true)}$$

PAL INFORMATION

$DX-0 \text{ (true)} = \text{PIXELRD-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QY-1 (true)}$

OR

$\text{RFSHREQ-1 (false)} * \text{IOADREN-1 (true)} * \text{RESET-1 (true)} * \text{SCRNTIM-1 (false)} * \text{QY-1 (false)} * \text{QX-1 (true)}$

OR

$\text{IOADREN-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QY-1 (true)}$

OR

$\text{RFSHREQ-1 (false)} * \text{IOADREN-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (false)} * \text{QY-1 (false)}$

OR

$\text{RFSHREQ-1 (true)} * \text{ALUACC-1 (false)} * \text{RDMWR-1 (false)} * \text{IOADREN-1 (false)} * \text{X10-1 (false)} * \text{Y10-1 (false)} * \text{DDACLK-1 (true)} * \text{RESET-1 (true)} * \text{QZ-1 (false)} * \text{QY-1 (false)}$

OR

$\text{RFSHREQ-1 (true)} * \text{ALUACC-1 (false)} * \text{RDMWR-1 (true)} * \text{PIXELRD-1 (false)} * \text{IOADREN-1 (false)} * \text{RESET-1 (true)} * \text{QZ-1 (false)} * \text{QY-1 (false)}$

OR

XSX-0 (false)

$\text{XSX-0 (true)} = \text{RFSHREQ-1 (true)} * \text{PIXELRD-1 (false)} * \text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QX-1 (true)}$

OR

$\text{RESET-1 (true)} * \text{QZ-1 (false)} * \text{QY-1 (false)} * \text{QX-1 (true)}$

OR

$\text{RESET-1 (true)} * \text{QZ-1 (true)} * \text{QY-1 (true)} * \text{QX-1 (false)}$

RAMCLKEN-0 (true) = IOADREN-1 (true) * SCRNTIM-1 (true) * QZ-1
(true) * QY-1 (false) * QX-1 (true)

OR

RFSHREQ-1 (true) * QZ-1 (false)

OR

RFSHREQ-1 (true) * QX-1 (true)

OR

RFSHREQ-1 (true) * QY-1 (true)

EN86ACC-0 (true) = RFSHREQ-1 (false) * ALUACC-1 (true) *
IOADREN-1 (true) * QY-1 (true)

OR

RFSHREQ-1 (false) * ALUACC-1 (true) *
IOADREN-1 (true) * QX-1 (true)

OR

PIXELRD-1 (false) * IOADREN-1 (false) * QZ-1
(false) * QX-1 (true)

OR

PIXELRD-1 (false) * IOADREN-1 (false) * QY-1
(true) * QX-1 (false)

OR

ALUACC-1 (true) * QZ-1 (false) * QY-1 (false)
* QX-1 (false)

OR

RFSHREQ-1 (true) * PIXELRD-1 (false) * QZ-1
(false) * QX-1 (true)

OR

RFSHREQ-1 (true) * PIXELRD-1 (false) * QY-1
(true)

PAL INFORMATION

$DDACKEN-0 \text{ (true)} = RDMWR-1 \text{ (true)} * QY-1 \text{ (true)}$

OR

$RDMWR-1 \text{ (true)} * QX-1 \text{ (true)}$

OR

$RFSHREQ-1 \text{ (true)} * ALUACC-1 \text{ (false)} * RDMWR-1 \text{ (false)} * IOADREN-1 \text{ (false)} * X10-1 \text{ (false)} * Y10-1 \text{ (false)} * DDACK-1 \text{ (true)} * QZ-1 \text{ (false)} * QY-1 \text{ (false)} * QX-1 \text{ (false)}$

OR

$RFSHREQ-1 \text{ (true)} * ALUACC-1 \text{ (false)} * IOADREN-1 \text{ (false)} * X10-1 \text{ (true)} * QZ-1 \text{ (false)}$

OR

$RFSHREQ-1 \text{ (true)} * ALUACC-1 \text{ (false)} * IOADREN-1 \text{ (false)} * Y10-1 \text{ (true)} * QZ-1 \text{ (false)}$

OR

$DDAXS-0 \text{ (false)}$

$DDAXS-0 \text{ (true)} = IOADREN-1 \text{ (false)} * QX-1 \text{ (true)}$

OR

$IOADREN-1 \text{ (false)} * QY-1 \text{ (true)} * QX-1 \text{ (false)}$

OR

$RDMWR-1 \text{ (true)} * QZ-1 \text{ (false)}$

OR

$RFSHREQ-1 \text{ (true)} * QX-1 \text{ (true)}$

OR

$RFSHREQ-1 \text{ (true)} * QY-1 \text{ (true)}$

U470

Table B-21
U470 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	CLK-1
2	Q7-1
3	Q6-1
4	Q5-1
5	Q4-1
6	Q3-1
7	Q2-1
8	Q1-1
9	Q0-1

Table B-22
U470 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
12	HORZTC-0
13	ENVCNT-0
14	HSYNC-0
15	HBLANK-0
16	OVLYLDCLK-0
17	SCRNTIM-0
18	IOADREN-0
19	RFSHREQ-0

Pins 10 and 11 are ground; Pin 20 is Vcc.

Equations

$$\text{RFSHREQ-0 (true)} = \text{Q7-1 (true)} * \text{Q6-1 (false)} * \text{Q5-1 (true)} * \\ \text{Q4-1 (false)} * \text{Q3-1 (false)} * \text{Q2-1 (true)} * \\ \text{Q0-1 (true)}$$

OR

$$\text{Q7-1 (true)} * \text{Q6-1 (false)} * \text{Q5-1 (true)} * \\ \text{Q4-1 (false)} * \text{Q3-1 (false)} * \text{Q2-1 (true)} * \\ \text{Q1-1 (true)}$$

OR

$$\text{Q7-1 (true)} * \text{Q6-1 (false)} * \text{Q5-1 (true)} * \\ \text{Q4-1 (false)} * \text{Q3-1 (true)} * \text{Q0-1 (false)}$$

OR

$$\text{Q7-1 (true)} * \text{Q6-1 (false)} * \text{Q5-1 (true)} * \\ \text{Q4-1 (false)} * \text{Q3-1 (true)} * \text{Q1-1 (false)}$$

OR

$$\text{Q7-1 (true)} * \text{Q6-1 (false)} * \text{Q5-1 (true)} * \\ \text{Q4-1 (false)} * \text{Q3-1 (true)} * \text{Q2-1 (false)}$$

$$\text{IOADREN-0 (true)} = \text{Q7-1 (false)} * \text{Q6-1 (true)} * \text{Q5-1 (false)} * \\ \text{Q4-1 (true)} * \text{Q3-1 (false)}$$

SCRNTIM-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (true) *
 Q4-1 (false) * Q3-1 (true) * Q2-1 (false) *
 Q1-1 (true) * Q0-1 (true)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (true) *
 Q4-1 (false) * Q3-1 (true) * Q2-1 (true) *
 Q1-1 (false)

OVLYLDCLK-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q3-1 (false) * Q2-1 (false) *
 * Q1-1 (true)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q2-1 (true)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q3-1 (true)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (true)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (true) *
 Q4-1 (false) * Q3-1 (false)

OR

Q7-1 (true) * Q6-1 (false) * Q5-1 (true) *
 Q4-1 (false) * Q2-1 (false)

HBLANK-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q3-1 (false) * Q2-1 (false) *
 Q1-1 (true) * Q0-1(true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q2-1 (true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q3-1 (true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (true) * Q4-1
 (false) * Q3-1 (false)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (true) * Q4-1
 (false) * Q2-1 (false)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (true) * Q4-1
 (false) * Q1-1 (false)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (true) * Q4-1
 (false) * Q0-1 (false)
 HSYNC-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (false) * Q4-1
 (false) * Q3-1 (true) * Q2-1 (true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) * Q4-1
 (false) * Q3-1 (true) * Q1-1 (true)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) * Q4-1
 (true) * Q3-1 (false) * Q1-1 (false)
 OR
 Q7-1 (true) * Q6-1 (false) * Q5-1 (false) * Q4-1
 (true) * Q3-1 (false) * Q2-1 (false)
 HORZTC-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (true) * Q4-1
 (false) * Q3-1 (true) * Q2-1 (true) * Q1-1
 (true) * Q0-1 (false)
 ENVCNT-0 (true) = Q7-1 (true) * Q6-1 (false) * Q5-1 (false) *
 Q4-1 (false) * Q3-1 (true) * Q2-1 (false) *
 Q1-1 (true) * Q0-1 (false)

U478

Table B-23
U478 PIN-OUT AND
SIGNAL NAMES
(INPUTS)

Pin Number	Signal Name
1	CNTRCLK-1
2	V7-1
3	V6-1
4	V5-1
5	V4-1
6	V3-1
7	V2-1
8	V1-1
9	V0-1
10	HZ-1
11	LD-1
14	CE-1
23	RESET-1

Table B-24
U478 PIN-OUT AND
SIGNAL NAMES
(OUTPUTS)

Pin Number	Signal Name
15	VTC-0
16	HTC-0
17	V8-1
18	V9-1
19	VSYN-0
20	VBANK-0
21	HBLANK-1
22	HTCI-1

Pins 12 and 13 are ground; Pin 24 is Vcc.

Equations

$$V8-1 \text{ (false)} = LD-1 \text{ (true)} * V8-1 \text{ (false)}$$

OR

$$LD-1 \text{ (false)} * CE-1 \text{ (false)}$$

OR

$$LD-1 \text{ (true)} * CE-1 \text{ (false)} * V7-1 \text{ (true)} * V6-1 \text{ (true)} * V5-1 \text{ (true)} * V4-1 \text{ (true)} * V3-1 \text{ (true)} * V2-1 \text{ (true)} * V1-1 \text{ (true)} * V0-1 \text{ (true)}$$

$$V9-1 \text{ (false)} = LD-1 \text{ (true)} * V9-1 \text{ (false)}$$

OR

$$LD-1 \text{ (false)} * CE-1 \text{ (false)}$$

OR

$$LD-1 \text{ (true)} * CE-1 \text{ (false)} * V8-1 \text{ (true)} * V7-1 \text{ (true)} * V6-1 \text{ (true)} * V5-1 \text{ (true)} * V4-1 \text{ (true)} * V3-1 \text{ (true)} * V2-1 \text{ (true)} * V1-1 \text{ (true)} * V0-1 \text{ (true)}$$

VTC-0 (false) = V9-1 (true) * V8-1 (true) * V7-1 (false) * V6-1
 (false) * V5-1 (true) * V4-1 (false) * V3-1
 (false) * V2-1 (false) * V1-1 (false) * V0-1
 (false) * V0-1 (false) * HZ-1 (false) * CE-1
 (false)

OR

V9-1 (true) * V8-1 (true) * V7-1 (true) * V6-1
 (true) * V5-1 (false) * V4-1 (false) * V3-1
 (false) * V2-1 (false) * V1-1 (false) * V0-1
 (false) * V0-1 (false) * HZ-1 (true) * CE-1
 (false)

OR

RESET-1 (false)

VSYNC-0 (true) = V9-1 (true) * V8-1 (false) * V7-1 (true) *
 V6-1 (true) * V5-1 (true) * V4-1 (true) *
 V3-1 (true) * V2-1 (true) * V1-1 (true) *
 V0-1 (true) * V0-1 (true) * HZ-1 (false) *
 CE-1 (false)

OR

V9-1 (true) * V8-1 (true) * V7-1 (false) * V6-1
 (false) * V5-1 (false) * V4-1 (false) * V3-1
 (false) * V2-1 (false) * HZ-1 (false)

OR

V9-1 (true) * V8-1 (false) * V7-1 (false) *
 V6-1 (true) * V5-1 (false) * V4-1 (true) * V3-1
 (true) * V2-1 (true) * V1-1 (true) * V0-1
 (true) * V0-1 (true) * HZ-1 (true) * CE-1
 (false)

OR

V9-1 (true) * V8-1 (true) * V7-1 (false) * V6-1
 (true) * V5-1 (true) * V4-1 (false) * V3-1
 (false) * V2-1 (false) * HZ-1 (true)

VBLANK-0 (true) = V9-1 (true) * V8-1 (false) * V7-1 (true) *
 V6-1 (true) * V5-1 (true) * V4-1 (true) *
 V3-1 (true) * V2-1 (true) * V1-1 (true) *
 V0-1 (true) * V0-1 (true) * CE-1 (false)

OR

V9-1 (true) * V8-1 (true) * LD-1 (true)

VTC-0 (false) = RESET-1 (false) * HTCI-1 (false)



Appendix C

CX TERMINAL INTERFACING INFORMATION

This appendix describes the terminal-to-Cluster Controller-to-IBM host interface for the CX terminal (the Cluster Controller is also generally known as the Control Unit). The end of Section 4 presents a simplified theory of operation for the CX Interface board.

CX TERMINAL OVERVIEW

The CX terminals have the following device features:

- Connects to an IBM system through a coaxial cable as if it were an IBM 3279 terminal.
- Emulates an IBM terminal (model 2 or 3) when displaying alphanumeric text, 24 or 34 lines total. It displays the IBM "operator information line," or status line, at the bottom two lines of the screen.
- Uses an IBM-style 87-key typewriter keyboard layout, but adds a TEKTRONIX Joydisk and function keys.
- Connects to other host computers or protocol converters through the existing RS-232 host port connector, and is fully compatible with standard 4111 terminals despite the different keyboard layout.
- TEKTRONIX graphics commands and software are also supported when transmitted over the coax cable from an IBM host.
- Does not support the following IBM 3279 options: Programmable Symbol Cell Graphics (GDDM), APL keyboard and character set, magnetic card reader, light pen, and security keyswitch.

Figure C-1 shows how the CX terminal connects to the IBM mainframe. The coaxial cable leads from the terminal's host port BNC connector (labeled "COMM") to either an IBM 3274 Cluster Controller, an ICA, or to an IBM 43X1 host computer. The IBM 3274 attaches either to an IBM Host (or IBM compatible) or to an IBM Communications Controller (or compatible). For the coax connection (from the CX terminal), any references to a Cluster Controller can also refer to an ICA or an IBM 43X1 as an acceptable alternative.

CONNECTION FROM CLUSTER CONTROLLER TO HOST

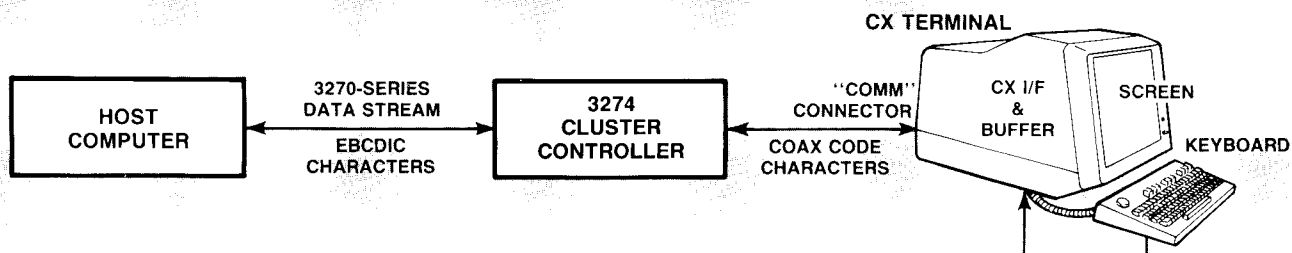
The details of the connection between the Cluster Controller and the host or communications controller are transparent to the terminal and its user. The connection may be over telephone lines and modems, or by an IBM "channel" direct to the host. It may use either the BSC or SNA/SDLC communications protocol for carrying data streams between the host and Cluster Controller. The important characteristics of this connection are as follows:

- The host or communications controller communicates with the Cluster Controller by command opcodes and text embedded in an "Extended 3270 Series Data Stream." Any text included in the data stream is encoded in IBM's EBCDIC¹ character code.
- The communications protocol (BSC or SNA/SDLC), between the Cluster Controller and host or communications controller, is directed by the host and is responsible for transporting the 3270 series data stream to and from the Cluster Controller.
- The host graphics applications programmer must format his commands as required by the 3270 series data stream. The details of the host I/O routines and how to send TEK graphics to the CX terminal are described in the CX4100 Series Host Support Manual (by TEKTRONIX).

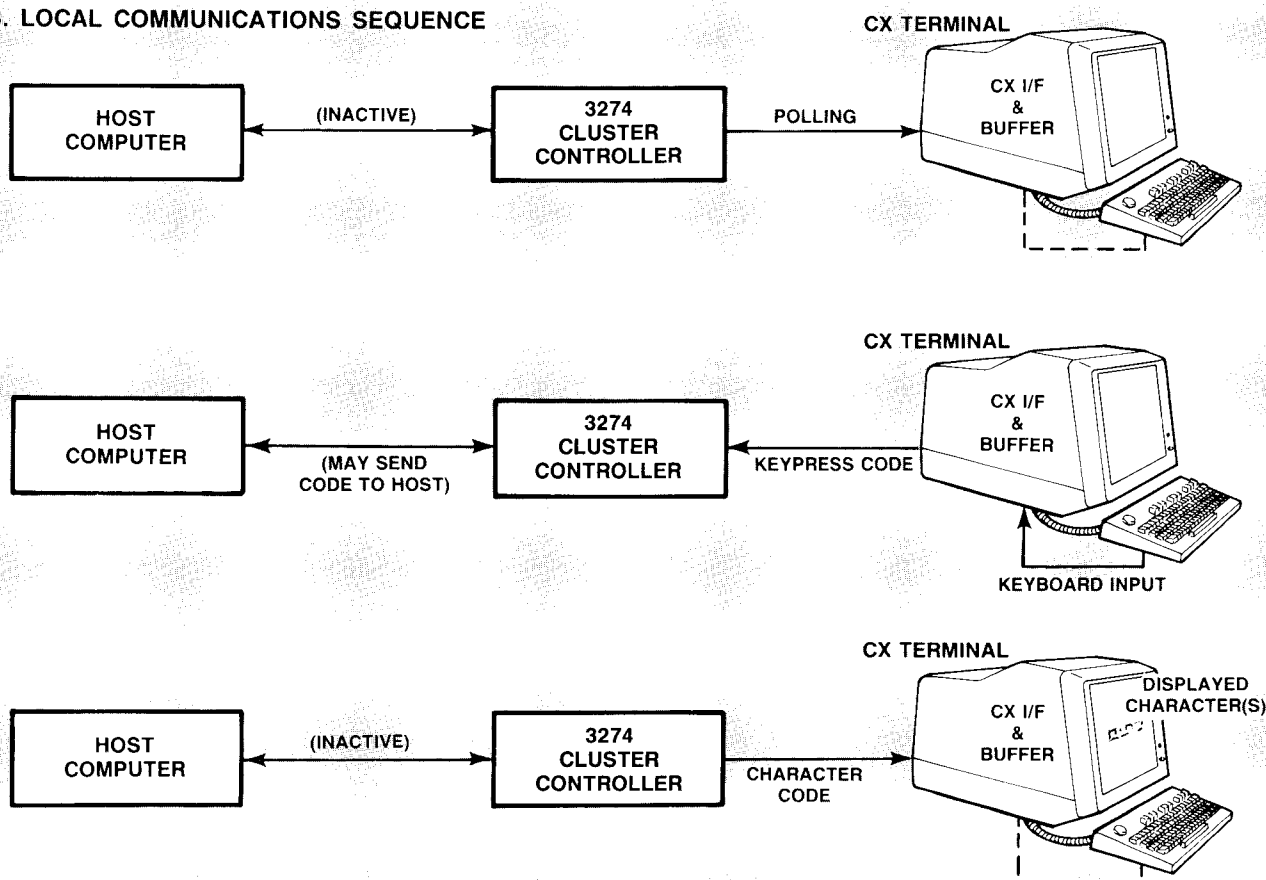
¹ Extended Binary Coded Decimal Interchange Code.

CX TERMINAL INTERFACING INFORMATION

A. HOST COMMUNICATION



B. LOCAL COMMUNICATIONS SEQUENCE



5644-115

Figure C-1. Connecting the CX Terminal to the IBM System Environment.

CONNECTION FROM TERMINAL TO CLUSTER CONTROLLER

In an IBM system, the terminal shares many of its intelligent functions with the Cluster Controller. The IBM terminology for the terminal is "display unit." The communications between the display unit and the Cluster Controller are on a fairly primitive level.

The Cluster Controller is continually polling the terminal. Actually, up to 32 "terminals" (displays or printers) may be coax-connected to a single Cluster Controller. The Cluster Controller continually polls its terminals to see if any need service².

When the operator presses a key, the terminal sends a keyscan code in response to the next poll from the Cluster Controller. The Cluster Controller then converts this code to a character code, using the special "coax code" character set. It sends the character code back to the terminal, writing it into the terminal's "character buffer." It is the responsibility of the terminal to display all text that is stored in its character buffer.

To send text onward to the host computer, the operator presses the ENTER key. The Cluster Controller then reads text from the terminal's character buffer and sends that text onward to the computer. In doing so, the Cluster Controller converts the characters from special "coax code," used in the terminal's character buffer, to the EBCDIC code used by the host computer. (Refer ahead to Figures C-3 through C-8 for specific EBCDIC Code Charts.)

Also, when the operator of the CX terminal presses the LOCAL COPY key (lower left corner of the keyboard), the Cluster Controller interprets the LOCAL COPY keyscan code as a command to spool the text from the terminal to the printer that is attached to another of the Cluster Controller's coax ports. It reads text from the terminal's character buffer, sends that text to a similar character buffer in the printer, and then commands the printer to print its buffer contents.

² This does not refer to repair.

PHYSICAL INTERFACE AND MODULATION SCHEME

The terminal-to-Cluster Controller interface is a type RS62A/U coaxial cable. The cable coming from the Cluster Controller has a male BNC connector, which mates with the female BNC connector on the terminal.

Data is transmitted serially in either direction, but in only one direction at a time. The bit rate of the data transfer is 2.3587 MHz. The Cluster Controller acts as a master, the terminal is a slave.

A biphasic modulation scheme is used.³ Bits on the coax appear as positive-going and negative-going voltage changes in the middle of their respective 424 ns bit intervals. A positive voltage change (in the middle of a bit interval) represents a binary 1, while a negative voltage change represents a binary 0. That is, a 1 is represented by a 212 ns low level, followed by a 212 ns high level; while a 0 is represented by a 212 ns high level, followed by a 212 ns low level.

The transmitting device (Cluster Controller or terminal) generates a predistorted pulse for each transition from high to low or visa versa. Figure C-2 shows these waveforms. Figures C-2A and C-2B show waveforms measured across the coaxial cable at the transmitting end. Figures C-2C and C-2D show the same waveforms as they appear after being attenuated and distorted by the maximum cable length of 5,000 feet (1,524 m). By using an IBM 3299, one can extend the cable length to 10,000 feet (3,048 m).

³ The wave-train consists of two types of pulse patterns: bi-phase 0, and bi-phase 1. These are shown in Figure C-2A and B.

CX TERMINAL INTERFACING INFORMATION

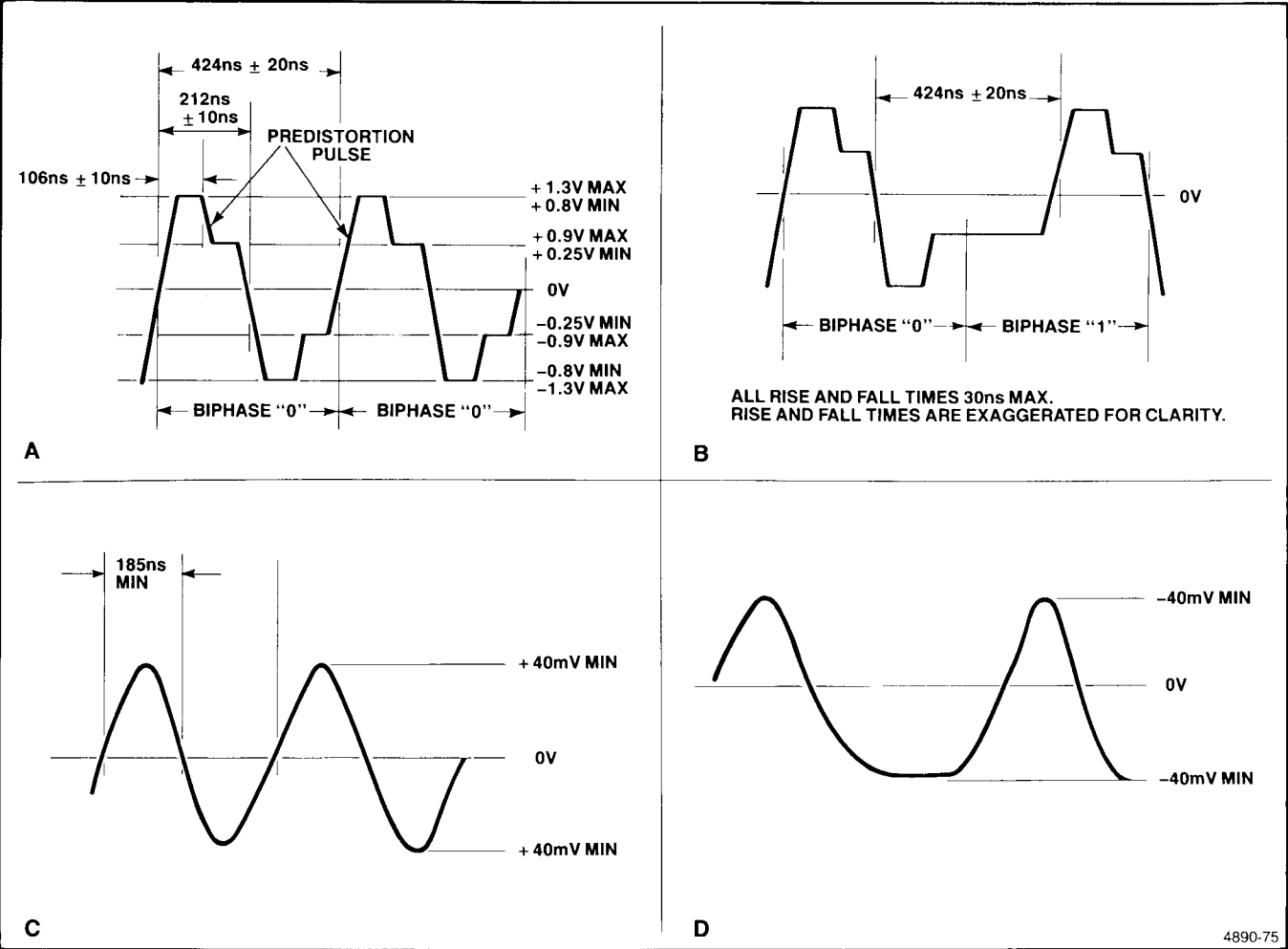


Figure C-2. Waveforms on the Coaxial Cable.

BINARY BITS	0,1		00				01				10				11			
	2,3		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	4,5,6,7	HEX 1 0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL					SP	&	—						{	}	\	0
0001	1		SBA						/		a	j	~		A	J		1
0010	2		EUA								b	k	s		B	K	S	2
0011	3		IC								c	l	t		C	L	T	3
0100	4										d	m	u		D	M	U	4
0101	5	PT	NL								e	n	v		E	N	V	5
0110	6										f	o	w		F	O	W	6
0111	7										g	p	x		G	P	X	7
1000	8	GE		SA							h	q	y		H	Q	Y	8
1001	9		EM	SFE					`		i	r	z		I	R	Z	9
1010	A						¢	!		:								
1011	B						.	\$,	#								
1100	C	FF	DUP	MF	RA		<	*	%	@								
1101	D	CR	SF				()	—	'								
1110	E		FM				+	;	>	=								
1111	F				SUB			⌐	?	"								

4890-68A

Figure C-3. North American EBCDIC Code Chart.

CX TERMINAL INTERFACING INFORMATION

BINARY BITS	0,1		00				01				10				11			
	2,3		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	4,5,6,7	HEX 1 0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		NUL				SP	&	—						{	}	\	0
0001	1			SBA					/		a	j	—		A	J		1
0010	2			EUA							b	k	s		B	K	S	2
0011	3			IC							c	l	t		C	L	T	3
0100	4										d	m	u		D	M	U	4
0101	5		PT	NL							e	n	v		E	N	V	5
0110	6										f	o	w		F	O	W	6
0111	7										g	p	x		G	P	X	7
1000	8		GE		SA						h	q	y		H	Q	Y	8
1001	9			EM	SFE				`		i	r	z		I	R	Z	9
1010	A						\$!		:								
1011	B						.	£	,	#								
1100	C		FF	DUP	MF	RA	<	*	%	@								
1101	D		CR	SF			()	—	'								
1110	E			FM			+	;	>	=								
1111	F					SUB		⌐	?	"								

4890-69A

Figure C-4. United Kingdom EBCDIC Code Chart.

BINARY BITS	0,1	00				01				10				11			
		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	4,5,6,7 HEX 1 0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL				SP	&	—						é	è	c	0
0001	1		SBA					/		a	j	..		A	J		1
0010	2		EUA			^ a	^ e			b	k	s		B	K	S	2
0011	3		IC			ä	ë			c	l	t		C	L	T	3
0100	4									d	m	u		D	M	U	4
0101	5	PT	NL							e	n	v		E	N	V	5
0110	6						i			f	o	w		F	O	W	6
0111	7						ï			g	p	x		G	P	X	7
1000	8	GE		SA						h	q	y		H	Q	Y	8
1001	9		EM	SFE						i	r	z		I	R	Z	9
1010	A					°	§	ù	:								
1011	B					.	\$,	£					^ o	^ u		
1100	C	FF	DUP	MF	RA	<	*	%	` a					ö	ü		
1101	D	CR	SF			()	—	'								
1110	E		FM			+	;	>	=								
1111	F				SUB	!	^	?	"						ÿ		

^a AZERTY Keyboard.

4890-70A

Figure C-5. French EBCDIC Code Chart.

CX TERMINAL INTERFACING INFORMATION

BINARY BITS	0,1		00				01				10				11			
	2,3		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	4,5,6,7	HEX	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		NUL				SP	&	—						ä	å	É	0
0001	1			SBA					/		a	j	ü		A	J		1
0010	2			EUA							b	k	s		B	K	S	2
0011	3			IC							c	l	t		C	L	T	3
0100	4										d	m	u		D	M	U	4
0101	5		PT	NL							e	n	v		E	N	V	5
0110	6										f	o	w		F	O	W	6
0111	7										g	p	x		G	P	X	7
1000	8		GE		SA						h	q	y		H	Q	Y	8
1001	9			EM	SFE				é		i	r	z		I	R	Z	9
1010	A						§	œ	o	:								
1011	B						.	Å	,	Ä								
1100	C		FF	DUP	MF	RA	<	*	%	Ö								
1101	D		CR	SF			()	—	'								
1110	E			FM			+	;	>	=								
1111	F					SUB	!	^	?	"								

4890-71A

Figure C-6. Swedish EBCDIC Code Chart.

BINARY BITS	0,1		00				01				10				11			
	2,3		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	HEX -1 0		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0	NUL					SP	&	—						æ	å	\	0
0001	1		SBA						/		a	j	ü		A	J		1
0010	2		EUA								b	k	s		B	K	S	2
0011	3		IC								c	l	t		C	L	T	3
0100	4										d	m	u		D	M	U	4
0101	5	PT	NL								e	n	v		E	N	V	5
0110	6										f	o	w		F	O	W	6
0111	7										g	p	x		G	P	X	7
1000	8	GE		SA							h	q	y		H	Q	Y	8
1001	9		EM	SFE					\		i	r	z		I	R	Z	9
1010	A						§	×	φ	:								
1011	B						.	Å	,	Æ								
1100	C	FF	DUP	MF	RA		<	*	%	Ø								
1101	D	CR	SF				()	—	'								
1110	E						+	;	>	=								
1111	F				SUB		!	^	?	"								

4890-72A

Figure C-7. Danish/Norwegian EBCDIC Code Chart.

CX TERMINAL INTERFACING INFORMATION

BINARY BITS	0,1		00				01				10				11			
	2,3		00	01	10	11	00	01	10	11	00	01	10	11	00	01	10	11
	HEX 1 0		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0000	0		NUL				SP	&	—						ä	ü	Ö	0
0001	1			SBA					/		a	j	ß		A	J		1
0010	2			EUA							b	k	s		B	K	S	2
0011	3			IIC							c	l	t		C	L	T	3
0100	4										d	m	u		D	M	U	4
0101	5		PT	NL							e	n	v		E	N	V	5
0110	6										f	o	w		F	O	W	6
0111	7										g	p	x		G	P	X	7
1000	8		GE		SA						h	q	y		H	Q	Y	8
1001	9				EM	SFE				˘	i	r	z		I	R	Z	9
1010	A						Ä	Ü	ö	:								
1011	B						.	\$,	#								
1100	C		FF	DUP	MF	RA	<	*	%	§								
1101	D		CR	SF			()	—	'								
1110	E			FM			+	;	>	=								
1111	F					SUB	!	^	?	"								

4890-73A

Figure C-8. German EBCDIC Code Chart.